IM4702/4712
Baud Rate Generator

INTERSIL

T-75-33-09

GENERAL DESCRIPTION

The IM4702/12 Baud Rate Generators provide necessary clock signals for digital data transmission systems, such as UARTs, using a 2.4576MHz crystal oscillator as an input. They control up to 8 output channels and can be cascaded for output expansion.

Output rate is controlled by four digital input lines, and with the specified crystal, is selectable from "zero" through 9600 Baud. In addition, 19200 Baud is possible via hardwiring.

Multi-channel operation is facilitated by making the clock frequency and the ÷8 prescaler outputs available externally. This allows up to eight simultaneous Baud rates to be generated.

The IM4712 is identical to the IM4702 with the exception that the IM4712 integrates the oscillator feedback resistor and two load capacitors on-chip.

ORDERING INFORMATION

Order Number	Temperature Range	Package
IM4702IJE	−40°C to +85°C	16-pin CERDIP
IM4702IPE	−40°C to +85°C	16-pin PLASTIC
IM4712IJE	−40°C to +85°C	16-pin CERDIP
IM4712IPE	−40°C to +85°C	16-pin PLASTIC

FEATURES

- **Provides 14 Most Commonly Used BAUD Rates**
- **On-Chip Oscillator Requires Only One External Part (IM4712)**
- **Controls Up to Eight Transmission Channels**
- **TTL Compatible Outputs Will Sink 1.6mA**
- **Uses Standard 2.4576MHz Crystal**
- **Low Power Consumption: 5.5mW Guaranteed Maximum Standby**
- **Pin and Function Compatible With 4702B and HD-4702**
- **Inputs Feature Active Pull-Ups**

PIN DESCRIPTION

Signal	Pin	Description
Q_0-Q_2	1,2,3	Prescaler Outputs
$\overline{ECP}$	4	External Clock Enable Input
CP	5	External Clock Input
O_X	6	Crystal Output
I_X	7	Crystal Input
V_{SS}	8	Negative Supply
C_0	9	Clock Output
Z	10	Baud Rate Output
S_0-S_3	14-11	Baud Rate Select Inputs
I_M	15	Multiplexed Input
V_{DD}	16	Positive Supply

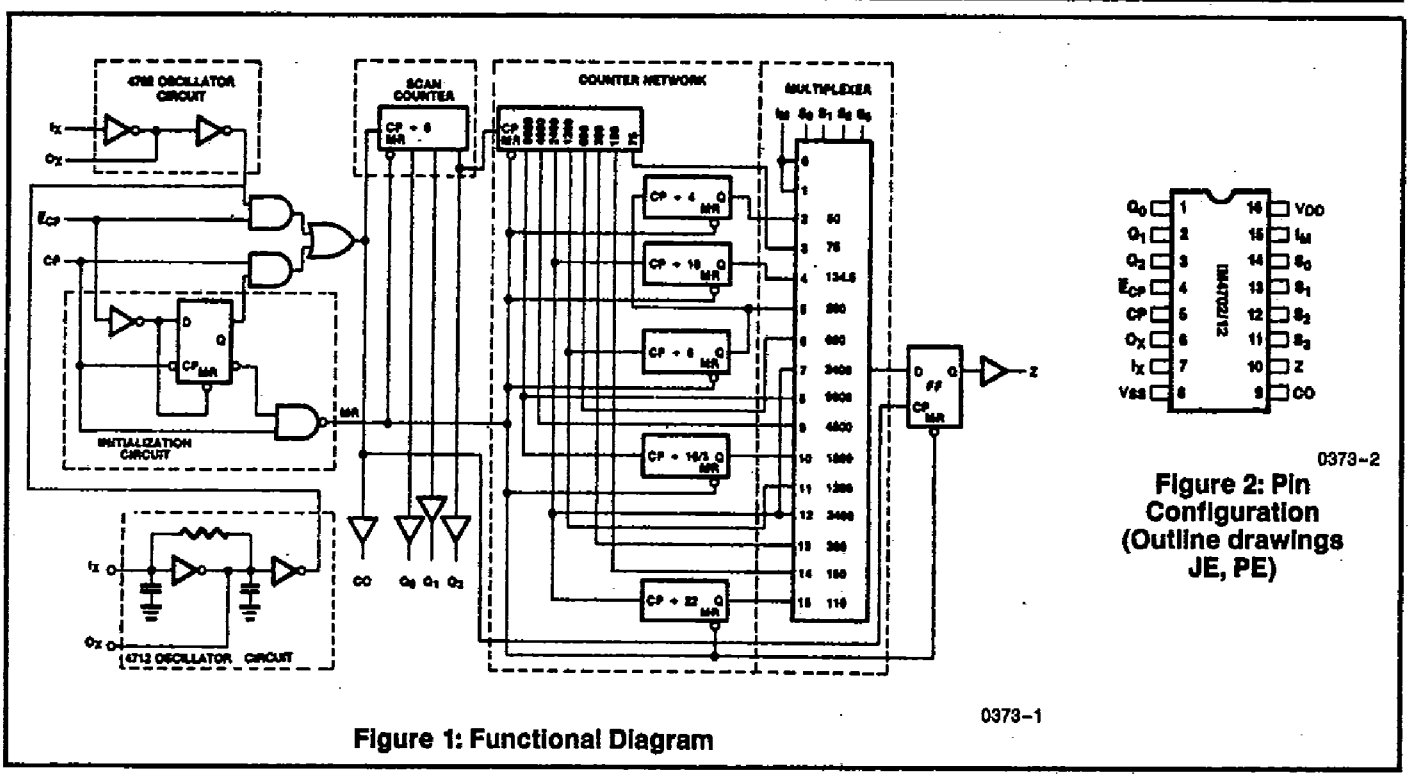


Figure 1: Functional Diagram

Figure 2: Pin Configuration (Outline drawings JE, PE)

NOTE: All typical values have been characterized but are not tested.

IM4702/4712

INTERSIL

T-75-33-09

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) ..... +8.0V
Input or Output Voltage ..... V_{SS} −0.3V to V_{DD}+0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... −40°C to +85°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS $V_{DD}=+5V\pm10\%$ $V_{SS}=0V$, $T_A=-40°C$ to $+85°C$

Symbol	Parameter		Test Conditions	Limits		Units
				Min	Max	
V_{IH}	Input Voltage High			70% V_{CC}		V
V_{IL}	Input Voltage Low				30% V_{CC}	
I_{IH}	Input Current High	Other Inputs	$V_{IN}=V_{DD}$ All other pins grounded		+1	
		I_X 4712			+10	
I_{IL}	Input Current Low	I_X 4702	Pin under test at ground All other Inputs at V_{DD}		−1	μA
		I_X 4712			+10	
		Other Inputs		−15	−100	
V_{OH}	Output Voltage High		$I_{OH}<-1\mu A$; Inputs at V_{SS} or V_{DD}	$V_{DD}-.05$		V
V_{OL}	Output Voltage Low		$I_{OL}<+1\mu A$; Inputs at V_{SS} or V_{DD}		0.05	
I_{OH}	Output Current High	O_X	Inputs at V_{SS} or V_{DD} $V_O=V_{DD}-.5$	−0.1		mA
		All other Outputs		−0.3		
			$V_O=+2.5V$	−1.0		
I_{OL}	Output Current Low	O_X	$V_O=0.4$; Inputs at V_{SS} or V_{DD}	−0.1		
		All other Outputs		1.6		
I_{STBY}	Quiescent Supply Current		$\overline{E}_{CP}=V_{DD}$; $CP=V_{SS}$ All other Inputs = V_{SS} or V_{DD}, All outputs open		1.0	

INTERSIL

T-75-33-09

AC CHARACTERISTICS $V_{DD} = +5V\ V_{SS} = 0V, T_A = 25°C$

Symbol	Parameter		Test Conditions	Limits Min	Limits Max	Units
t_{plh}(4702)	Propagation delay(1), I_x to CO		C_L (except O_x) = 50pF $C_{L(Ox)}$ = 7pF R_L = 200kΩ Input Transition times ≤20ns Input low = 1.0V Input high = V_{CC} − 1.0V		350	ns
t_{phl}(4702)					275	
t_{plh}(4712)					350	
t_{pll}(4712)					275	
t_{plh}	Propagation delay(1), CP to CO				260	
t_{phl}					220	
t_{plh}	Propagation delay(1), CO to Q_n				(2)	
t_{phl}					(2)	
t_{plh}	Propagation delay(1), CO to Z				85	
t_{phl}					75	
t_{tlh}	Output Transition Time, (1) (except O_x)				160	
t_{thl}					75	
t_s	Set Up Time	Select to CO		350		
		I_M to CO		350		
t_h	Hold Time	Select to CO		0		
		I_M to CO		0		
$t_wCP(L)$	Clock pulse width(3)			120		
$t_wCP(H)$				120		
$t_wI_x(L)$(4702)				160		
$t_wI_x(H)$(4702)	I_x Pulse Width			160		
$t_wI_x(L)$(4712)				190		
$t_wI_x(H)$(4712)				190		

NOTES: 1. Propagation delays and output transition times will vary with output load capacitance.
2. For multichannel operation, propagation delay (CO to Q_n) plus set-up time (Select to CO) is guaranteed to be less than 367ns for the IM4702/12.
3. The first high level clock pulse after $\overline{E}_{cp}$ goes low must be at least 200ns wide to ensure resetting of all counters.
4. For design reference only, not 100% tested.

T-75-33-09

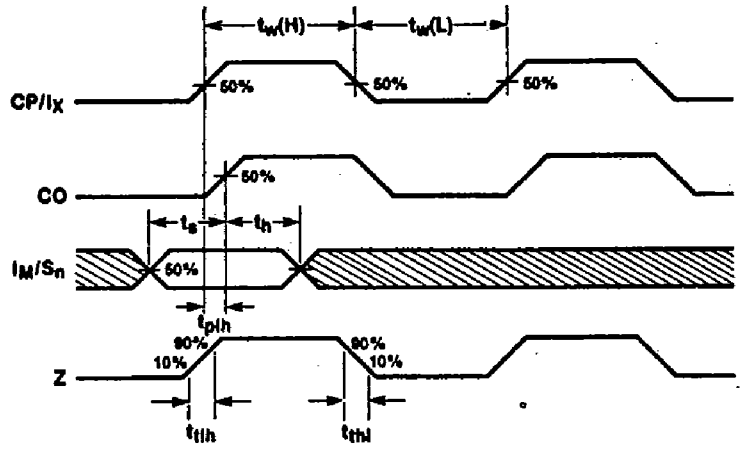


Figure 3: Switching Waveforms

FUNCTIONAL DESCRIPTION

Digital data transmission systems employ a wide range of standardized bit rates, ranging from 50 baud (for electromechanical devices) to 9600 baud (for high speed modems). Modern electronic systems commonly use Universal Asynchronous Receiver and Transmitter circuits (UARTs) to convert parallel data inputs into a serial bit stream (transmitter) and to reconvert the serial bit stream into parallel outputs (receiver). In order to resynchronize the incoming serial data, the reciever requires a clock rate which is a multiple of the incoming bit rate. Popular MOSLSI UART circuits use a clock that is 16 times the transmitted bit rate. The IM4702/12 can generate 14 standard clock rates from one common high frequency input.

The IM4702/12 contains the following five function subsystems.

Oscillator — For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 baud x 16 x 16, since the scan counter and the first flip-flop of the counter chain act as an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The IM4702/12 can be driven from two alternate clock sources: (1) When the $\overline{E}_{cp}$ (External Clock Enable) input is LOW, the CP input is the clock source. (2) When the $\overline{E}_{cp}$ input is HIGH, a crystal connected between I_X and O_X, or a signal applied to the I_x input, is the clock source.

Prescaler (Scan Counter) — The clock frequency is made available on the CO (Clock Output) pin and is applied to the ÷ 8 prescaler with buffered outputs Q_0, Q_1, and Q_2.

Table 1: Clock Modes and Initialization

I_X	$\overline{E}_{CP}$	CP	Operation
⎍⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍	Reset During First CP = HIGH Time

H = HIGH Level
L = LOW Level
X = Don't Care
⎍ = 1st HIGH Level Clock Pulse After $\overline{E}_{CP}$ Goes LOW
⎍⎍⎍ = Clock Pulses

0373-8

Counter Network — The prescaler output Q_2 is a square wave of ⅛ the input frequency, and is used to drive the frequency counter network generating 13 standardized frequencies. Note that the frequencies are labeled in the block diagram and described in terms of the transmission bit rate. In a conventional system using a 2.4576MHz clock input, the actual output frequencies are 16 times higher.

The output from the first frequency divider flip-flop is thus labeled 9600, since it is used to transmit or receive 9600 baud (bits per second). The actual frequency at this node is 16 x 9.6kHz = 153.6kHz. Seven more cascaded binaries generate the appropriate frequencies for bit rates 4800, 2400, 1200, 600, 300, 150, and 75.

T-75-33-09

The other five bit rates are generated by individual counters:

bit rate 1200 is divided by 6 to generate bit rate 200,

bit rate 200 is divided by 4 to generate bit rate 50,

bit rate 2400 is divided by 18 to generate bit rate 134.5 with a frequency error of −0.87%,

bit rate 2400 is also divided by 22 to generate bit rate 110 with a frequency error of −0.83%, and

bit rate 9600 is divided by 16/3 to generate bit rate 1800.

The 16/3 division is accomplished by alternating the divide ratio between 5 (twice) and 6 (once). The result is an exact average output frequency with some frequency modulation. Taking advantage of the ÷ 16 feature of the UART, the resulting distortion is less than 0.78% regardless of the number of elements in a character, and therefore well within the timing accuracy specified for high speed communications equipment. All signals except 1800, have a 50% duty cycle.

Output Multiplexer — The outputs of the counter network are fed to a 16-input multiplexer, which is controlled by the Rate Select inputs (S_0-S_3). The multiplexer output is then resynchronized with the incoming clock in order to cancel all cumulative delays and to present an output signal at the buffered output (Z) that is synchronous with the prescaler outputs (Q_0-Q_2). Table 2 lists the correspondance between select code and output bit rate. Two of the 16 codes do not select an internally generated frequency, but select an input into which the user can feed either a different, non-standardized frequency, or a static level (HIGH or LOW) to generate "zero baud".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 baud) require that no more than one input be grounded, easily achieved with a single pole, 5-position switch. 2400 baud is selected by two different codes, so that the whole spectrum of modern digital communication rates has a common HIGH on the S_3 input.

Initialization (Reset) — The initialization circuit generates a common master reset signal for all flip-flops in the IM4702/12. This signal is derived from a digital differentiator that senses the first HIGH level on the CP input after the $\overline{E}_{CP}$ input goes LOW. Upon initialization, all counters are reset and all outputs will be in the LOW state. When $\overline{E}_{CP}$ is HIGH, selecting the Crystal input, CP must be LOW; a HIGH level on CP would apply a continuous reset.

All inputs to the 4702/12 except I_X have on-chip pull-up circuits; the I_X input of the 4712 has a high value resistor tied to O_X.

Table 2: Truth Table for Rate Select Inputs

S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

L = LOW Level
H = HIGH Level

Note 1: Actual output frequency is 16 times the indicated output rate, assuming a clock frequency of 2.4576MHz.

Table 3: Crystal Specifications

Parameters	Typical Crystal Spec
Frequency	2.4576MHz "AT" Cut
Series Resistance (Max)	250Ω
Unwanted Modes	−6dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF ± 0.5pF

APPLICATIONS

Single Channel Bit Rate Generator

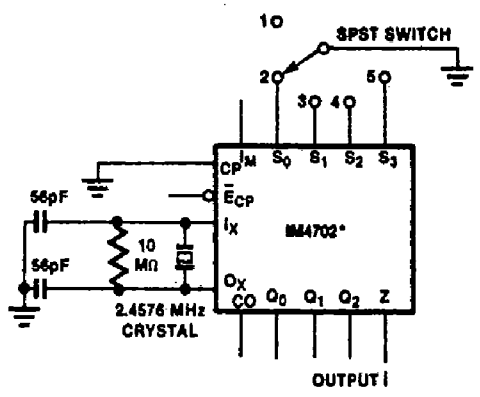
Figure 4 shows the simplest application of the IM4702/12. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 100, 150, 300, 1200, and 2400 or 3600 Baud. For many low cost terminals, these five bit rates are adequate.

This mode of operation is commonly chosen for applications using industry standard 1402/6402 UARTs.

IM4702/4712

INTERSIL

T-75-33-09



0373-4

Switch Position	Bit Rate
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

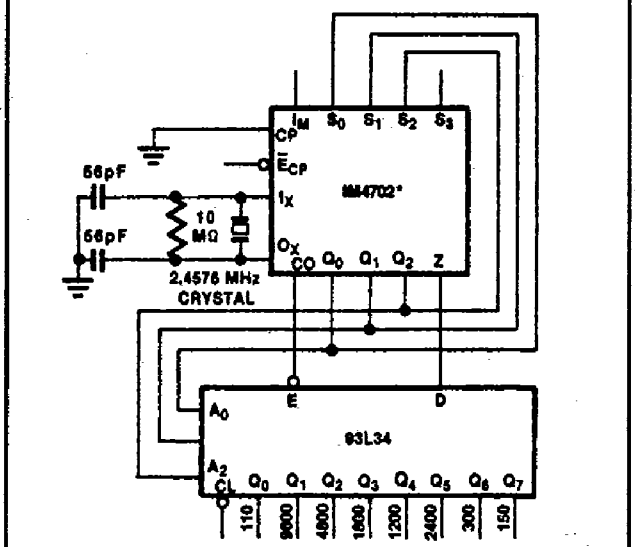
Figure 4: Switch Selectable Bit Rate Generator Configuration Providing Five Bit Rates

Simultaneous Generation of Several Bit Rates

Figure 5 shows a simple scheme that generates eight bit rates on eight output lines, using one IM4702/12 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select inputs of the multiplexer causes the IM4702/12 to sequentially interrogate the state of eight different frequency signals. The 93L34 Bit Addressable Latch, addressed by the same Scan Counter Outputs, reconverts the multiplexed single Output (Z) into eight parallel output frequency signals. In the simple scheme of Figure 5, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud	Q_3: 1800 Baud	Q_6: 300 Baud
Q_1: 9600 Baud	Q_4: 1200 Baud	Q_7: 150 Baud
Q_2: 4800 Baud	Q_5: 2400 Baud	

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

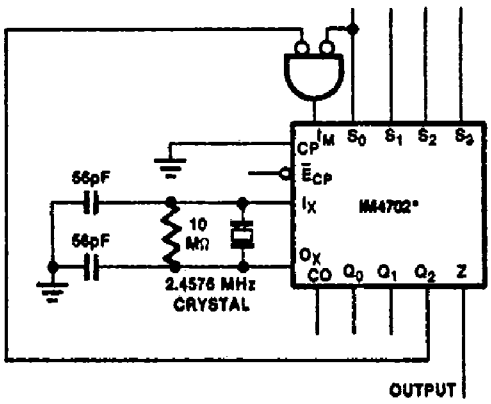


0373-5

Figure 5: Bit Rate Generator Configuration With Eight Simultaneous Frequencies

19200 Baud Operation

A 19200 baud signal is available on the Q_2 output, but is not internally connected to the multiplexer. This signal can be generated on the Z output by connecting the Q_2 output to the I_M input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the IM4702/12. (See Figure 6).



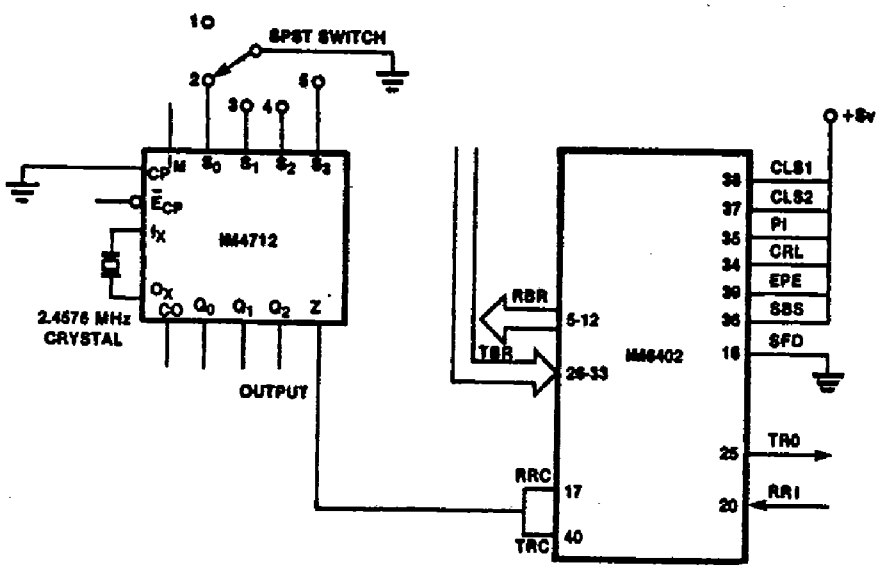
0373-6

Figure 6: 19200 Baud Operation

* The 4712 may replace the 4702 in the above applications with the standard 2.4576MHz crystal. The two external capacitors and one resistor are not required when using the 4712.

NOTE: All typical values have been characterized but are not tested.

T-75-33-09



0373-7

Figure 7: IM4712 Baud Rate Generator With IM6402 CMOS UART