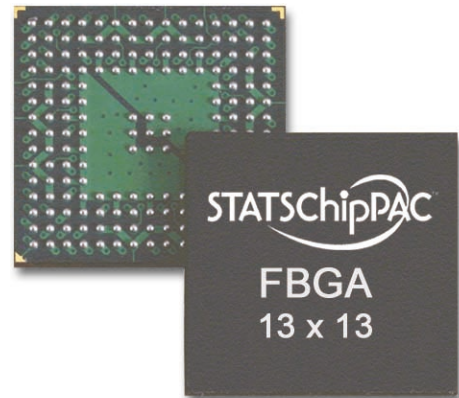


FBGA

Fine Pitch Ball Grid Array

- Array molded, cost effective, space saving package solution
- Available in 1.40mm (LFBGA), 1.20mm (TFBGA), and 1.00mm (VFBGA), 0.80mm (WFBGA) and 0.55mm (UFBGA) maximum thickness
- Laminate substrate based package which enables 2 and 4 layers of routing flexibility



FEATURES

- Thin, lightweight, space saving package
- Flexible body sizes range from 4mm x 4mm to 23mm x 23mm
- 0.50, 0.65, 0.75, 0.80, 1.00mm ball pitch
- Eutectic & Pb free solder balls
- Green package available
- Multiple routing layers and dedicated ground/power planes available for improved electrical performance
- BT laminate materials (2 and 4 metal layers)
- JEDEC standard compliant

APPLICATIONS

- Microprocessors/Controllers
- Wireless RF
- Analog
- ASIC
- Memory
- Simple PLDs
- Others

DESCRIPTION

STATS ChipPAC's Fine Pitch Ball Grid Array (FBGA) is a laminate substrate based chip scale package with plastic overmolded encapsulation and an array of fine pitch solder ball terminals. The FBGA package's reduced outline and thickness and higher density options make it an ideal advanced technology packaging solution for high performance and/or portable applications. The use of the latest materials and advanced assembly infrastructure produce a reliable and cost effective package. Lead free and halogen free compatible material sets are available. STATS ChipPAC's FBGA is available in a broad range of JEDEC standard body sizes with LFBGA (<1.70mm [typically <1.40mm]), TFBGA (<1.20mm), VFBGA (<1.00mm), WFBGA (<0.80mm) and UFBGA (0.55mm max.) thickness. LFBGA-H (with attached heatsink) is qualified for small body sizes.

FBGA

Fine Pitch Ball Grid Array

SPECIFICATIONS

Die Thickness	75–300µm (3-12 mils)
Mold Cap Thickness	0.25-0.90mm
Marking	Laser
Packing Options	Tape & reel/JEDEC tray

RELIABILITY

Moisture Sensitivity Level	JEDEC Level 2A, 260°C Reflow
Temperature Cycling	Condition C (-65°C to 150°C), 1000 cycles
High Temp Storage	150°C, 1000 hrs
Pressure Cooker Test	121°C/100% RH/2atm, 168 hrs
Temperature/Humidity Test	85°C/85% RH, 1000 hrs
Unbiased HAST	130°C/85% RH/2 atm, 96 hrs

THERMAL PERFORMANCE, θ_{ja} (°C/W)

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

Package	Body Size (mm)	Pin Count	Die Size (mm)	Thermal Performance θ_{ja} (°C/W)
LFBGA	11 x 11 (2L)	144	4.5 x 4.5	34.1
	15 x 15 (4L)	208	10.2 x 10.2	19.4

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2.

ELECTRICAL PERFORMANCE

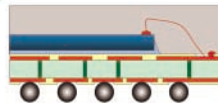
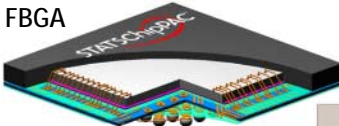
Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (2L)	2 - 7	34 - 119	1.30 - 4.55	0.26 - 2.28	0.25 - 0.95	0.06 - 0.42
Total (2L)	4 - 9	154 - 239	2.95 - 6.20	0.71 - 3.13	0.35 - 1.05	0.07 - 0.44
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (4L)	2 - 7	34 - 119	0.90 - 3.15	0.18 - 1.58	0.35 - 1.10	0.06 - 0.42
Total (4L)	4 - 9	154 - 239	2.55 - 4.80	0.63 - 2.43	0.45 - 1.20	0.07 - 0.44

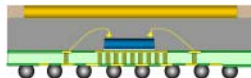
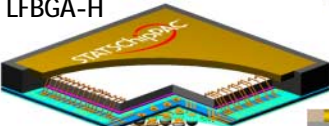
Note: Net = Total Trace Length + Via + Solder Ball.

CROSS-SECTION

FBGA



LFBGA-H



PACKAGE CONFIGURATIONS

Body Sizes (mm)	4x4 to 23x23; Common body sizes: 5x10, 7x9, 8x10, 8x11, 8x12, 8x14, 10x12, 10x14, 13x13, 15x15, 16x16, 17x17
Ball Count	40 to 450
Ball Pitch (mm)	0.50 to 0.80
Typ. Pkg. Thickness	LFBGA: 1.70mm (1.40mm max. typical) TFBGA: 1.20mm max. VFBGA: 1.00mm max. WFBGA: 0.80mm max. UFBGA: 0.55mm max.

Corporate Office 10 Ang Mo Kio St. 65, #05-17/20 Techpoint, Singapore 569059 Tel: 65-6824-7777 Fax: 65-6720-7823

Global Offices USA 510-979-8000 JAPAN 81-3-5789-5850 CHINA 86-21-5976-5858 MALAYSIA 603-4257-6222
KOREA 82-31-639-8911 TAIWAN 886-3-593-6565 UK 44-1483-413-700 NETHERLANDS 31-38-333-2023

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