

MC10EPT20, MC100EPT20

3.3V LVTTTL/LVCMOS to Differential LVPECL Translator

The MC10EPT20 is a 3.3 V TTL/CMOS to differential PECL translator. Because PECL (Positive ECL) levels are used, only +3.3 V and ground are required. The small outline SOIC-8 package and the single gate of the EPT20 makes it ideal for those applications where space, performance, and low power are at a premium.

The 100 Series contains temperature compensation.

- 390 ps Typical Propagation Delay
- Maximum Input Clock Frequency > 1 GHz Typical
- Operating Range $V_{CC} = 3.0\text{ V}$ to 3.6 V with $GND = 0\text{ V}$
- PNP TTL Input for Minimal Loading
- Q Output will Default HIGH with Input Open
- Pb-Free Packages are Available



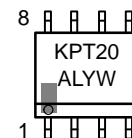
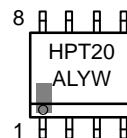
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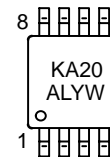
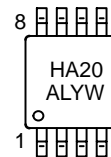
MARKING DIAGRAMS*



SO-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location

L = Wafer Lot
Y = Year
W = Work Week

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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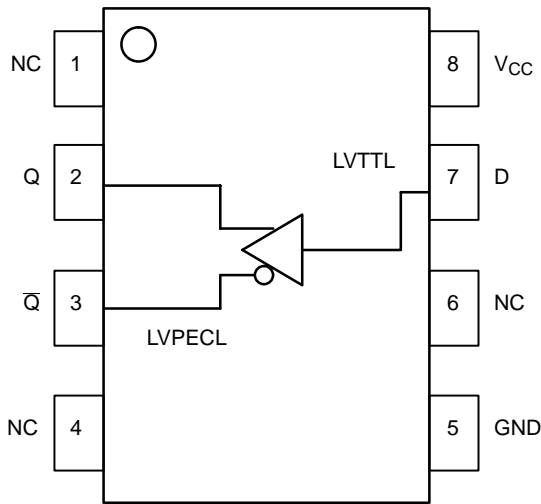


Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q, \bar{Q}	Differential PECL Outputs
D	LVTTTL Input
V _{CC}	Positive Supply
GND	Ground
NC	No Connect

Figure 1.8—Lead Pinout (Top View) and Logic Diagram

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 1.5 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in
Transistor Count	150 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Power Supply	GND = 0 V		6	V
V _I	Input Voltage	GND = 0 V	V _I ≤ V _{CC}	6	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 SOIC-8	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	°C/W
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

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Table 4. LVTTTL INPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current ($V_{in} = 2.7\text{ V}$)			20	μA
I_{IHH}	Input HIGH Current MAX ($V_{in} = 6.0\text{ V}$)			100	μA
I_{IL}	Input LOW Current ($V_{in} = 0.5\text{ V}$)			-0.6	mA
V_{IK}	Input Clamp Voltage ($I_{in} = -18\text{ mA}$)			-1.2	V
V_{IH}	Input HIGH Voltage	2.0			V
V_{IL}	Input LOW Voltage			0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. 10EPT PECL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $GND = 0\text{ V}$ (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Positive Power Supply Current "HIGH"	18	23	28	18	23	28	19	24	29	mA
V_{OH}	Output HIGH Voltage (Note 3)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 3)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Output parameters vary 1:1 with V_{CC} .
3. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

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Table 6. 100EPT PECL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $GND = 0\text{ V}$ (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Negative Power Supply Current	20	25	30	22	27	32	23	28	33	mA
V_{OH}	Output HIGH Voltage (Note 5)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 5)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Output parameters vary 1:1 with V_{CC} .
5. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

Table 7. AC CHARACTERISTICS $V_{CC} = 3.0\text{ V}$ to 3.6 V , $GND = 0\text{ V}$ (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Input Clock Frequency		> 1			> 1			> 1		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential	280	350	430	300	370	450	320	400	490	ps
t_{SKEW}	Device-to-Device Skew (Note 7)			150			150			170	ps
t_{JITTER}	RMS Random Clock Jitter		< 1	< 2		< 1	< 2		< 1	< 2	ps
t_r , t_f	Output Rise/Fall Times (20% – 80%)	70	100	170	80	120	180	90	140	190	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Measured using a LVTTTL source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
7. Skew is measured between outputs under identical transitions.

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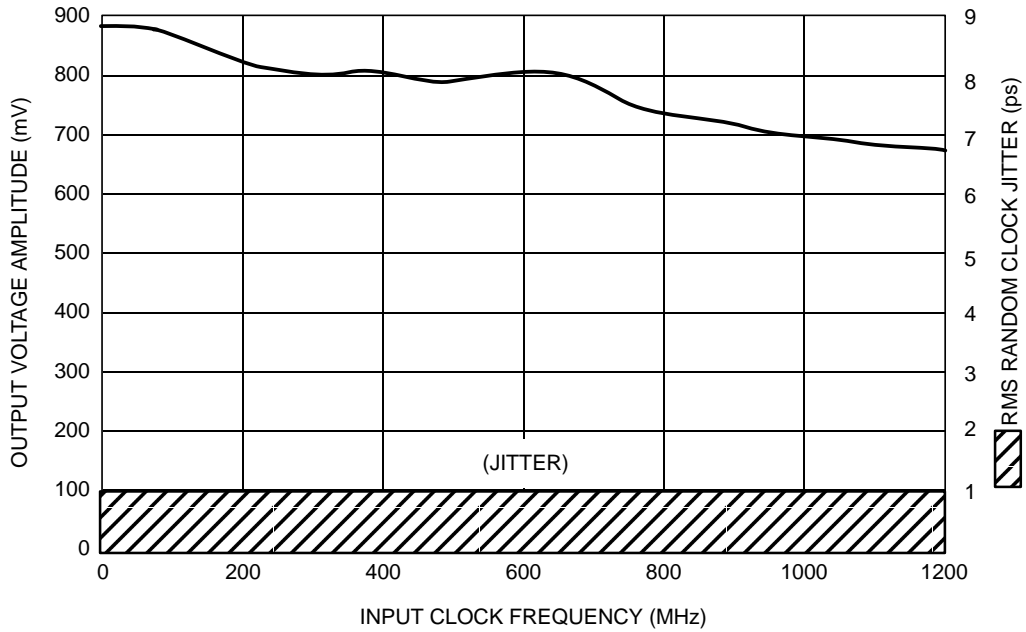


Figure 2. Output Voltage Amplitude (V_{OUTpp})/RMS Jitter vs. Input Clock Frequency at Ambient Temperature

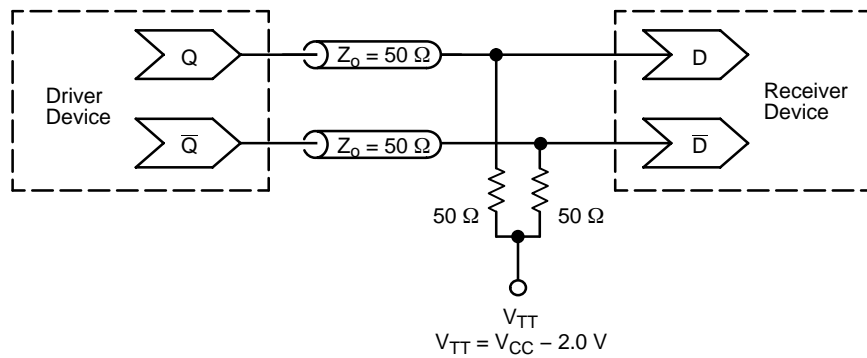


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

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ORDERING INFORMATION

Device	Package	Shipping†
MC10EPT20D	SO-8	98 Units / Rail
MC10EPT20DR2	SO-8	2500 / Tape & Reel
MC10EPT20DT	TSSOP-8	100 Units / Rail
MC10EPT20DTR2	TSSOP-8	2500 / Tape & Reel
MC100EPT20D	SO-8	98 Units / Rail
MC100EPT20DG	SO-8 (Pb-Free)	98 Units / Rail
MC100EPT20DR2	SO-8	2500 / Tape & Reel
MC100EPT20DT	TSSOP-8	100 Units / Rail
MC100EPT20DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100EPT20DTR2	TSSOP-8	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

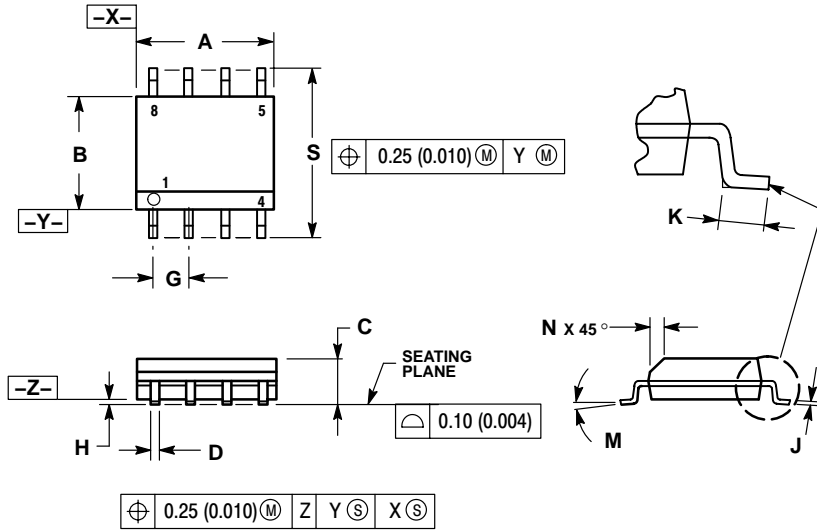
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1642/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

SOIC-8 NB
D SUFFIX
CASE 751-07
ISSUE AC

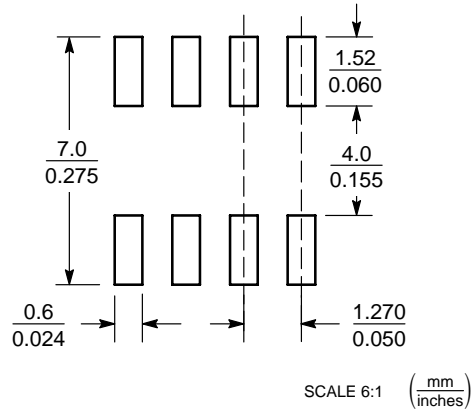


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

