

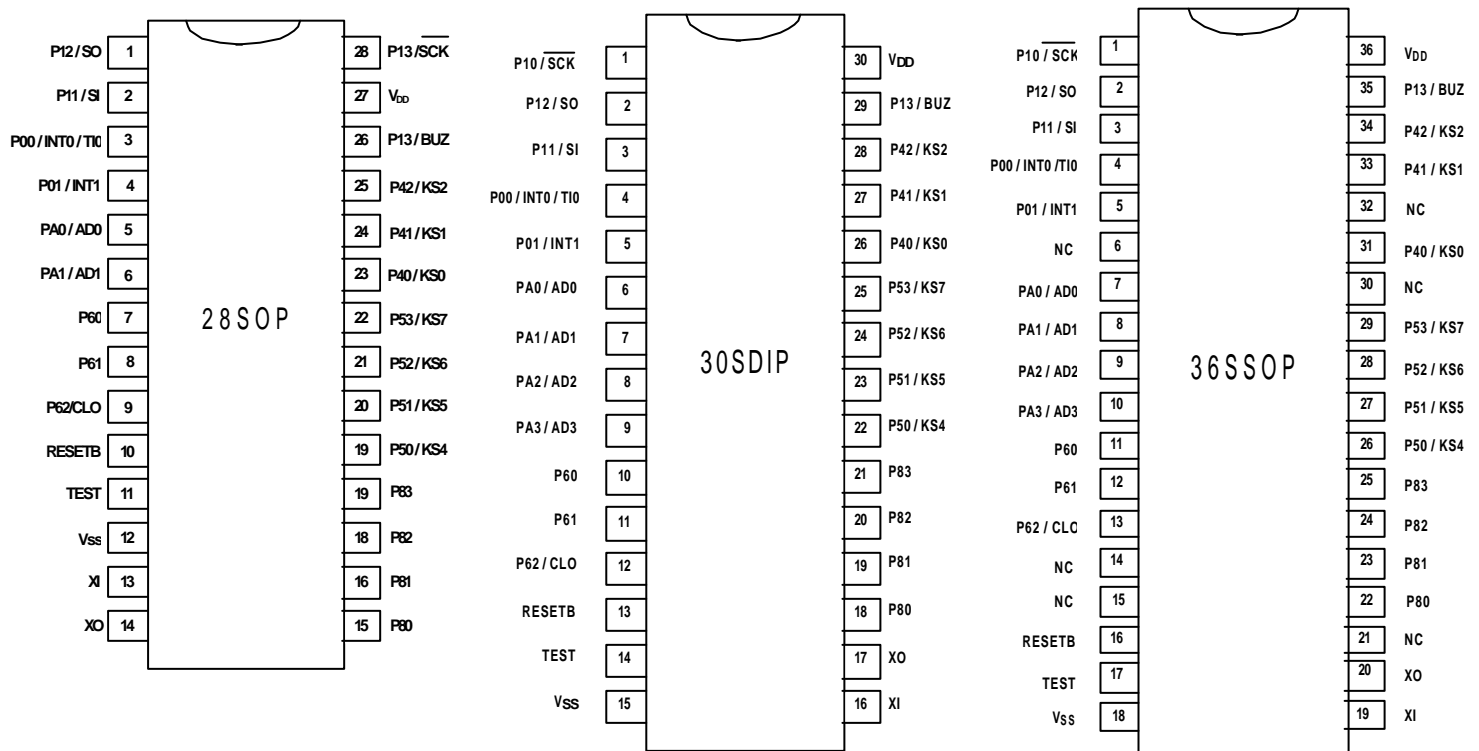
Description

The SD42C4404(4302) is a 4-bit single chip micro-computer having 4K(2K) bytes ROM and is designed with CMOS silicon gate technology. The SD42C4404 includes such peripherals as various timers, A/D converter, serial communication interface, on-chip oscillator and clock circuitry. The high performance CPU and internal peripherals allow flexible & cost effective system design in industrial and home appliances. And the OTP device (42P4404) can shorten system development periods and help the process for software debugging.

Ordering Information

Type NO.	Marking	Package Code.
SD42C4404	SD42C4404	28SOP/30SDIP/36SSOP

Pin Configuration



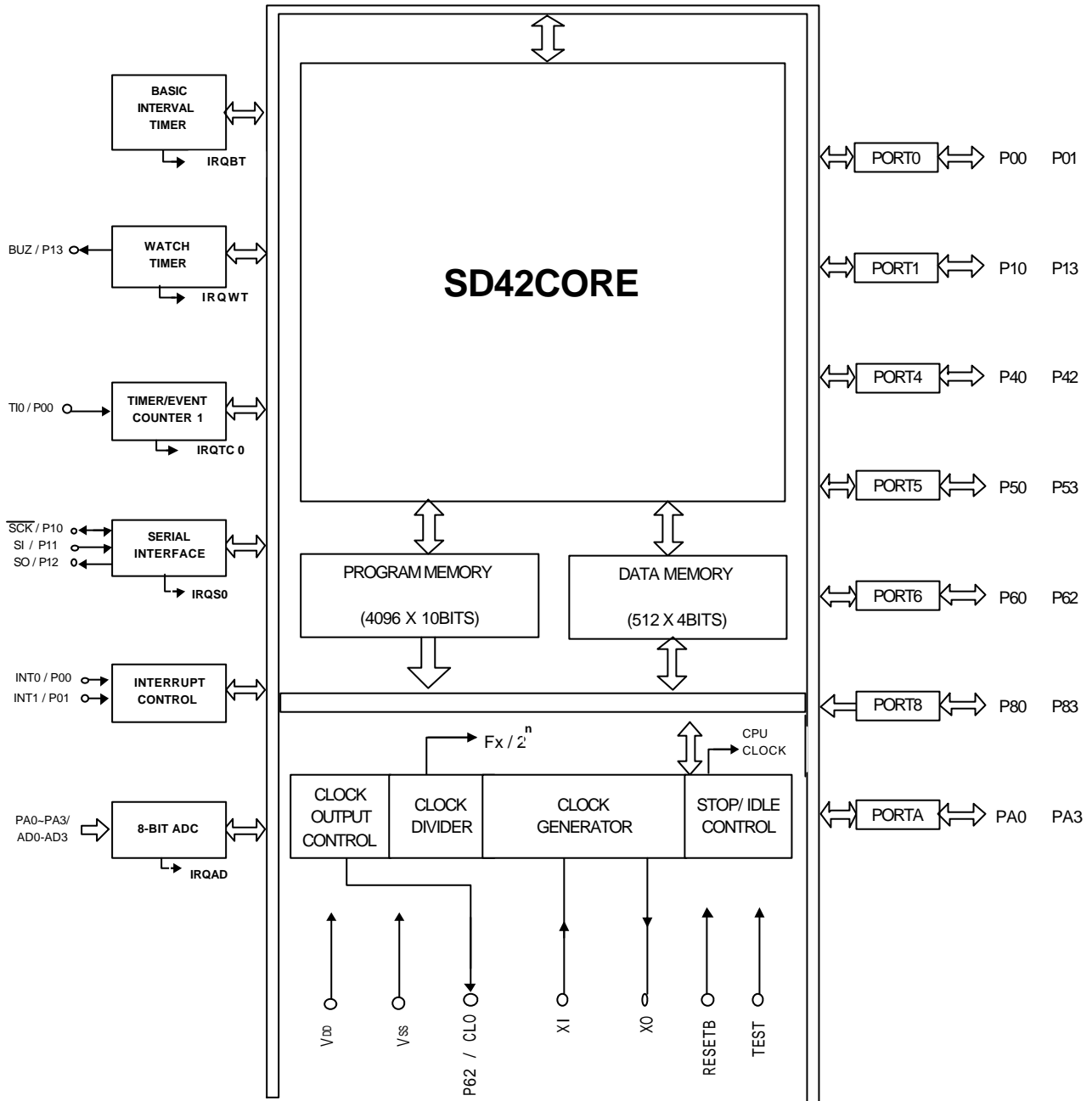
Features

- Memory mapped I/O
- Program memory : 4096 x 10bits (DMC42C4404)
2048 x 10bits (DMC42C4302)
- Data memory : 512 x 4bits (DMC42C4404)
256 x 4bits (DMC42C4302)
- Instructions
 - Various bit manipulation
 - 8-bit data operation
 - 7-bit relative branch
 - 1 byte absolute call
- Instruction cycle times ($XI = 4.19\text{MHz}$)
 - 15.3 us ($XI/64 = 65.5\text{KHz}$)
 - 1.91 us ($XI/8 = 524.0\text{KHz}$)
 - 0.95 us ($XI/4 = 1.05\text{MHz}$)
- 4 Register Bank
- General register : 8 x 4-bit respectively
- Accumulator
 - Bit Accumulator (CY), 4 bit Accumulator (A),
8 bit Accumulator (XA)
- Multiple vectored interrupt source
 - External interrupt : 3
 - Internal interrupt : 4
- Watch timer (at 4.19MHz)
 - fast mode : 3.91 msec
 - normal mode : 0.5 sec
 - buzzer output : 1, 2, 4 KHz
- Basic interval timer
 - 8 kinds of period
 - Used stabilization wait timer to wake up Stop mode
- One 8-bit timer / event counter
- Key scan
 - 7 channels
- 8-bit serial communication interface
 - External / Internal clock selection
 - Mode : Transmit, Receive
Receive only
Clock continuous
- 8-bit A/D converter
 - 8-bit successive approximate type
 - 4 channels
 - Sample and hold
 - Conversion time : 17.1us at 4.19MHz
- 24 I/O Pins
 - CMOS Pins : 16
 - High current LED direct drive pins
 - Internal pull-up resistor (Mask option)
 - Internal pull-down resistor (Mask option)
- Power saving mode
 - STOP : Main clock, CPU clock stop
 - STBY : Only CPU clock stop
Main clock operation
- Operating voltage range
 - $V_{DD} = 2.5 \sim 5V \pm 10\%$
- Operating temperature range
 - $T_A = -40$ to $+85$

APPLICATION

Telephone, General

BLOCK DIAGRAM



Program Memory (ROM)

	CONTENTS
0000H	VECTOR ADDRESS AREA
001FH 0020H	ZERO-PAGE CALL AREA
005FH 0060H	4K Byte
0FFFH	

Vector Address

	Prioty	INTERRUPT SUORCE	
0000H	0	RESET	Reset Signal
0002H	1	IRQBT	Basic Interval Timer
0004H	2	IRQ0	External interrupt 0
0006H	3	IRQ1	External interrupt 1
0008H			
000AH	5	IRQTC1	Timer Event Counter 1
000CH			
000EH			
0010H			
0012H	9	IRQS0	Serial I/O 0
0014H	10	IRQAD	8 bit ADC
0016H			
0018H	12	IRQWT	Watch Timer
001AH	13	IRQKS	Key Scan
001CH			
001EH	15	-	reserved

Data Memory (RAM)

		DIRECT	INDIRECT		STACK	GENERAL REGISTER	
		m	@HL	@DE @DL		RB=0 RB=2	RB=1 RB=4
BANK 0 (1K)	\$00 PAGE0 (256 Byte)	MB=0	MB=0	MP=0	SPS=0		
	\$FF PAGE1 (256 Byte)			MP=1			
	\$FF PAGE2 (256 Byte)			MP=2	SPS=1		
	\$FF PAGE3 (256 Byte)	I/O MEMORY		MP=3	SPS=2		
	\$FF						

; Usable

I/O Address Map

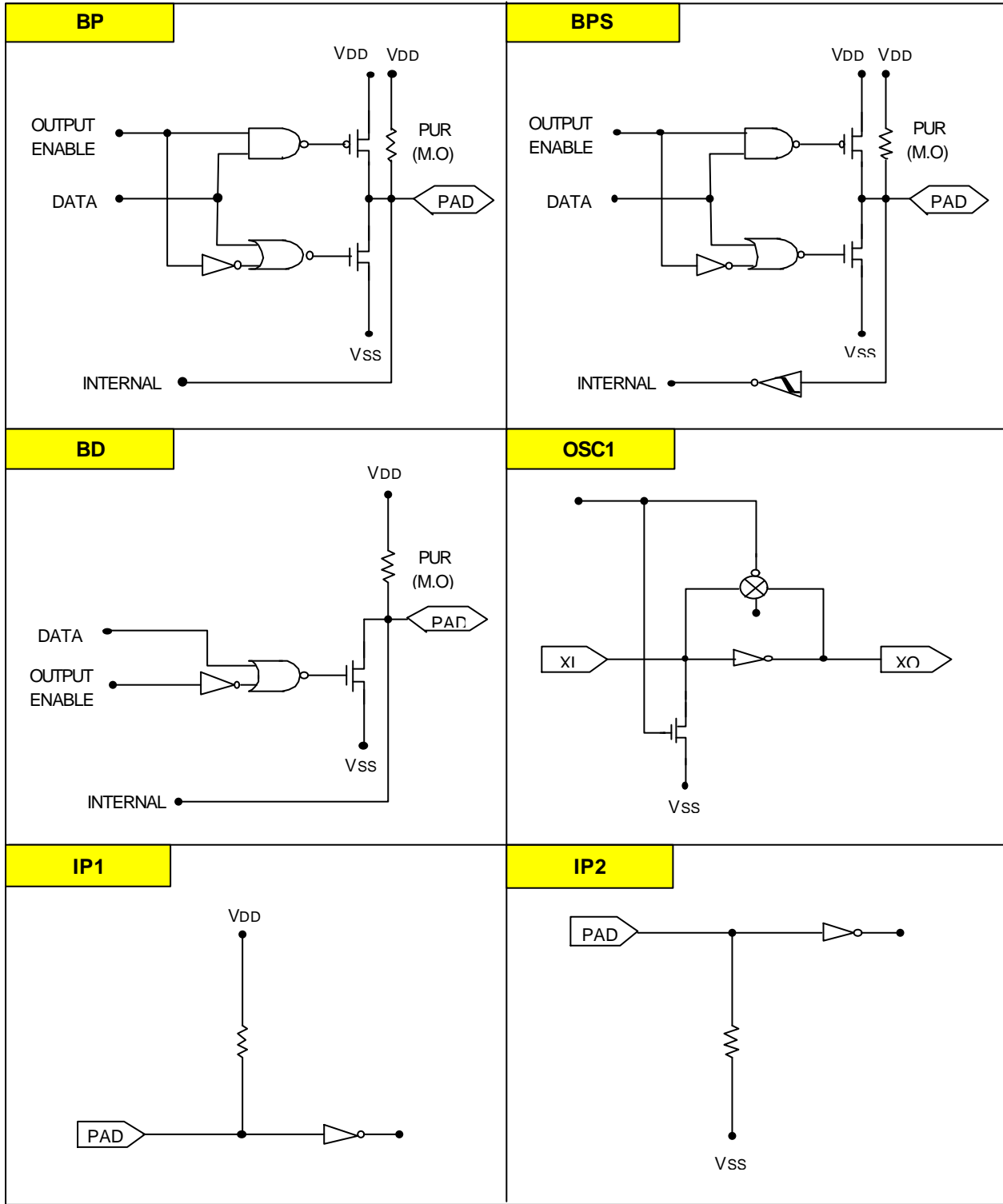
ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL VALUE
	b3	b2	b1	b0		1 bit	4 bit	8bit		
318H	Stack pointer low (SPL)				R/W			O	Stack pointer low	E
319H	Stack pointer high (SPH)				R/W			O	stack pointer high	F
31AH	SP3	SP2	SP1	SP0	R/W			O	Stack Page Select Low (SPSL)	0
31BH	-	-	SP5	SP4	R/W			O	Stack Page Select High (SPSh)	0
31CH	AC		IS1	IS0	R/W	O	O	O	Psw low (PSWL)	0
31DH	CY	Z	OV	T					Psw high (PSWH)	0
326H	T/E counter mode register 1				W	326H.3			clock source select. counter start (ch1)	00
327H	(TMOD1)									
328H	T/E counter register 1				R				readable count value (ch1)	00
329H	(TMCNT1)									
32AH	T/E reference register 1				W				count reference register (ch1)	FF
32BH	(TMREF1)									
332H	Basic Timer mode register(BMOD)				R/W	332H.3			clock select, Bit start	0
334H	Basic interval timer count				R				readable count register	00
335H	register(BITCNT)									
336H	Watch timer mode register				R/W	336H.3			clock/buzzer select. bit3	00
337H	(WMOD)									
386H	Adc8 mode register (ADCM8)				R/W	386H.3		O	analog input pin select. start & low 4bit readable	00
387H										
388H	Adc8 output latch (ADCOL8)				R			O	8bit conversion data	00
389H										
3A0H	Power control register (PCON)				R/W			O	system clock select, idle, stop mode	00
3A2H	Operating mode register (SCMOD)				R/W	O			main/sub system clock select	0
3A4H	Clock output mode register (CLOMD)				W			O	cpu clock output select, clock out ENDIS	00
3A8H	Serial interface mode register0				W	3A8H.3		O	receive/transmit mode. clock select	00
3A9H	(SIOM0)									
3AAH	Serial interface buffer0				R/W				serial shift register 0	XX
3ABH	(SBUFF0)									
3B2H	Power on flag (PONF)				P/W	3B2H.0		O	power on reset flag	0
3C3H	IPSR3	IPSR2	IPSR1	IPSR0						
3C4H	External interrupt mode register0 (IMOD0)				W			O	external interrupt 0 edge detection	00
3C5H	External interrupt mode register1 (IMOD1)				W			O	external interrupt 1 edge detection	00
3D8H			IEBT	IRQBT	R/W	O	O		Interrupt EN/IRQ flag	0
3D9H	IEAD8	IRQAD8	IEWT	IRQWT	R/W	O	O		Interrupt EN/IRQ flag	0
3DAH			IES0	IRQS0	R/W	O	O		Interrupt EN/IRQ flag	0
3DBH	IE1	IRQC1			R/W	O	O		Interrupt EN/IRQ flag	0
3DCH	IE1	IRQ1	IE0	IRQ0	R/W	O	O		Interrupt EN/IRQ flag	0

ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL VALUE
	b3	b2	b1	b0		1 bit	4 bit	8bit		
3DDH	IETC2	IRQTC2			R/W	0	0		Interrupt EN/IRQ flag	0
3DEH					R/W	0	0		Interrupt EN/IRQ flag	0
3E0H	PW03	PW02	PW01	PW00	W			0	port 0, 1 mode register (PMGA)	00
3E1H	PW13	PW12	PW11	PW10						
3E4H	PW43	PW42	PW41	PW40	W			0	port 4, 5 mode register (PMGC)	00
3E5H	PW53	PW52	PW51	PW50						
3E6H	PW63	PW62	PW61	PW60	W			0	port 6, 7 mode register (PMGD)	00
3E7H	PW73	PW72	PW71	PW70						
3E8H	PW83	PW82	PW81	PW80	W			0	port 8, 9 mode register (PMGE)	00
3E9H	PW93	PW92	PW91	PW90						
3EAH	PWA3	PWA2	PWA1	PWA0	W			0	port a, b mode register (PMGF)	00
3EBH	PWB3	PWB2	PWB1	PWB0						
3F0H	PORT0 (R0)				R/W	0	0		R0 Port Data Register	0
3F1H	PORT1 (R1)				R/W	0	0		R1 Port Data Register	0
3F4H	PORT4 (R4)				R/W	0	0	0	R4 Port Data Register	0
3F5H	PORT5 (R5)								R5 Port Data Register	0
3F6H	PORT6 (R6)				R/W	0	0		R6 Port Data Register	0
3F8H	PORT8 (R8)				R/W	0	0		R8 Port Data Register	0
3FAH	PORTA (RA)				R/W	0	0		RA Port Data Register	0

Pin Description

PIN SYMBOL	SHARED PIN	I/O	FUNCTION	RESET	PORT TYPE		
P00	INT0/TI0		4-BIT I/O PORT	INPUT	BPS		
P01	INT1	I/O	PORT 0				
P10	SCK	I/O	4-BIT I/O PORT		PORT 1	BPS	
P11	SI						
P12	SO						
P13	BUZ						
P4	-						
P5	-	PORT5					
P6	-	PORT6					
P8	-	PORT8					
PA	AD0~AD3	PORTA					
INT0/TI0	P00	I	External interrupt input port rising/falling edge detection Event pulse input port for the timer/event counters		BPS		
INT1	P01						
SCK	P10	I/O	Serial clock in/out port		BPS		
SI	P11	I	Serial data input port				
SO	P12	O	Serial data output port				
BUZ	P13	O	Buzzer output port				
Key Scan	P4-P5	I	Key scan input				
AD0~AD3	PA	I	Analog input for the 8-bit A/D converter			BP	
XI	-	I	XI, XO are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.			OSC1	
XO		O					
RESETB	-	I	Reset input pin	IP1			
TEST	-	I	Normally connect to V _{SS}	IP2			
V _{DD} , V _{SS}	-		Power & ground				

I/O Circuits



NOTE) PUR : Pull-Up Resistor
 M.O : Mask Option

Absolute Maximum Ratings

(TA = 0 to 70 , VDD = 5V ±10%, fX = 4.19MHz)

PARAMETER	SYMBOL	CONDITION	RATING		UNIT
Supply Voltage	VDD	-	-0.3 to +7.0		V
Input Voltage	VI	All I/O ports	-0.3 to VDD+0.3		V
Output Voltage	VO	-	-0.3 to VDD+0.3		V
Output Current High	IOH	One I/O port active	-15		mA
		All I/O ports active	-30		
Output Current Low	IOL	One I/O port active	Peak Value	+30	mA
		-	RMS Value	+15	
		Total value for ports P0, P1, P4, P5, P6, P8, PA	Peak Value	+100	
			RMS Value	+60	
Operating Temperature	TA	-	-40 to +85		
Storage Temperature	Tstg	-	-55 to +125		

* RMS values are calculated as peak value x $\sqrt{\text{Duty}}$

* Exceeding beyond those listed values under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Electrical Characteristics

(VSS = 0, VDD = 5V ±10%, TA = 25 °C, fX = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION		LIMIT			UNIT	
				MIN.	TYP.	MAX.		
High Level Input Voltage	VIH1	Port 0,1 (Schmitt Input)		0.8 VDD	-	VDD	V	
	VIH2	XI		VDD - 0.5	-	VDD		
	VIH3	Port 4,5,6,8,A RESETB, TEST		0.7 VDD	-	VDD		
Low Level Input Voltage	VIL1	Port 0,1 (Schmitt Input)		0	-	0.2 VDD	V	
	VIL2	XI		0	-	0.4		
	VIL3	Port 4,5,6,8,A RESETB, TEST		0	-	0.3 VDD		
High Level Output Voltage	VOH	Port 0,1,6,A	(IOH = - 5mA)	4.2	4.5	-	V	
		Port 0,1,6,A	(IOH = - 100uA)	4.6	4.9	-		
Low Level Output Voltage	VOL	Port 4, 5 (Open-Drain)	(IOL = 10mA)	-	-	2	V	
		Port 0,1,6,A	(IOL = 10mA)	-	0.4	0.6		
		Port 0,1,6,A	(IOL = 1mA)	-	0.1	0.3		
High Level Input Leakage Current	IIH	Port 0,1,4,5,6,8,A VPPOEX, RESETB		-	1.2	3	uA	
		XI		-	5	15		
Low Level Input Leakage Current	IIL	Port 0,1,4,5,6,8,A VPPOEX, TEST		-	-1.2	-3	uA	
		XI		-	-5	-15		
Supply Current	IDD1	Main Clock (XI) = 4.19MHz	Dynamic Mode	VDD = 5V ±10%	-	-	10	mA
			Idle Mode		-	-	5	

DC Electrical Characteristics

(V_{SS} = 0, V_{DD} = 5V ±10%, T_A = 25 °C, f_κ = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION		LIMIT			UNIT	
				MIN.	TYP.	MAX.		
Supply Current	IDD2	Main Clock (XI) = 2MHz	Dynamic Mode	V _{DD} = 3V ±10%	-	-	2	mA
			Idle Mode		-	-	1	
	IDD5	Main Clock (XI) = 4.19MHz	Stop Mode	V _{DD} = 5V ±10%	-	1	5	uA
				V _{DD} = 3V ±10%	-	0.5	3	
Pull-up Resistor	RL1	V _I = 0V, V _{DD} = 5V ±10% RESETB		20	-	60	Kohm	
Pull-down Resistor	RL2	V _I = 0V, V _{DD} = 5V ±10% TEST		10	-	30		

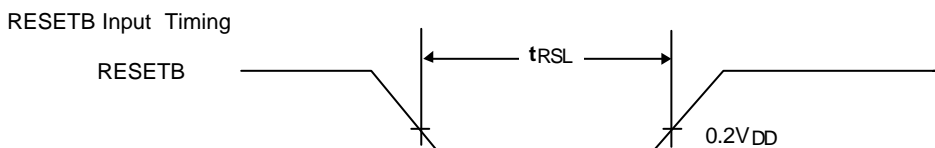
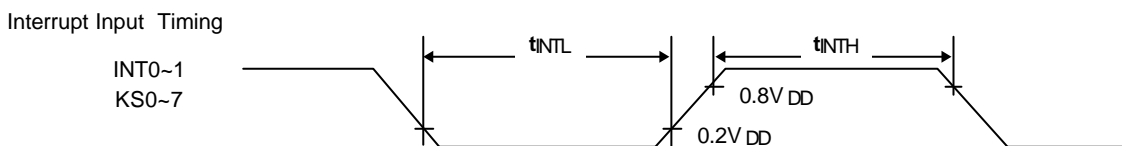
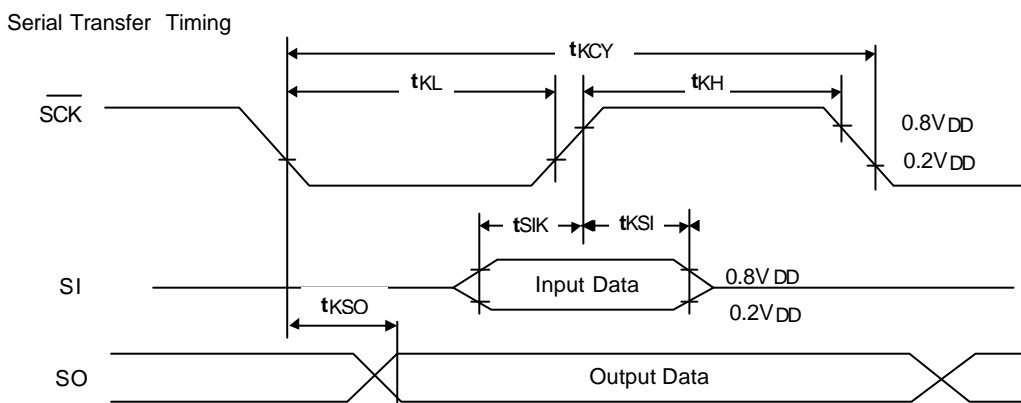
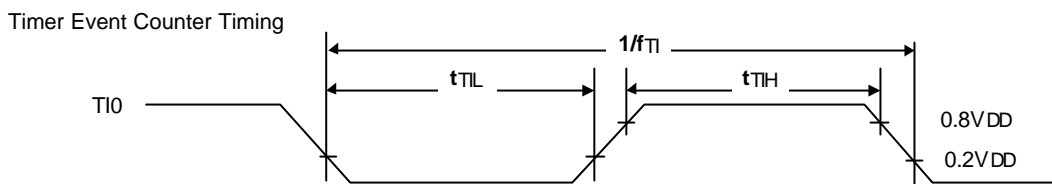
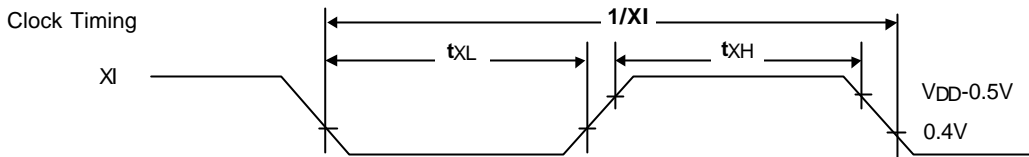
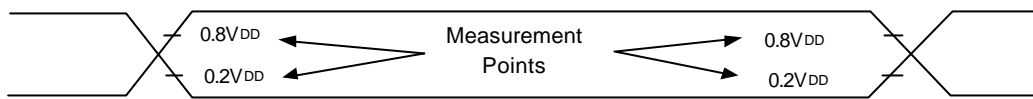
AC Electrical Characteristics

(T_A = -40 to +85 , V_{DD} = 2.7 to 6.0V)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Cycle Time	t _{cy}	Main system clock	V _{DD} = 4.5 to 6.0V	0.95	-	64	uS
			V _{DD} = 2.7 to 3.3V	3.8	-	64	uS
TIO Input Frequency	f _{TI}	V _{DD} = 4.5 to 6.0V		0	-	1	MHz
		V _{DD} = 2.7 to 3.3V		0	-	275	KHz
TIO Input High, Low Level Width	t _{TIH}	V _{DD} = 4.5 to 6.0V		0.48	-	-	uS
	t _{TIL}	V _{DD} = 2.7 to 3.3V		1.8	-	-	uS
Interrupt Input High, Low Level Width		INT0		(1)	-	-	uS
	t _{INTH}	INT1		10	-	-	uS
	t _{INTL}	KS0 to 7		10	-	-	uS
SCK Cycle Time	t _{KCY}	V _{DD} = 4.5 to 6.0V	Input	800	-	-	nS
			Output	1600	-	-	nS
		V _{DD} = 2.7 to 3.3V	Input	3200	-	-	nS
			Output	3800	-	-	nS
SCK High, Low Level Width	t _{KH}	V _{DD} = 4.5 to 6.0V	Input	400	-	-	nS
			Output	t _{KCY/2-50}	-	-	nS
	t _{KL}	V _{DD} = 2.7 to 3.3V	Input	1600	-	-	nS
			Output	t _{KCY/2-150}	-	-	nS
SI Set up Time to SCK High	t _{SIK}		Input	100	-	-	nS
			Output	150	-	-	nS
SI Hold Time to SCK High	t _{KSI}		Input	400	-	-	nS
			Output	400	-	-	nS
SCK to S0 Output Delay Time	t _{KSO}	V _{DD} = 4.5 to 6.0V	Input	-	-	300	nS
			Output	-	-	250	nS
		V _{DD} = 2.7 to 3.3V	Input	-	-	1000	nS
			Output	-	-	1000	nS
RESETB Low Level	t _{RSL}			10	-	-	uS

(1) 2t_{cy} or 128/f_x, depending on the setting of the interrupt mode register.

AC Timing Measurement Points (Except XI)



RAM Data Retention Characteristics (in STOP Mode)

(TA = -40 to +85)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	VDDDR		2.0	-	6.0	V
Data Retention Supply Current	IDDDR	VDDDR = 2.0V	-	0.1	10	uA
Release Signal Set Time	tSREL		0	-	-	uS
Oscillation Stabilization Wait Time	tWAIT	When released by RESETB	-	2 ¹⁷ /fx	-	mS
		When released by interrupt Signal	-	NOTE 1)	-	mS

NOTE 1) Depends on the setting of the basic interval timer mode register.

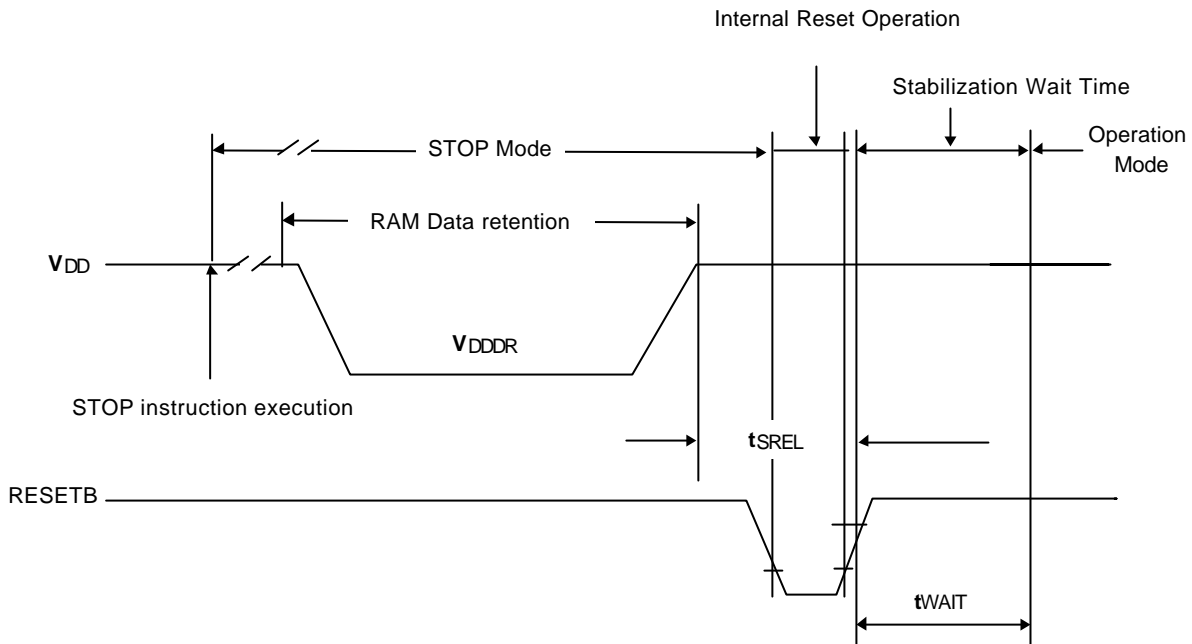
(refer to the table below)

(fx = 4.19MHz)

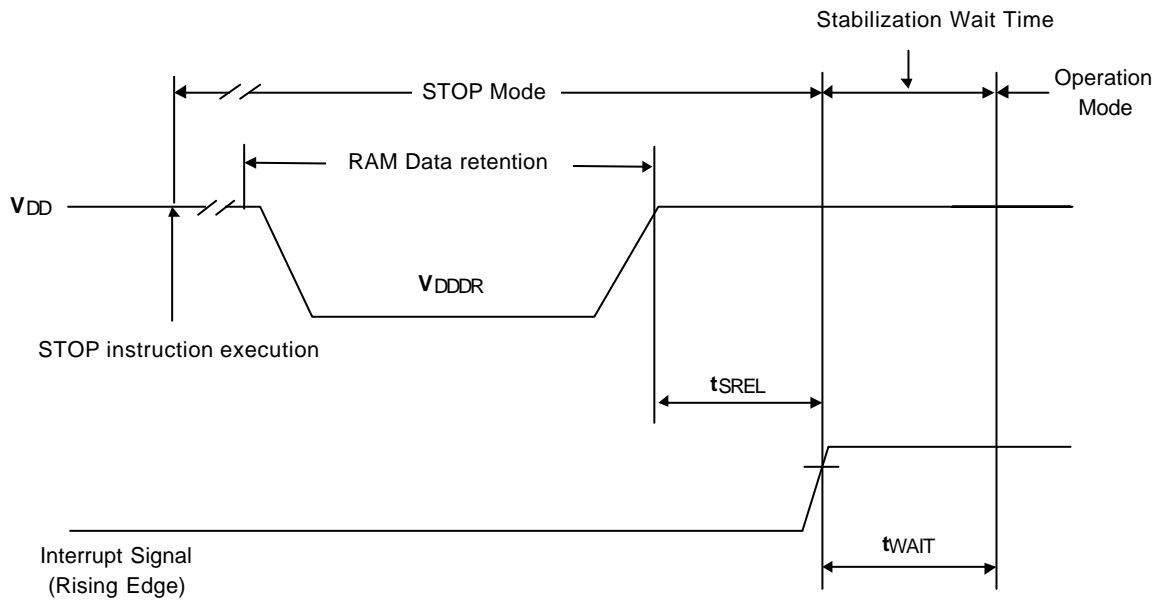
BMOD2	BMOD1	BMOD0	Oscillation Stabilization
0	0	0	2 ²⁰ /fx (Approximately 250ms)
0	1	1	2 ¹⁷ /fx (Approximately 31.3ms)
1	0	0	2 ¹⁵ /fx (Approximately 7.82ms)
1	0	1	2 ¹³ /fx (Approximately 1.95ms)

RAM Data Retention Timing

When STOP mode is released by RESETB input



When STOP mode is released by interrupt signal



SD42P4404

Description

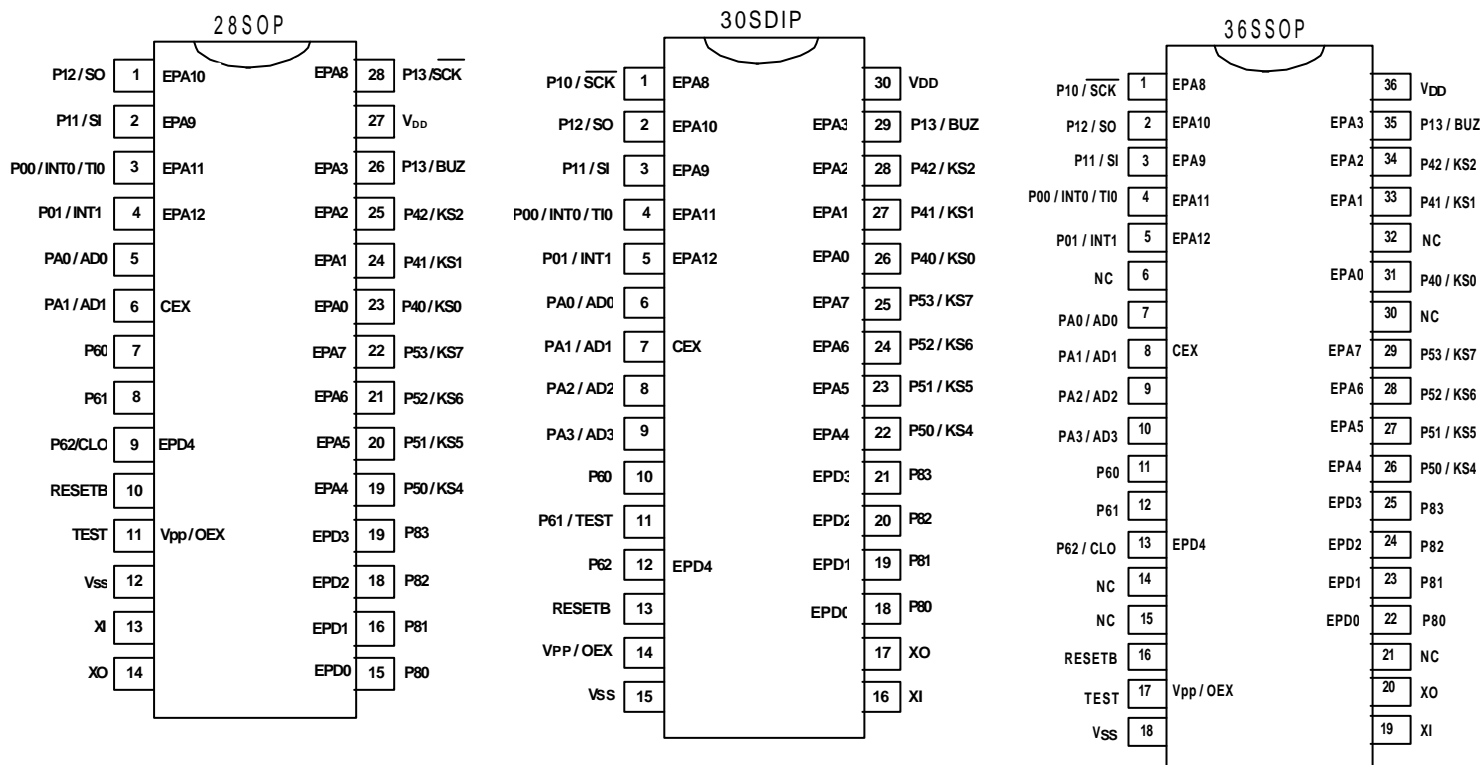
The SD42P4404 is a system evaluation LSI having a built in One-time PROM for SD42C4404. A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket. The function of this device is exactly same as the SD42C4404 by programming to the internal PROM.

The SD42P4404 is OTP version of the SD42C4404 which internal ROM has been changed from MASK ROM to EPROM.

Ordering Information

Type NO.	Marking	Package Code.
SD42P4404	SD42P4404	28SOP/30SDIP/36SSOP

Pin Configuration



Device Operation

The operational modes of the SD42P4404 are listed in Table 1.

A single 5V power supply is required in the read mode.

All inputs are TTL levels except for V_{PP} / \overline{OEX} .

$$V_{PP} = 12.5 \pm 0.5V$$

MODE \ PINS	\overline{CEX}	V_{PP} / \overline{OEX}	V_{DD}	OUTPUT
READ	V_{IL}	V_{IL}	5.0V	D _{OUT}
PROGRAM	V_{IL}	V_{PP}	6.0V	D _{IN}
VERIFY	V_{IL}	V_{IL}	6.0V	D _{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	6.0V	High Z

TABLE 1. Operating Modes

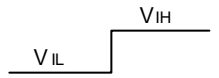
PIN NAME	MODE	
	EPROM MODE	USER MODE
TEST	V_{IL}	V_{IH}
RESETB	V_{IL}	

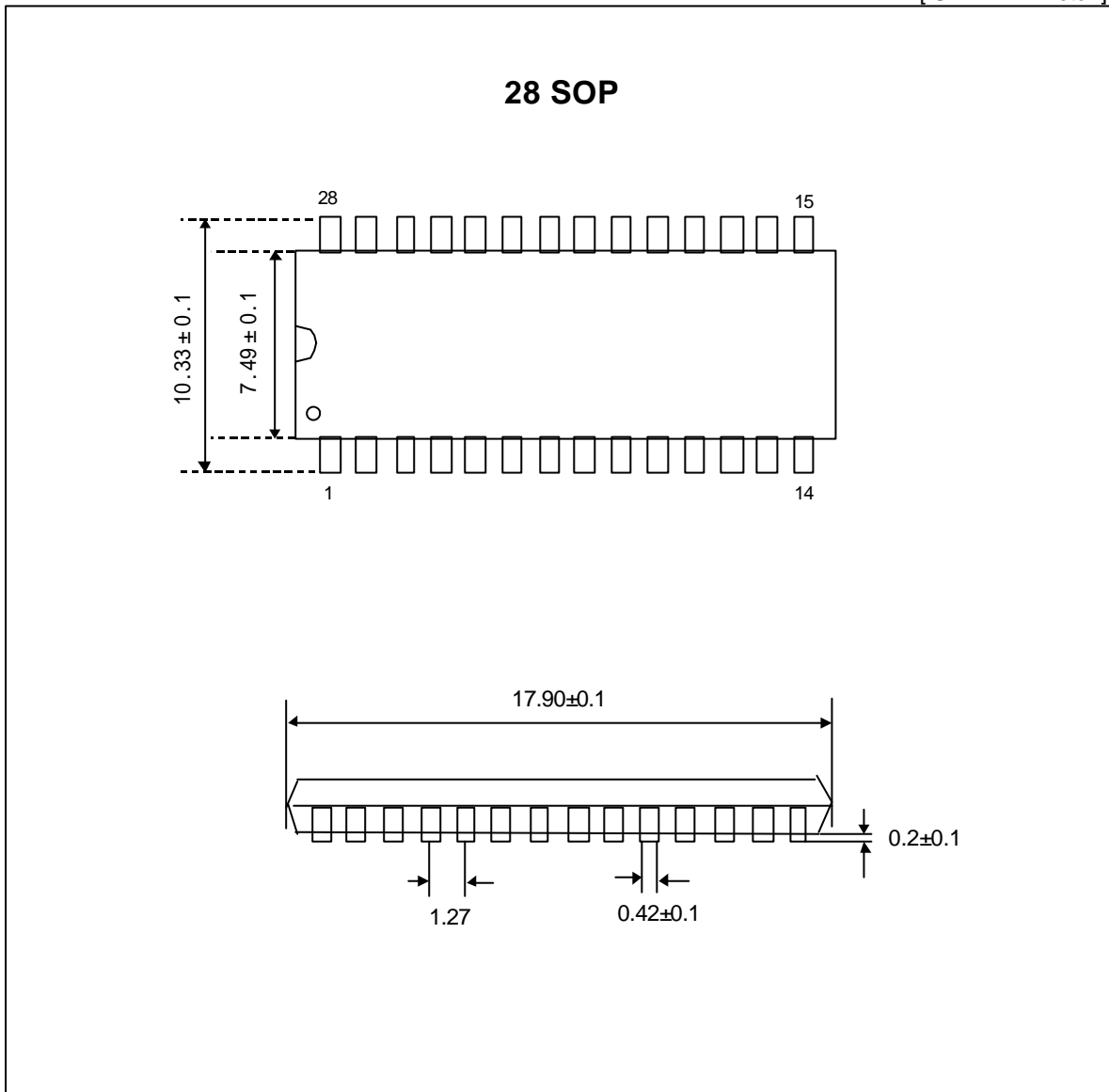
TABLE 2. The modes of SD42P4404

DC Programming Characteristics

PARAMETER	SYMBOL	TEST CONDITION	LIMIT		UNIT
			MIN.	MAX.	
Input Low Voltage	V_{IL}		-0.1	0.8	V
Input High Voltage	V_{IH}		2.0	V_{DD}	V
Output Low Voltage during Verify	V_{OL}	$I_{OL} = 2.1mA$	-	0.45	V
Output High Voltage during Verify	V_{OH}	$I_{OH} = -400\mu A$	2.4	-	V
Quick-pulse Programming	V_{PP}		12.5	13.0	V
Quick-pulse Programming	V_{DD}		6.0	6.5	V

Package Dimension

[UNIT : Millimeter]



Package Dimension

[UNIT : Millimeter]

