DRAM

256K x 16 DRAM

FAST PAGE MODE T-46-23-17

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 500mW active, typical
- All device pins are fully TTL compatible
- 512 cycle refresh in 8ms (9 rows and 9 columns)
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS and HIDDEN
- Optional FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle (MT4C16257/9 only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C16258/9 only)

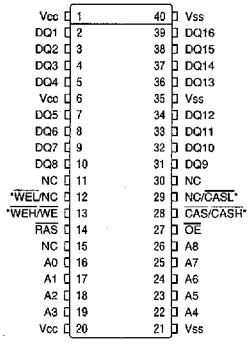
OPTIONS

	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Write Cycle Access	
BYTE or WORD via WE (non-maskable)	MT4C16256
BYTE or WORD via CAS (non-maskable)	MT4C16257
BYTE or WORD via WE (maskable)	MT4C16258
BYTE or WORD via CAS (maskable)	MT4C16259
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (475 mil)	Z

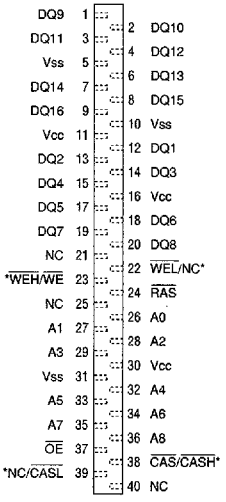
NOTE: Available in die form. Please consult factory for die data sheets.

PIN ASSIGNMENT (Top View)

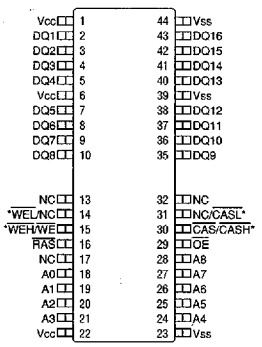
40-Pin SOJ (Q-6)



40-Pin ZIP (O-4)



40-Pin TSOP (R-5)



*MT4C16256/8 / MT4C16257/9

GENERAL DESCRIPTION

The MT4C16256/7/8/9 are randomly accessed solid-state memories containing 4,194,304 bits organized in a x16 configuration. The MT4C16256 and MT4C16258 have both BYTE WRITE and WORD WRITE access cycles via two write enable pins. The MT4C16257 and MT4C16259 have both BYTE WRITE and WORD WRITE access cycles via two CAS pins. The MT4C16258 and MT4C16259 are also able to perform WRITE-PER-BIT accesses.

The MT4C16256 and MT4C16257 function in the same manner except that WEL and WEH on MT4C16256 and CASL and CASH on MT4C16257 control the selection of byte WRITE access cycles. WEL and WEH function in an identical manner to WE in that either WEL or WEH will generate an internal WE. CASL and CASH function in an identical manner to CAS in that either CASL or CASH will generate an internal CAS.

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The MT4C16256 "$\overline{WE}$" function and timing are determined by the first $\overline{WE}$ ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C16257 "$\overline{CAS}$" function and timing are determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$)to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. $\overline{CASL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and $\overline{CASH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through $\overline{CASL}$ or $\overline{CASH}$ in the same manner during READ cycles for the MT4C16257.

The MT4C16258 and MT4C16259 function in the same manner as MT4C16256 and MT4C16257, respectively; and they have NONPERSISTENT MASKED WRITE cycles capabilities. This option allows the MT4C16258 and MT4C16259 to operate with either normal WRITE cycles or with NONPERSISTENT MASKED WRITE cycles.

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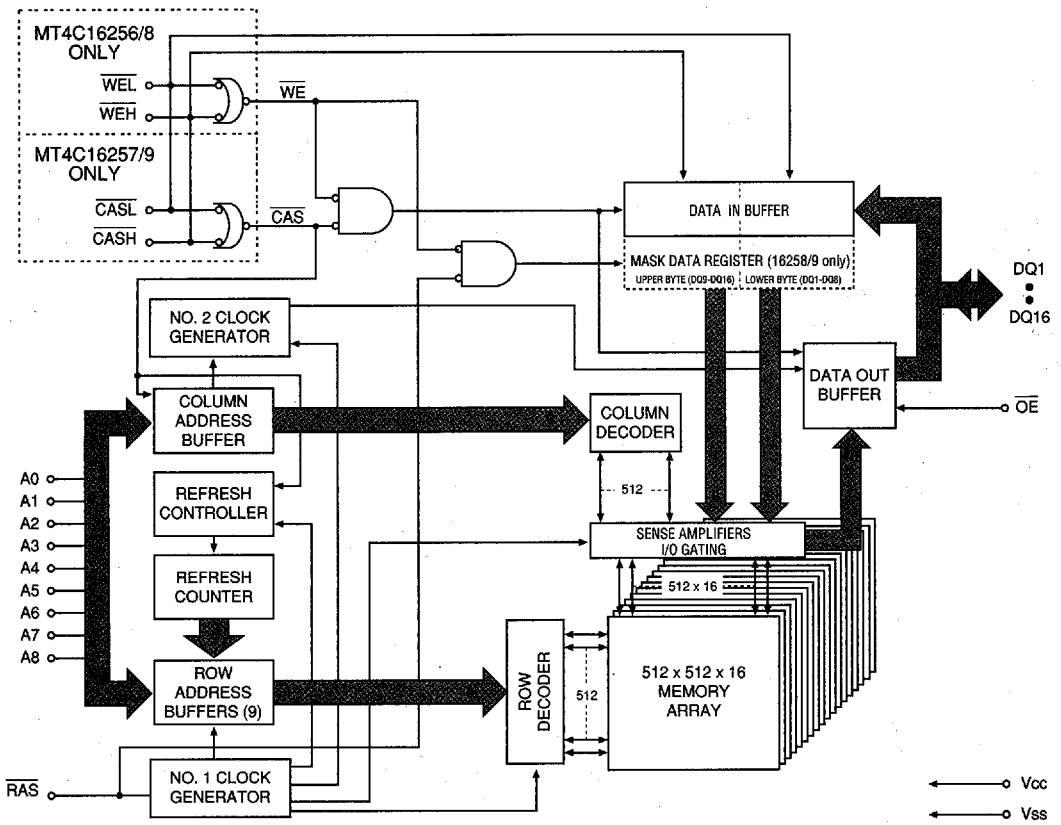
FUNCTIONAL BLOCK DIAGRAM



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PIN DESCRIPTIONS

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SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
14	16	24	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to latch in the 9 row-address bits and strobe the $\overline{WE}$ and DQs on the MASKED WRITE option (MT4C16258 and MT4C16259 only).
28	30	38	$\overline{CAS}$/ $\overline{CASH}$	Input	Column Address Strobe: $\overline{CAS}$ (MT4C16256/8) is used to latch-in the 9 column-address bits and enable the DRAM output buffers, and strobe the data inputs on WRITE cycles. $\overline{CAS}$ controls DQ1 through DQ16. Column Address Strobe Upper Byte: $\overline{CASH}$ (MT4C16257/9) is the $\overline{CAS}$ control for DQ9 through DQ16. The DQs for the byte not being accessed will remain in a High-Z (high impedance) state during either a READ or a WRITE access cycle.
27	29	37	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ (MT4C16256/8) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/9) must be LOW and $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8) or $\overline{WE}$ (MT4C16257/9) must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
13	15	23	$\overline{WEH}$/$\overline{WE}$	Input	Write Enable Upper Byte: $\overline{WEH}$ (MT4C16256/8) is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If $\overline{WE}$ or $\overline{WEH}$ is LOW, the access is a WRITE cycle. If either $\overline{WE}$ or $\overline{WEH}$ is LOW at $\overline{RAS}$ time on MT4C16258, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only). Write Enable: $\overline{WE}$ (MT4C16257/9) controls DQ1 through DQ16inputs. If $\overline{WE}$ is LOW, the access is a WRITE cycle. The MT4C16258/9 also use $\overline{WE}$ to enable the MASK register during $\overline{RAS}$ time.
12	14	22	$\overline{WEL}$/NC	Input	Write Enable Lower Byte: $\overline{WEL}$ (MT4C16256/8) is the $\overline{WE}$ control for DQ1 through DQ8 inputs. If $\overline{WEL}$ is LOW, the access is a WRITE cycle. If $\overline{WEL}$ is LOW at $\overline{RAS}$ time on MT4C16258, then it is also a MASKED WRITE cycle. The DQs for the byte not being written will remain in a High-Z state (BYTE WRITE cycle only).
29	31	39	NC/$\overline{CASL}$	Input	Column Address Strobe Low Byte: $\overline{CASL}$ (MT4C16257/9) is the $\overline{CAS}$ control for DQ1 through DQ8. The DQs for the byte not being accessed will remain in a High-Z state during either a READ or a WRITE access cycle.
16-19, 22-26	18-21, 24-28	26-29, 32-36	A0-A8	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CASL}$ / $\overline{CASH}$) to select one 16-bit word (or 8-bit byte) out of the 256K available words.

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PIN DESCRIPTIONS (continued)

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SOJ PINS	TSOP PINS	ZIP PINS	SYMBOL	TYPE	DESCRIPTION
2-5, 7-10, 31-34, 36-39	2-5, 7-10, 35-38, 40-43	12-15, 17-20, 1-4, 6-9	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ / $\overline{WEH}$ (MT4C16256/8) or $\overline{CASL}$ / $\overline{CASH}$ (MT4C16257/8) to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM Location. All sixteen I/Os are active for READ cycles (MT4C16256/8). The MT4C16257/9 allow for BYTE READ cycles.
11, 15, 30	13, 17	21, 25, 40	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 6, 20	1, 6, 22	11, 16, 30	Vcc	Supply	Power Supply: +5V ±10%
21, 35, 40	23, 39, 44	5, 10, 31	Vss	Supply	Ground

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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits.

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW. The MT4C16256 and MT4C16258 each have one $\overline{CAS}$ control while the MT4C16257 and MT4C16259 have two: $\overline{CASL}$ and $\overline{CASH}$.

The $\overline{CASL}$ and $\overline{CASH}$ inputs internally generate a $\overline{CAS}$ signal functioning in an identical manner to the single $\overline{CAS}$ input on the other 256K x 16 DRAMs. The key difference is each $\overline{CAS}$ controls its corresponding DQ tristate logic (in conjunction with $\overline{OE}$ and $\overline{WE}$). $\overline{CASL}$ controls DQ1 through DQ8, and $\overline{CASH}$ controls DQ9 through DQ16.

The MT4C16257 and MT4C16259 "$\overline{CAS}$" function is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last one to transition back HIGH. The two $\overline{CAS}$ controls give the MT4C16257 and MT4C16259 both byte READ and byte WRITE cycle capabilities.

READ or WRITE cycles on the MT4C16257 or MT4C16259 are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C16256 or MT4C16258. The MT4C16256 and MT4C16258 "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C16256 and MT4C16258) or $\overline{WE}$ (MT4C16257 and MT4C16259).

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for ROW address control.

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$. Enabling $\overline{WEL}$/$\overline{CASL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while Enabling $\overline{WEH}$ or $\overline{CASH}$ will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ or $\overline{CASL}$ and $\overline{CASH}$ selects a WORD WRITE cycle.

The MT4C16256, MT4C16257, MT4C16258 and MT4C16259 can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the $\overline{WE}$ or the $\overline{CAS}$ inputs. Figure 1 illustrates the MT4C16256 BYTE WRITE and WORD WRITE cycles and Figure 2 illustrates the MT4C16257 BYTE WRITE and WORD WRITE cycles.

The MT4C16257 also has BYTE READ and WORD READ cycles, since it uses two $\overline{CAS}$ inputs to control its byte accesses. Figure 3 illustrates the MT4C16257 BYTE READ and WORD READ cycles.

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MASKED WRITE ACCESS CYCLE (MT4C16258/9 Only)

The MASKED WRITE mode control input selects normal WRITE access or MASKED WRITE access cycles. Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C16256 and MT4C16257 do not have the MASKED WRITE cycle function.

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the following WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be either written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated (non-persistent), even if the previous cycle's mask was the same mask.

Figure 4 illustrates the MT4C16258 MASKED WRITE operation and Figure 5 illustrates the MT4C16259 MASKED WRITE operation.

T-46-23-17

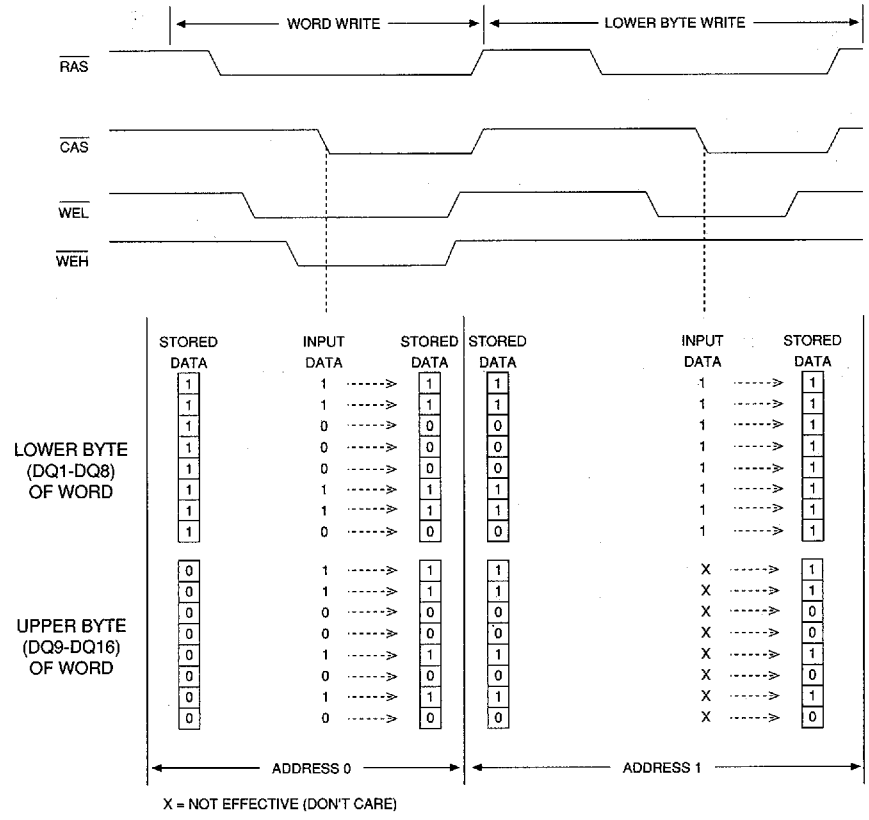

Figure 1
MT4C16256/8 WORD AND BYTE WRITE EXAMPLE

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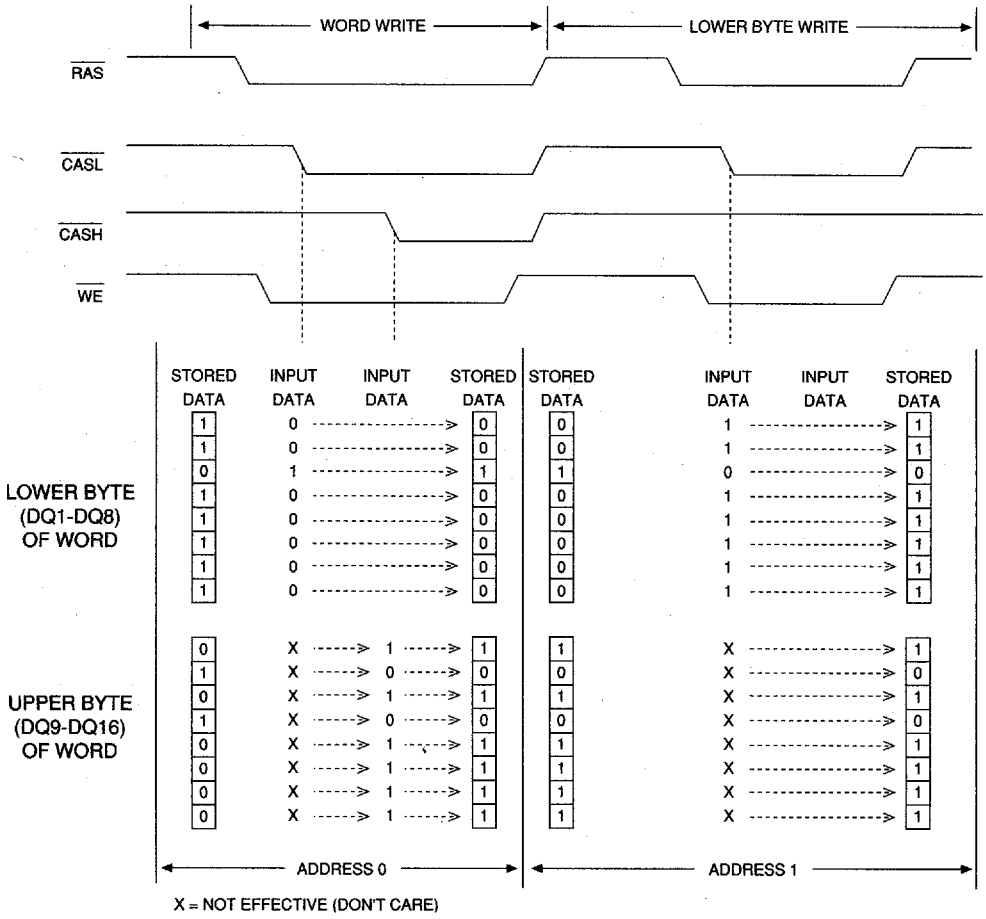

Figure 2
MT4C16257/9 WORD AND BYTE WRITE EXAMPLE

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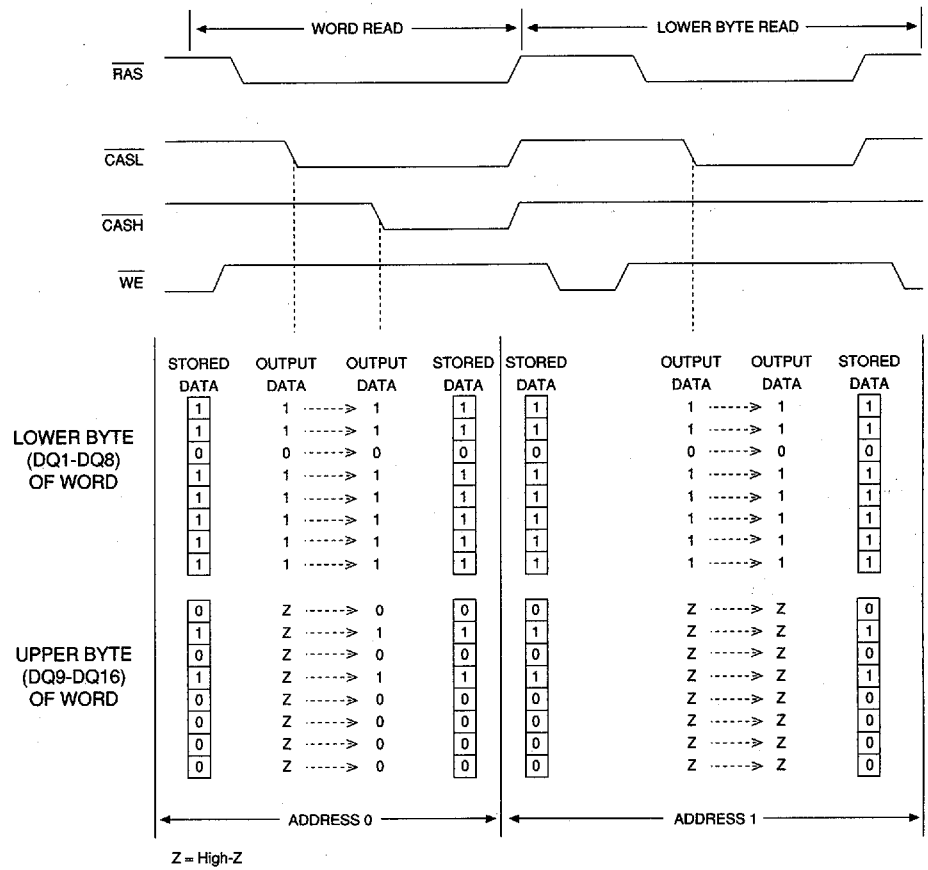

Figure 3
MT4C16257/9 WORD AND BYTE READ EXAMPLE

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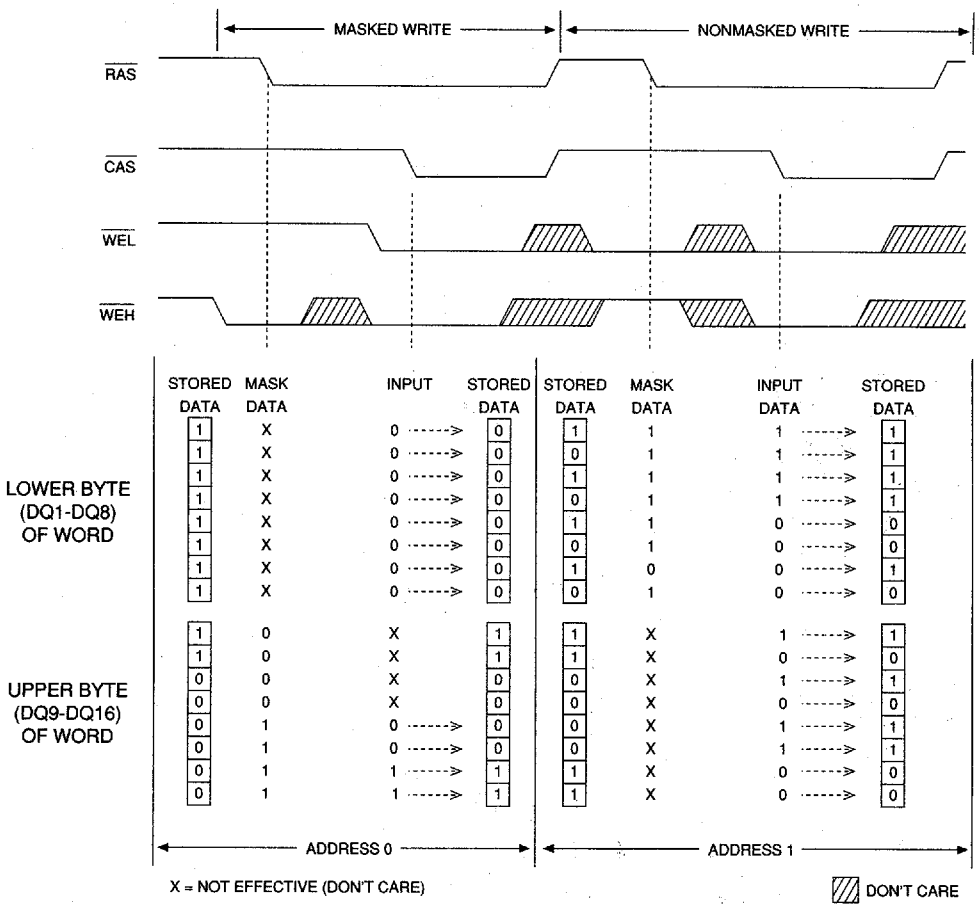

Figure 4
MT4C16258 MASKED WRITE EXAMPLE

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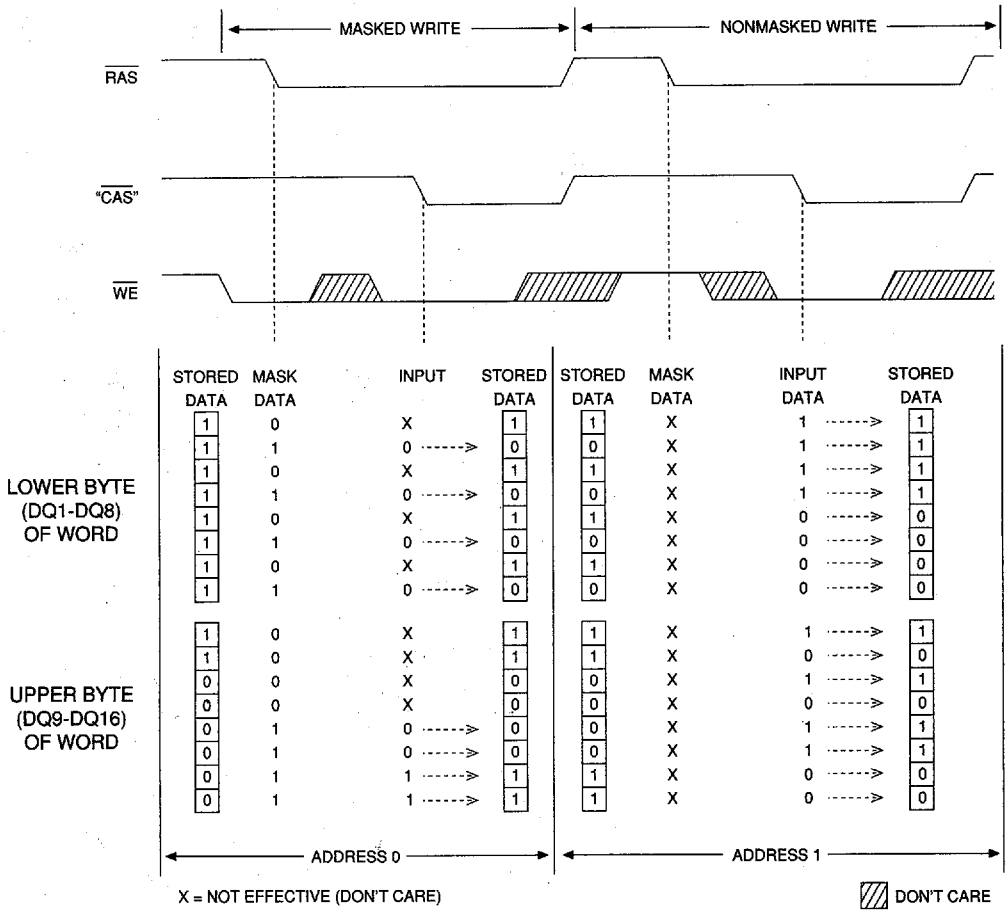

Figure 5
MT4C16259 MASKED WRITE EXAMPLE

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TRUTH TABLE: MT4C16256/8

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FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	3
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	3
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	3
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 3
PAGE-MODE READ	1st Cycle	L	H→L	H	H	L	ROW	COL	Data Out	
	2nd Cycle	L	H→L	H	H	L	n/a	COL	Data Out	
PAGE-MODE WRITE	1st Cycle	L	H→L	L	L	X	ROW	COL	Data In	1, 3
	2nd Cycle	L	H→L	L	L	X	n/a	COL	Data In	1, 3
PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data In	1, 3
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 3
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2, 3
RAS-ONLY REFRESH		L	H	H	H	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	H	H	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Data-in will be dependent on the mask provided (MT4C16258 only). Refer to Figure 4.

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TRUTH TABLE: MT4C16257/9

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FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES tR	ADDRESSES tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	5
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	5
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	5
READ-WRITE		L	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data Out	2
READ	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data Out	2
PAGE-MODE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data In	1, 5
WRITE	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data In	1, 5
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1, 2, 5
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1, 2, 5
HIDDEN	READ	L→H→L	L	L	H	L	ROW	COL	Data Out	2
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 3, 5
RAS-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	L	H	X	X	X	High-Z	4

NOTE:
1. These WRITE cycles may also be BYTE WRITE cycles (either CASL or CASH active).
2. These READ cycles may also be BYTE READ cycles (either CASL or CASH active).
3. EARLY-WRITE only.
4. Only one of the two CAS must be active (CASL or CASH).
3. Data-in will be dependent on the mask provided (MT4C16259 only). Refer to Figure 5.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	160	140	120	mA	3, 4, 42
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC (MIN); ^tCP, ^tASC = 10ns)	I_{CC4}	120	110	100	mA	3, 4, 42
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	160	140	120	mA	3, 5, 42
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	160	140	120	mA	3, 5

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CAPACITANCE

(Note: 2)

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PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$/($\overline{CASL}$,$\overline{CASH}$), ($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	180		200		245		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	45		50		55		ns	35
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	95		100		110		ns	35
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		25	ns	15, 33
Output Enable time	^tOE		20		20		25	ns	33
Access time from column address	^tAA		35		40		45	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		40		45		55	ns	33
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (PAGE MODE)	^tRASP	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		25		ns	40
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	25	100,000	ns	39
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	32
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16, 36
$\overline{CAS}$ precharge time (PAGE MODE)	^tCP	10		10		10		ns	36
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	50	20	60	25	75	ns	17, 31
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	32
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		10		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	15	40	20	55	ns	18
Column address setup time	^tASC	0		0		0		ns	31
Column address hold time	^tCAH	15		15		20		ns	31
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		75		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		40		55		ns	
Read command setup time	^tRCS	0		0		0		ns	26, 31
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26 ,32
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	33

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	tOFF	0	15	0	15	0	20	ns	20, 29, 33
Output disable time	tOD		15		15		20	ns	29, 41
Write command setup time	tWCS	0		0		0		ns	21, 26, 31
Write command hold time	tWCH	15		15		20		ns	26, 40
Write command hold time (referenced to $\overline{RAS}$)	tWCR	55		60		75		ns	26
Write command pulse width	tWP	10		10		20		ns	26
Write command to $\overline{RAS}$ lead time	tRWL	20		20		25		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		20		25		ns	26, 32
Data-in setup time	tDS	0		0		0		ns	22, 33
Data-in hold time	tDH	15		15		20		ns	22, 33
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	95		105		135		ns	21
Column address to $\overline{WE}$ delay time	tAWD	60		65		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	45		45		60		ns	21, 31
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF		8		8		8	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	10		10		10		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	5, 31
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	10		10		10		ns	5, 32
MASKED WRITE command to $\overline{RAS}$ setup time	tWRS	0		0		0		ns	26, 27
$\overline{WE}$ hold time (MASKED WRITE and $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRH	15		15		15		ns	26
Mask data to $\overline{RAS}$ setup time	tMS	0		0		0		ns	26, 27
Mask data to $\overline{RAS}$ hold time	tMH	15		15		15		ns	26, 27
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	20		20		25		ns	28
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
Last $\overline{CAS}$ going LOW to first $\overline{CAS}$ to return HIGH	tCLCH	10		10		10		ns	34
$\overline{WE}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tWRP	10		10		10		ns	

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NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gate and 100pF.
14. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that ^tRCD ≥ ^tRCD (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, not a reference to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, a LATE-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C16256/8. Write command is defined as $\overline{WE}$ going LOW on the MT4C16257/9.
27. MT4C16258/9 only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).

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NOTES (continued)

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30. Notes 31 through 41 apply to MT4C16257/9 only (*):
31. *The first $\overline{CAS}$x edge to transition LOW.
32. *The last $\overline{CAS}$x edge to transition HIGH.
33. *Output parameter (DQx) is referenced to corresponding $\overline{CAS}$ input; DQ1-DQ8 by $\overline{CASL}$ and DQ9-DQ16 by $\overline{CASH}$.
34. *Last falling $\overline{CAS}$x edge to first rising $\overline{CAS}$x edge.
35. *Last rising $\overline{CAS}$x edge to next cycle's last rising $\overline{CAS}$x edge.
36. *Last rising $\overline{CAS}$x edge to first falling $\overline{CAS}$x edge.
37. *First DQs controlled by the first $\overline{CAS}$x to go LOW.
38. *Last DQs controlled by the last $\overline{CAS}$x to go HIGH.
39. *Each $\overline{CAS}$x must meet minimum pulse width.
40. *Last $\overline{CAS}$x to go LOW.
41. *All DQs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
42. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

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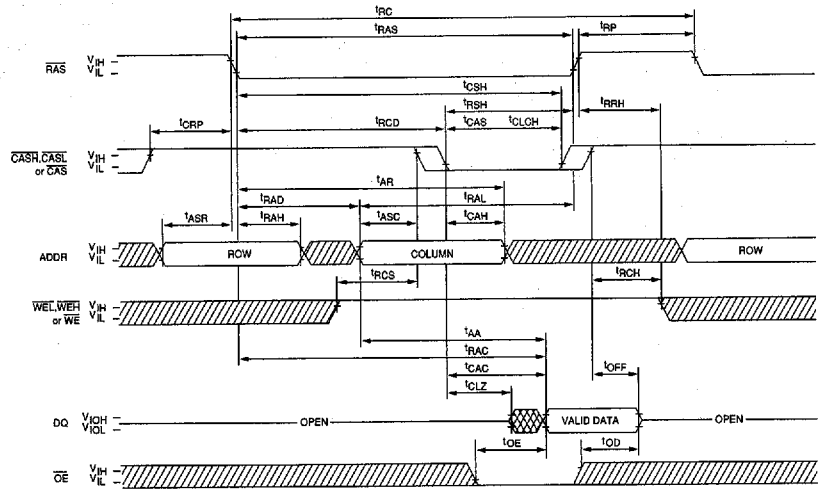
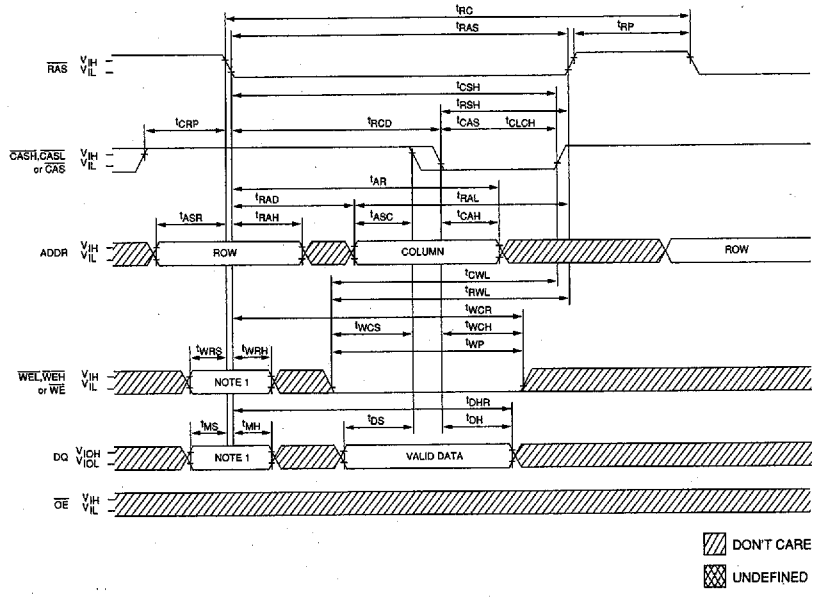
READ CYCLE



EARLY-WRITE CYCLE



NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

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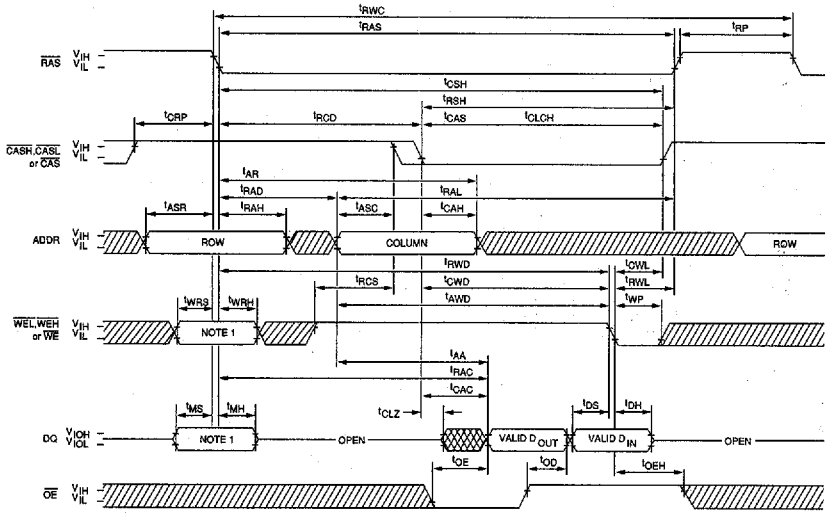
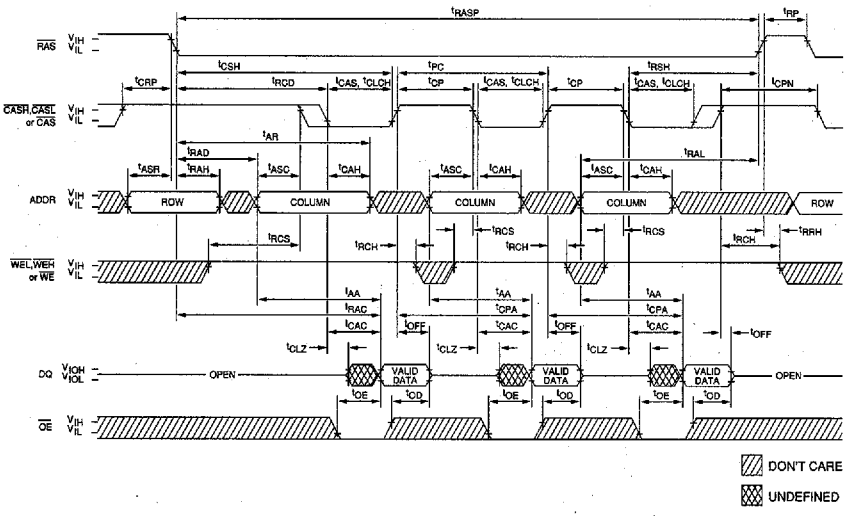
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES) T-46-23-17



FAST-PAGE-MODE READ CYCLE



NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

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WIDE DRAM

FAST-PAGE-MODE EARLY-WRITE CYCLE

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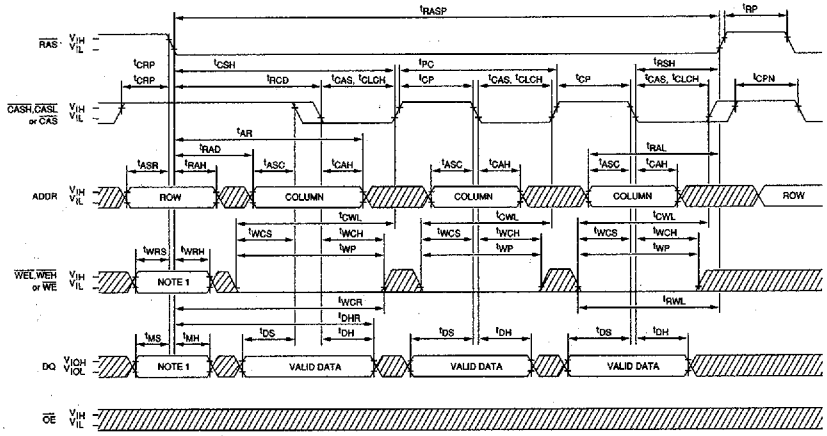
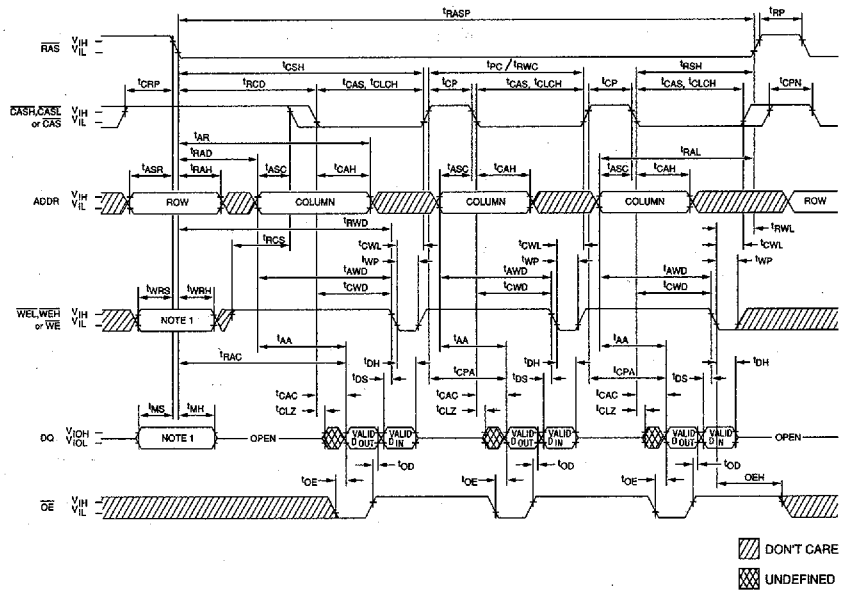


FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C16258 and MT4C16259 only. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE ($\overline{WE}$ LOW at $\overline{RAS}$ time). $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C16256 and MT4C16257 are "don't care" at $\overline{RAS}$ time.

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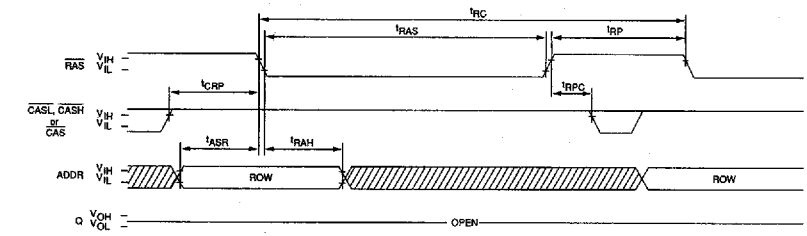
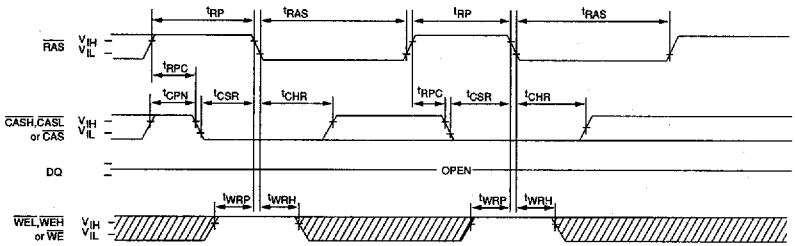
RAS ONLY REFRESH CYCLE

(ADDR = A0-A8, OE; WEL, WEH or WE = DON'T CARE)



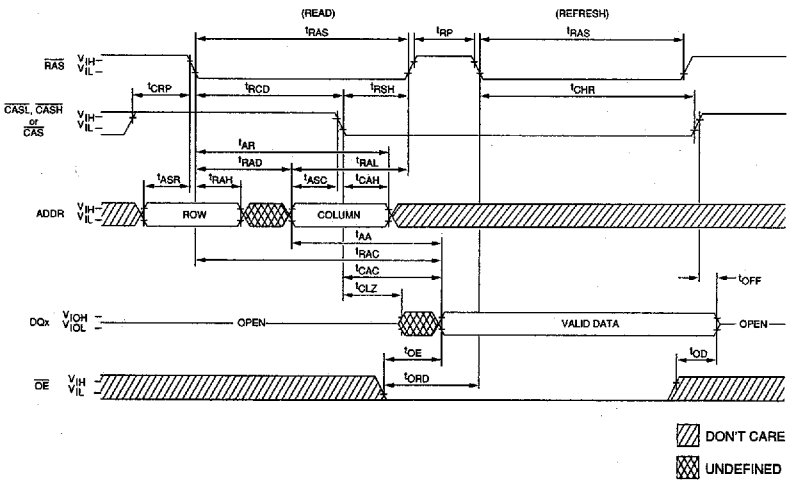
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A8; and OE = DON'T CARE)



HIDDEN REFRESH CYCLE [24]

(WEL, WEH or WE = HIGH; OE = LOW)



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