

Complementary Plastic Power Transistors

NPN/PNP Silicon DPAK For Surface Mount Applications

... designed for low voltage, low-power, high-gain audio amplifier applications.

- Collector-Emitter Sustaining Voltage —
 $V_{CEO(sus)} = 25 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain — $h_{FE} = 70 \text{ (Min) @ } I_C = 500 \text{ mAdc}$
 $= 45 \text{ (Min) @ } I_C = 2 \text{ Adc}$
 $= 10 \text{ (Min) @ } I_C = 5 \text{ Adc}$
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("–1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("T4" Suffix)
- Low Collector-Emitter Saturation Voltage —
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$
 $= 0.75 \text{ Vdc (Max) @ } I_C = 2.0 \text{ Adc}$
- High Current-Gain — Bandwidth Product — $f_T = 65 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakage — $I_{CBO} = 100 \text{ nAdc @ Rated } V_{CB}$

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	40	Vdc
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Emitter-Base Voltage	V_{EB}	8	Vdc
Collector Current — Continuous Peak	I_C	5 10	Adc
Base Current	I_B	1	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	12.5 0.1	Watts W/ $^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}^*$ Derate above 25°C	P_D	1.4 0.011	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	$^\circ\text{C/W}$
Junction to Ambient*	$R_{\theta JA}$	89.3	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (1) ($I_C = 10 \text{ mAdc}, I_E = 0$)	$V_{CEO(sus)}$	25	—	Vdc
Collector Cutoff Current ($V_{CB} = 40 \text{ Vdc}, I_E = 0$) ($V_{CB} = 40 \text{ Vdc}, I_E = 0, T_J = 125^\circ\text{C}$)	I_{CBO}	—	100 100	nAdc
Emitter Cutoff Current ($V_{BE} = 8 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	100	nAdc

* When surface mounted on minimum pad sizes recommended.

(continued)

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\approx 2\%$.

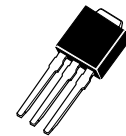
REV 1

NPN
MJD200
PNP
MJD210

SILICON
POWER TRANSISTORS
5 AMPERES
25 VOLTS
12.5 WATTS

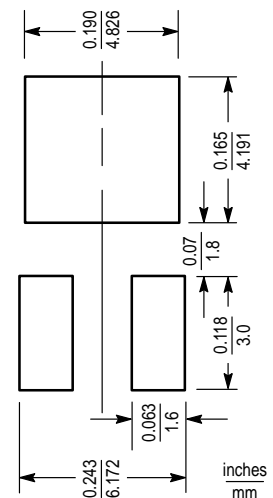


CASE 369A-13



CASE 369-07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MJD200 MJD210

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS				
DC Current Gain (1) ($I_C = 500\text{ mAdc}$, $V_{CE} = 1\text{ Vdc}$) ($I_C = 2\text{ Adc}$, $V_{CE} = 1\text{ Vdc}$) ($I_C = 5\text{ Adc}$, $V_{CE} = 2\text{ Vdc}$)	h_{FE}	70 45 10	— 180 —	—
Collector–Emitter Saturation Voltage (1) ($I_C = 500\text{ mAdc}$, $I_B = 50\text{ mAdc}$) ($I_C = 2\text{ Adc}$, $I_B = 200\text{ mAdc}$) ($I_C = 5\text{ Adc}$, $I_B = 1\text{ Adc}$)	$V_{CE(sat)}$	— — —	0.3 0.75 1.8	Vdc
Base–Emitter Saturation Voltage (1) ($I_C = 5\text{ Adc}$, $I_B = 1\text{ Adc}$)	$V_{BE(sat)}$	—	2.5	Vdc
Base–Emitter On Voltage (1) ($I_C = 2\text{ Adc}$, $V_{CE} = 1\text{ Vdc}$)	$V_{BE(on)}$	—	1.6	Vdc

DYNAMIC CHARACTERISTICS

Current–Gain — Bandwidth Product (2) ($I_C = 100\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f_{test} = 10\text{ MHz}$)	f_T	65	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	MJD200 MJD210 C_{ob}	— —	80 120	pF

- (1) Pulse Test: Pulse Width = $300\ \mu\text{s}$, Duty Cycle $\approx 2\%$.
 (2) $f_T = |h_{fe}| \cdot f_{test}$.

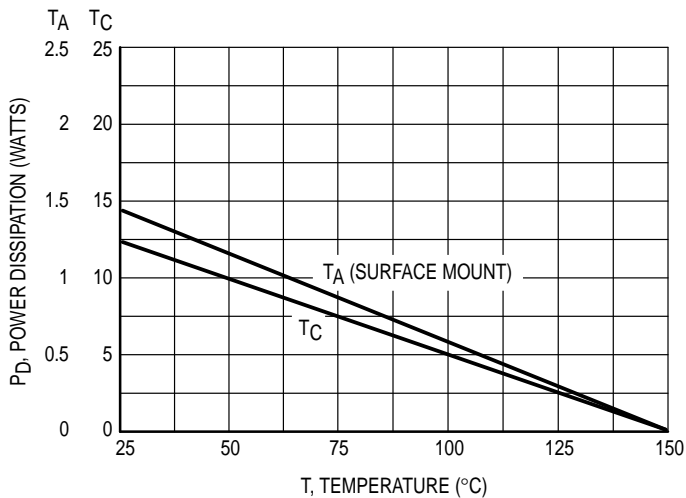


Figure 1. Power Derating

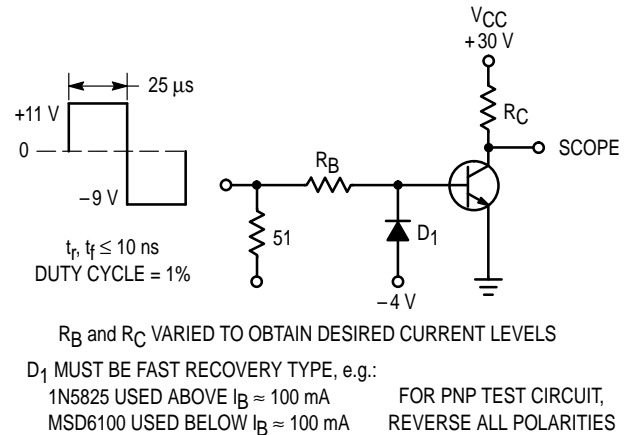


Figure 2. Switching Time Test Circuit

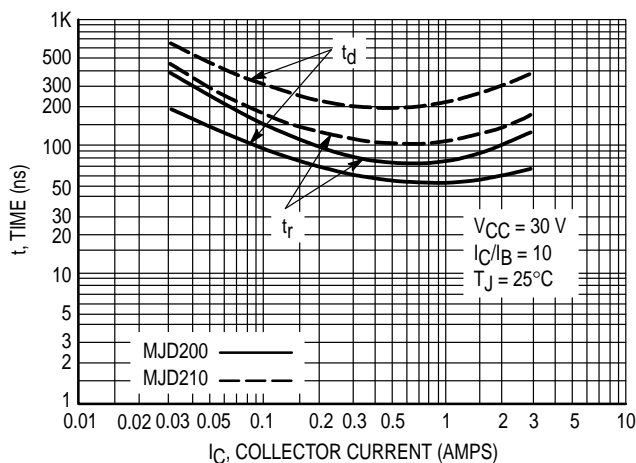


Figure 3. Turn–On Time

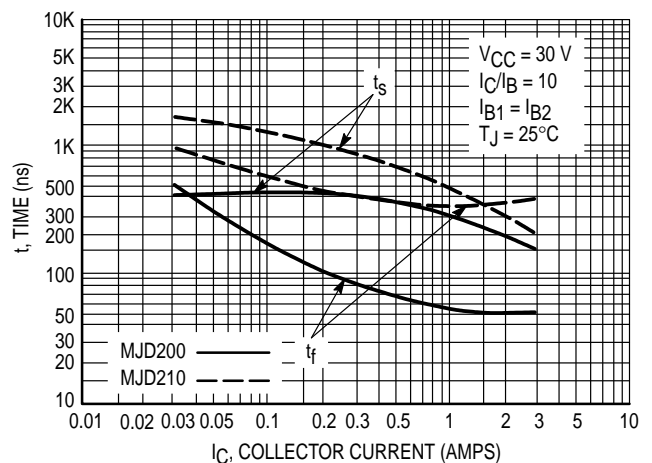


Figure 4. Turn–Off Time

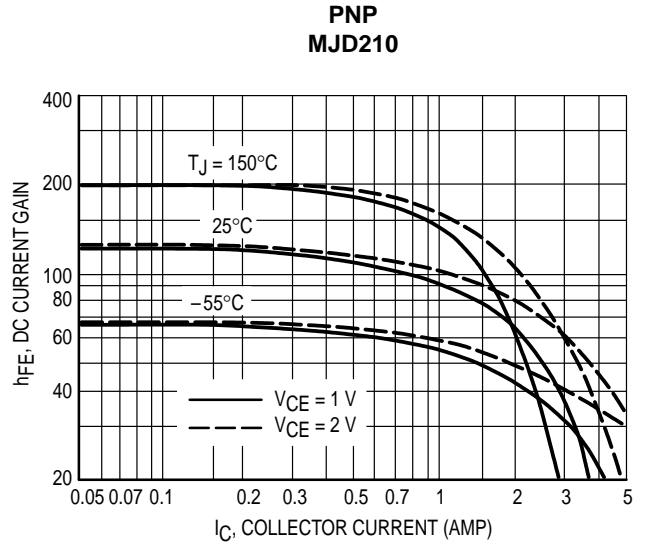
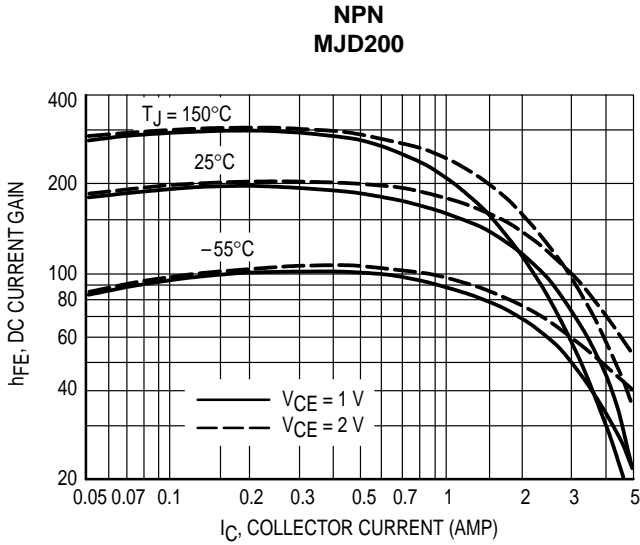


Figure 5. DC Current Gain

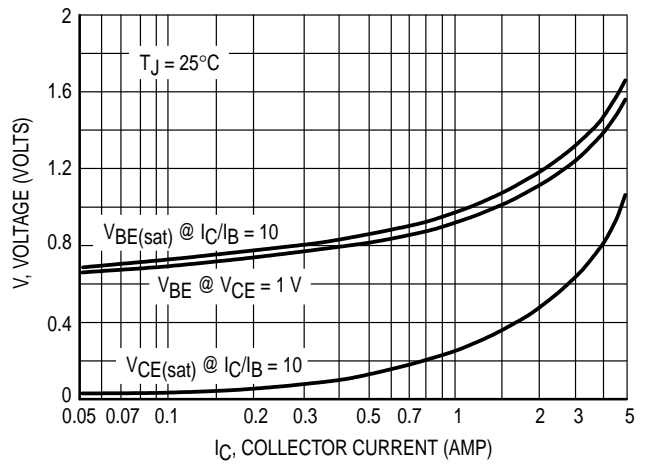
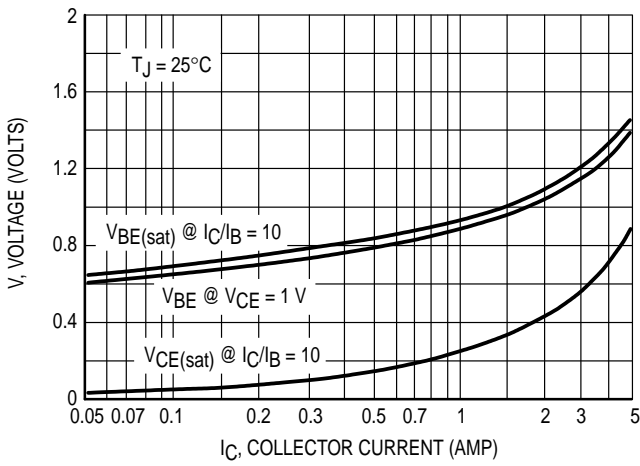


Figure 6. "On" Voltage

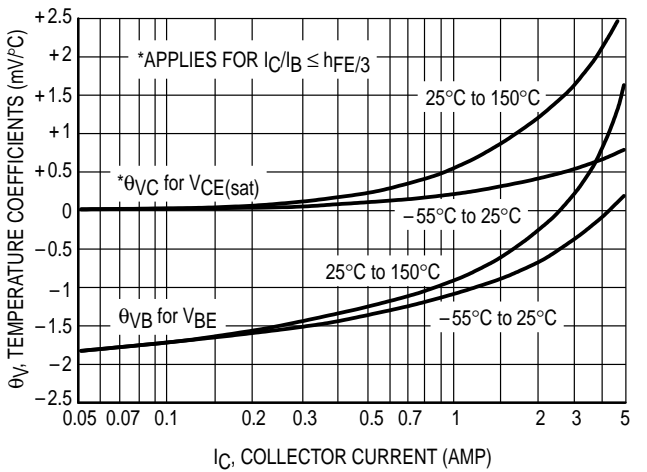
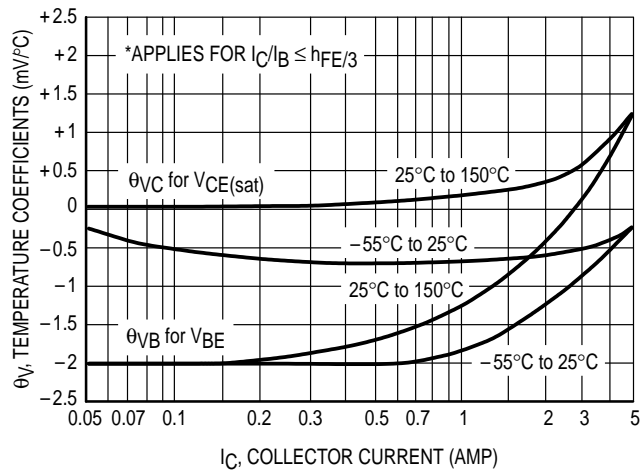


Figure 7. Temperature Coefficients

MJD200 MJD210

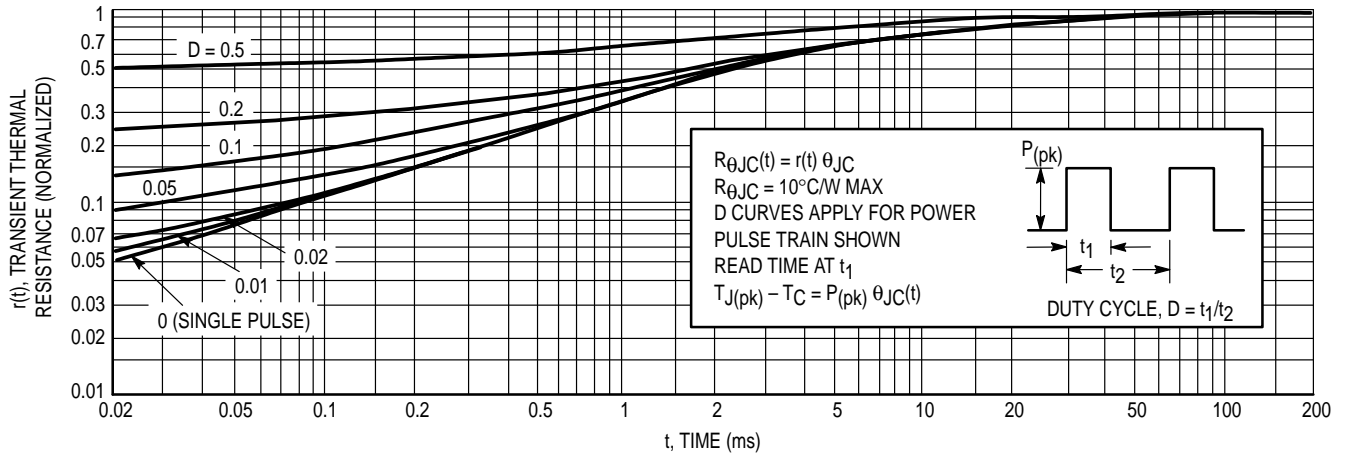


Figure 8. Thermal Response

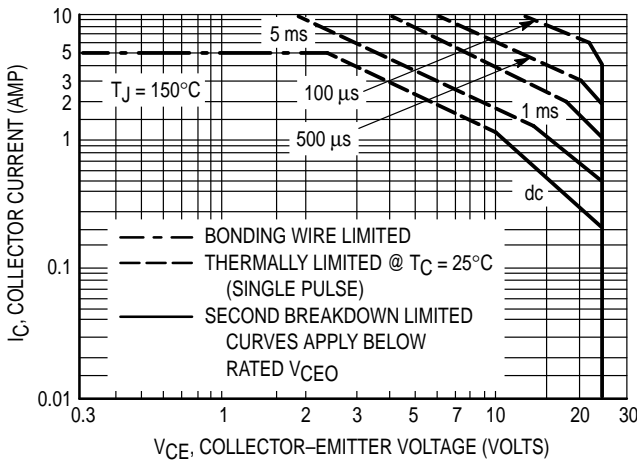


Figure 9. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^{\circ}\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Case 369-05 may be ordered by adding a "-1" suffix to the device title (i.e. MJD200-1)

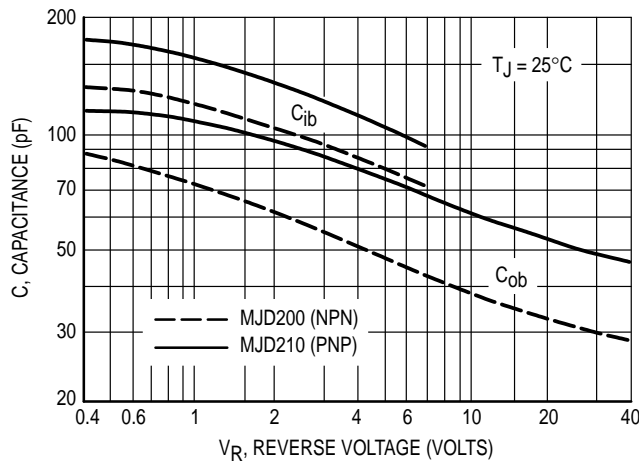
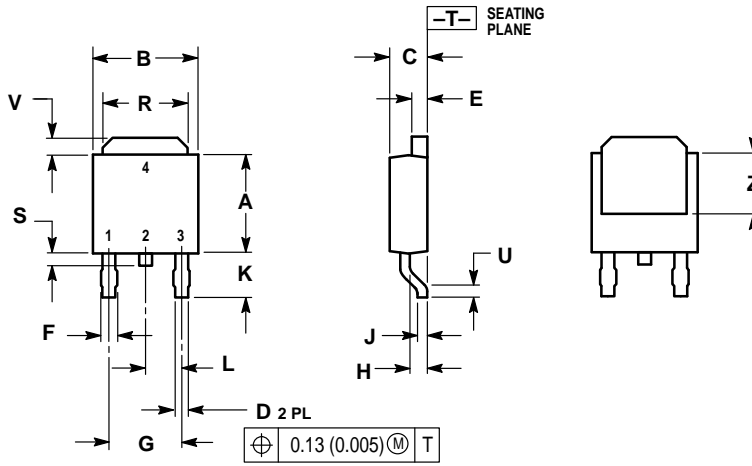


Figure 10. Capacitance

PACKAGE DIMENSIONS

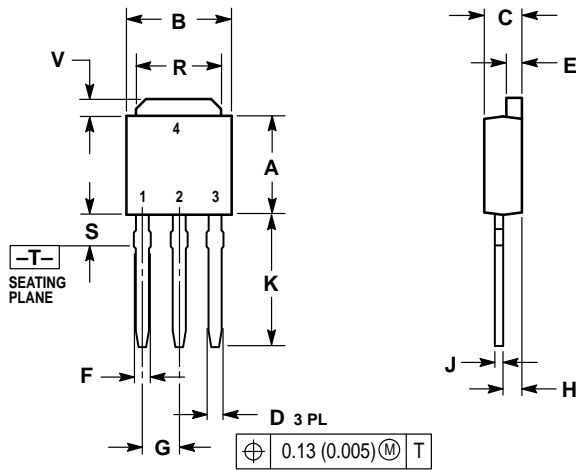


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

- STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR

CASE 369A-13
 ISSUE W




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G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

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 PIN 1. BASE
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CASE 369-07
 ISSUE K

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How to reach us:

USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609
INTERNET: <http://Design-NET.com>

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

