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DATA SHEET

gmZAN2

Flat Panel Monitor Controller IC

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Document History:

Revision	Description	Date
C0022-DAT-01A	Initial Release	June 2001
C0022-DAT-01B	4 pins were changed from reserve to three VSS (pin 5, 59 and 147) one VDD (pin 60). Voltages have been swapped (pin 40 and108) from 2.5V to 3.3V and vice versa (pin 125); Table 3 and Table 6	July 2001
C0022-DAT-01C	Added ESM in section 1 and 2.1.15 and updated section 3 with measured values	October 2001
C0022-DAT-01D	Changed max. external OSD Clock frequency to 80MHz in section 2.8.4 and in Table 18 and Figure 14	August 2002

Related Documents:

Doc Number	Title
C0022-PBR-01C	gmZAN2 Product Brief
C0021-DAT-01F	gmZAN1 Data Sheet

Table of Contents

Table of Figures

List of Tables

1. OVERVIEW

The gmZAN2 is a continuation of Genesis Microchips's successful and most widely adopted design, the gmZAN1, used in the analog interface mainstream XGA LCD monitors. It provides a further overall cost reduction alternative to the existing gmZAN1 designs with lower power consumption. It is as fully featured as the gmZAN1 by integrating the Genesis patented Display Perfection Technology as well as the latest generation of analog mixed signal technology that has proven to be high-quality and most reliable. In addition, the gmZAN2 includes Energy Spectrum Management that helps further reduce the cost associated with the LCD monitors meeting emissions standards by reducing EMI. It may eliminate the use of parallel-to-serial transmitter and serial-to-parallel receiver devices

As shown Figure 2, the gmZAN2 has an integrated the Genesis sixth generation ADC and is feature compatible to the gmZAN1. It is **the LCD monitor controller** for the mainstream XGA LCD monitors. It provides a very cost-effective and simplified design.

A reference design is available to demonstrate the gmZAN2 solution.

1.1 Features

Feature Overview

- Fully integrated 135MHz 8-bit triple-ADC, PLL, and pre-amplifier
- Adaptive Contrast Enhancement (ACE) scaling
- On-chip programmable OSD engine
- Integrated PLLs
- 10-bit programmable gamma correction
- Host interface with 1 or 4 data bits
- Pin-compatible & firmware compatible to gmZAN1

- **Integrated Analog Front End**
  - Integrated 8-bit triple ADC
  - Up to 135MHz sampling rates
  - No additional components needed
  - All color depths up to 24-bits/pixel are supported

- **High-Quality Advanced Scaling**
  - Fully programmable zoom
  - Independent horizontal / vertical zoom
  - Enhanced and adaptive scaling algorithm for optimal image quality
  - Recovery Mode / Native Mode

- **Input Format**
  - Analog RGB up to XGA 85Hz

- **Output Format**
  - Support for 8 or 6-bit panels (with high quality dithering)
  - One or two pixel output format

- **Built In High-Speed Clock Generator**
  - Fully programmable timing parameters
  - On-chip PLLs generate clocks for the on-chip ADC and pixel clock from a single reference oscillator

- **Auto-Configuration / Auto-Detection**
  - Phase and image positioning
  - Input format detection

- **Operating Modes**
  - Bypass mode with no filtering
  - Multiple zoom modes:
    - with filtering
    - with adaptive (ACE) filtering

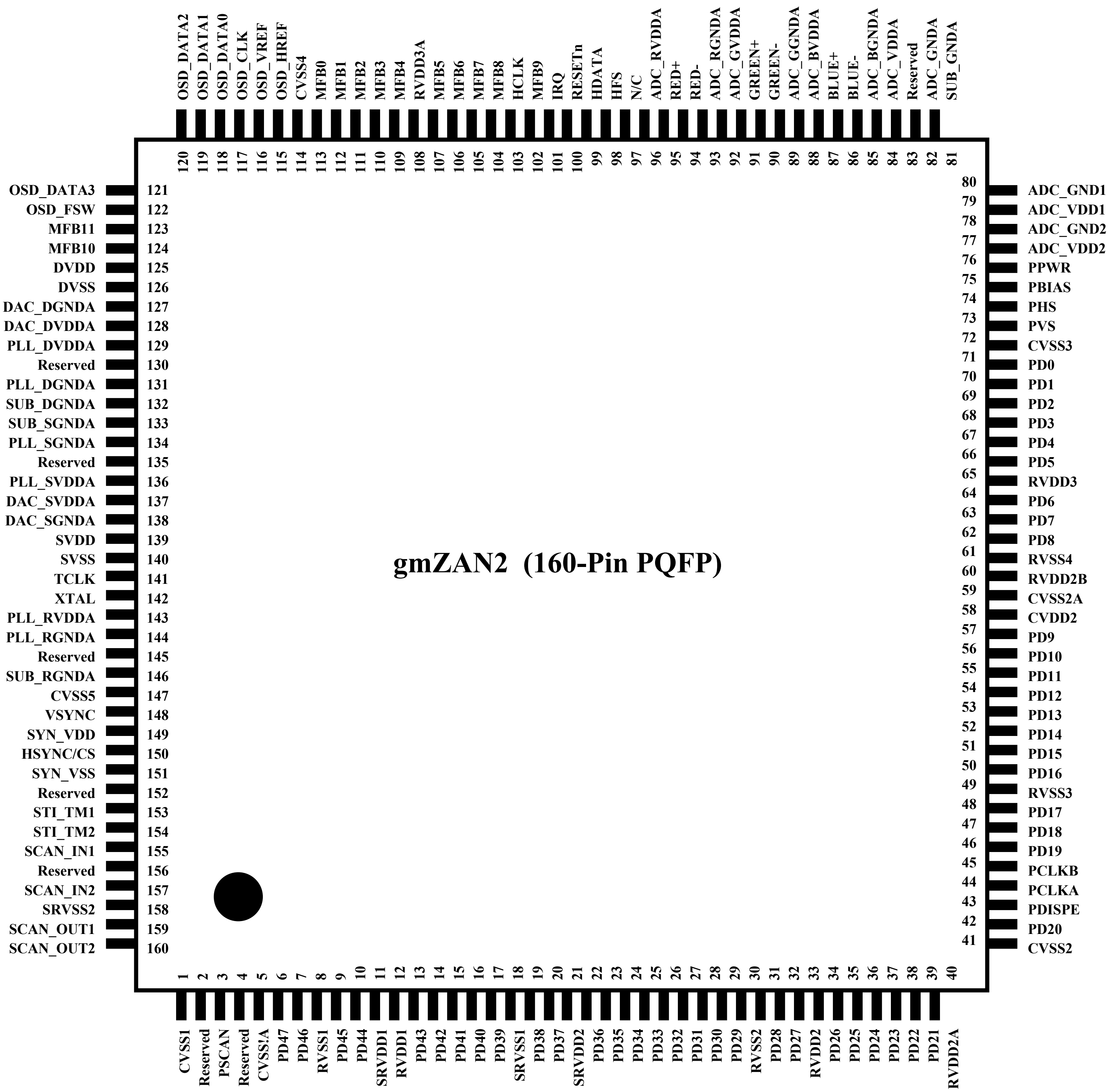
- **Integrated On-Screen Display**
  - On-chip character RAM and ROM for better customization
  - External OSD supported for greater flexibility
  - Many other font capabilities including: blinking, overlay and transparency

Package

- 160-pin PQFP

1.2 Pin Out Diagram

Figure 1. gmZAN2 Pin Diagram



1.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 1. Analog-to-Digital Converter

Pin	Name	In/Out	Drive Current (@10pF)	Voltage	Description
77	ADC_VDD2			2.5V	Digital power for ADC encoding logic. Must be bypassed with 0.1 uF capacitor to pin 78 (ADC_GND2)
78	ADC_GND2				Digital GND for ADC encoding logic. Must be directly connected to the digital system ground plane.
79	ADC_VDD1			2.5V	Digital power for ADC clocking circuit. Must be bypassed with 0.1 uF capacitor to pin 80 (ACD_GND1)
80	ADC_GND1				Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
81	SUB_GNDA				Dedicated pin for substrate guard ring that protects the ADC reference system. Must be directly connected to the analog system ground plane.
82	ADC_GNDA				Analog ground for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be directly connected to analog system ground plane.
84	ADC_VDDA			3.3V	Analog power for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Must be bypassed with 0.1 uF capacitor to pin 82 (ADC_GNDA).
83	Reserved				Test output. Do not connect.
85	ADC_BGNDA				Analog ground for the blue channel. Must be directly connected to the analog system ground plane.
88	ADC_BVDDA			3.3V	Analog power for the blue channel. Must be bypassed with 0.1 uF capacitor to pin 85 (BGNDA).
86	BLUE-	In			Negative analog input for the Blue channel.
87	BLUE+	In			Positive analog input for the Blue channel.
89	ADC_GGNDA				Analog ground for the green channel . Must be directly connected to the analog system ground plane.
92	ADC_GVDDA			3.3V	Analog power for the green channe. Must be bypassed with 0.1 uF capacitor to pin 89 (ADC_GGNDA).
90	GREEN-	In			Negative analog input for the Green channel.
91	GREEN+	In			Positive analog input for the Green channel.
93	ADC_RGNDA				Analog ground for the red channel. Must be directly connected to the analog sys tem ground plane.
96	ADC_RVDDA			3.3V	Analog power for the red channel. Must be bypassed with 0.1 uF capacitor to pin 93 (ADC_RGNDA).
94	RED-	In			Negative analog input for the Red channel.
95	RED+	In			Positive analog input for the Red channel.

Table 2. Host Interface (HIF) / External On-Screen Display

Pin	Name	In / Out	Drive Current (@10pF)	Voltage	Description
98	HFS	in			Host Frame Sync. Frames the packet on the serial channel.
103	HCLK	in			Clock signal input for the 3-wire serial communication.
99	HDATA	in/out	4 mA		Data signal for the 3-wire serial communication
100	RESETn	in			Resets the gmZAN2 chip to a known state when low.
101	IRQ	out	4 mA		Interrupt request output
115	OSD-HREF	out	4 mA		HSYNC output for an external OSD controller chip.
116	OSD-VREF	out	4 mA		VSYNC output for an external OSD controller chip.
117	OSD-Clk	out	8 mA		Clock output for an external OSD controller chip.
118	OSD-Data0	in			Data input 0 from an external OSD controller.
119	OSD-Data1	in			Data input 1 from an external OSD controller.
120	OSD-Data2	in			Data input 2 from an external OSD controller.
121	OSD-Data3	in			Data input 3 from an external OSD controller.
122	OSD-FSW	in			External OSD window display enable. Displays data from external OSD controller when high.
123	MFB11	in/out	8 mA		Multi-Function Bus 11. One of twelve multi-function signals MFB[11:0].
124	MFB10	in/out	8 mA		Multi-Function Bus 10. One of twelve multi-function signals MFB[11:0].
102	MFB9	in/out	8 mA		Multi-Function Bus 9. One of twelve multi-function signals MFB[11:0]. Also used as HDATA3 in a 4-bit host interface configuration.
104	MFB8	in/out	8 mA		Multi-Function Bus 8. One of twelve multi-function signals MFB[11:0]. Also used as HDATA2 in a 4-bit host interface configuration.
105	MFB7	in/out	8 mA		Multi-Function Bus 7. One of twelve multi-function signals MFB[11:0]. Also used as HDATA1 in a 4-bit host interface configuration.
106	MFB6	in/out	8 mA		Multi-Function Bus 6. One of twelve multi-function signals MFB[11:0]. Internally pulled up. When externally pulled down (sampled at reset) the host interface is configured for 4 bits wide. In this configuration, MFB9:7 are used as HDATA3:1.
107	MFB5	in/out	8 mA		Multi-Function Bus 5. One of twelve multi-function signals MFB[11:0]. Internally pulled up. When externally pulled down (sampled at reset) the chip uses an external crystal resonator across pins 141 and 142, instead of an oscillator.
109	MFB4	in/out	8 mA		Multi-Function Bus 4. One of twelve multi-function signals MFB[11:0].
110	MFB3	in/out	8 mA		Multi-Function Bus 3. One of twelve multi-function signals MFB[11:0].
111	MFB2	in/out	8 mA		Multi-Function Bus 2. One of twelve multi-function signals MFB[11:0].
112	MFB1	in/out	8 mA		Multi-Function Bus 1. One of twelve multi-function signals MFB[11:0].
113	MFB0	in/out	8 mA		Multi-Function Bus 0. One of twelve multi-function signals MFB[11:0].

Table 3. Clock Recovery / Time Base Conversion

Pin	Name	In / Out	Drive Current (@10pF)	Voltage	Description
125	DVDD			2.5V	Digital power for Destination DDS (direct digital synthesizer). Must be bypassed with a 0.1 uF capacitor to digital ground plane.
127	DAC_DGNDA				Analog ground for Destination DDS DAC. Must be directly connected to the ana log system ground plane.
128	DAC_DVDDA			3.3V	Analog power for Destination DDS DAC. Must be bypassed with a 0.1 uF capaci tor to pin 127 (DAC_DGNDA)
129	PLL_DVDDA			3.3V	Analog power for the Destination DDS PLL. Must be bypassed with a 0.1 uF capacitor to pin 131 (PLL_DGNDA)
130	Reserved				Test output. Do not connect.
131	PLL_DGNDA				Analog ground for the Destination DDS PLL. Must be directly connected to the analog system ground plane.
132	SUB_DGNDA				Dedicated pin for the substrate guard ring that protects the Destination DDS. Must be directly connected to the analog system ground plane.
133	SUB_SGNDA				Dedicated pin for the substrate guard ring that protects the Source DDS. Must be directly connected to the analog system ground plane.
134	PLL_SGNDA				Analog ground for the Source DDS PLL. Must be directly connected to the ana log system ground.
135	Reserved				Test output. Do not connect.
136	PLL_SVDDA			3.3V	Analog power for the Source DDS PLL. Must be bypassed with a 0.1 uF capaci tor to pin 134 (PLL_SGNDA)
137	DAC_SVDDA			3.3V	Analog power for the Source DDS DAC. Must be bypassed with a 0.1 uF capaci tor to pin 138 (DAC_SGNDA)
138	DAC_SGNDA				Analog ground for the Source DDS DAC. Must be directly connected to the ana log system ground.
139	SVDD			2.5V	Digital power for the Source DDS and destination DDS. Must be bypassed with a 0.1 uF capacitor to digital ground plane.
141	TCLK	In			Reference clock (TCLK) input from the 50 Mhz crystal oscillator.
142	XTAL	Out			If using an external oscillator, leave this pin floating. If using an external crystal, connect crystal between TCLK (141) and XTAL (142). See MFB5 (pin 107).
143	PLL_RVDDA			3.3V	Analog power for the Reference DDS PLL. Must be bypassed with a 0.1 uF capacitor to pin 144 (PLL_RGNDA)
144	PLL_RGNDA				Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
145	Reserved				Test output. Do not connect.
146	SUB_RGNDA				Dedicated pin for the substrate guard ring that protects the Reference DDS. Must be directly connected to the analog system ground plane.
148	VSYNC	In			CRT Vsync input. TTL Schmitt trigger input.
149	SYN_VDD			2.5V	Digital power for CRT Sync input
150	HSYNC/ CSYNC	In			CRT Hsync or CRT composite sync input. TTL Schmitt trigger input.

Table 4. TFT Panel Interface

Pin	Name	In / Out	Drive Current (@10pF)	Description 2pxl/clk 8-bit	2pxl/clk 6-bit	1pxl/clk 8-bit	1pxl/clk 6-bit	TFT
6	PD47	out	2 mA ~ 20 mA	OB1	-	-	-	
7	PD46	out	2 mA ~ 20 mA	OB0	-	-	-	
9	PD45	out	2 mA ~ 20 mA	OG1	-	-	-	
10	PD44	out	2 mA ~ 20 mA	OG0	-	-	-	
13	PD43	out	2 mA ~ 20 mA	OR1	-	-	-	
14	PD42	out	2 mA ~ 20 mA	OR0	-	-	-	
15	PD41	out	2 mA ~ 20 mA	EB1	-	B1	-	
16	PD40	out	2 mA ~ 20 mA	EB0	-	B0	-	
17	PD39	out	2 mA ~ 20 mA	EG1	-	G1	-	
19	PD38	out	2 mA ~ 20 mA	EG0	-	G0	-	
20	PD37	out	2 mA ~ 20 mA	ER1	-	R1	-	
22	PD36	out	2 mA ~ 20 mA	ER0	-	R0	-	
23	PD35	out	2 mA ~ 20 mA	OB7	OB5	-	-	
24	PD34	out	2 mA ~ 20 mA	OB6	OB4	-	-	
25	PD33	out	2 mA ~ 20 mA	OB5	OB3	-	-	
26	PD32	out	2 mA ~ 20 mA	OB4	OB2	-	-	
27	PD31	out	2 mA ~ 20 mA	OB3	OB1	-	-	
28	PD30	out	2 mA ~ 20 mA	OB2	OB0	-	-	
29	PD29	out	2 mA ~ 20 mA	OG7	OG5	-	-	
31	PD28	out	2 mA ~ 20 mA	OG6	OG4	-	-	
32	PD27	out	2 mA ~ 20 mA	OG5	OG3	-	-	
34	PD26	out	2 mA ~ 20 mA	OG4	OG2	-	-	
35	PD25	out	2 mA ~ 20 mA	OG3	OG1	-	-	
36	PD24	out	2 mA ~ 20 mA	OG2	OG0	-	-	
37	PD23	out	2 mA ~ 20 mA	OR7	OR5	-	-	
38	PD22	out	2 mA ~ 20 mA	OR6	OR4	-	-	
39	PD21	out	2 mA ~ 20 mA	OR5	OR3	-	-	
42	PD20	out	2 mA ~ 20 mA	OR4	OR2	-	-	
46	PD19	out	2 mA ~ 20 mA	OR3	OR1	-	-	
47	PD18	out	2 mA ~ 20 mA	OR2	OR0	-	-	
48	PD17	out	2 mA ~ 20 mA	EB7	EB5	B7	B5	
50	PD16	out	2 mA ~ 20 mA	EB6	EB4	B6	B4	
51	PD15	out	2 mA ~ 20 mA	EB5	EB3	B5	B3	
52	PD14	out	2 mA ~ 20 mA	EB4	EB2	B4	B2	
53	PD13	out	2 mA ~ 20 mA	EB3	EB1	B3	B1	
54	PD12	out	2 mA ~ 20 mA	EB2	EB0	B2	B0	
55	PD11	out	2 mA ~ 20 mA	EG7	EG5	G7	G5	
56	PD10	out	2 mA ~ 20 mA	EG6	EG4	G6	G4	
57	PD9	out	2 mA ~ 20 mA	EG5	EG3	G5	G3	

Pin	Name	In / Out	Drive Current (@10pF)	Description 2pxl/clk 8-bit	2pxl/clk 6-bit	1pxl/clk 8-bit	1pxl/clk 6-bit	TFT
62	PD8	out	2 mA ~ 20 mA	EG4	EG2	G4	G2	
63	PD7	out	2 mA ~ 20 mA	EG3	EG1	G3	G1	
64	PD6	out	2 mA ~ 20 mA	EG2	EG0	G2	G0	
66	PD5	out	2 mA ~ 20 mA	ER7	EG5	R7	R5	
67	PD4	out	2 mA ~ 20 mA	ER6	ER4	R6	R4	
68	PD3	out	2 mA ~ 20 mA	ER5	ER3	R5	R3	
69	PD2	out	2 mA ~ 20 mA	ER4	ER2	R4	R2	
70	PD1	out	2 mA ~ 20 mA	ER3	ER1	R3	R1	
71	PD0	out	2 mA ~ 20 mA	ER2	ER0	R2	R0	
43	PDispE	out	2 mA ~ 20 mA	This output provides a panel display enable signal that is active when flat panel data is valid.				
74	PHS	out	2 mA ~ 20 mA	This output provides the panel line clock signal.				
73	PVS	out	2 mA ~ 20 mA	This output provides the frame start signal.				
44	PCLKA	out	2 mA ~ 20 mA	This output is used to drive the flat panel shift clock.				
45	PCLKB	out	2 mA ~ 20 mA	Same as PCLKA above. The polarity and the phase of this signal are independently programmable.				
75	Pbias	out	8 mA	This output is used to turn on / off the panel bias power or controls back-light.				
76	Ppwr	out	8 mA	This output is used to control the power to a flat panel.				

NOTE: Drive current of the panel output pins are programmable.

Table 5. Test Pins & Reserve Pins

Pin	Name	In/Out	Drive Current	Description
2	Reserved			N/C. Do not connect.
3	PSCAN	In		Enable automatic device test. When this input is pulled high, the automatic device test mode is entered. An internal pull-down resistor drives this input low for normal operation. This pin should always be tied to ground.
4	Reserved			N/C. Do not connect.
152	Reserved			N/C. Do not connect.
156	Reserved			N/C. Do not connect.
155	SCAN_IN1	In		Scan input 1 used for device testing. This pin should always be tied to ground.
157	SCAN_IN2	In		Scan input 2 used for automatic device testing. This pin should always be tied to ground.
159	SCAN_OUT1	Out		Scan output 1 used for automatic device testing. This pin should not be connected.
160	SCAN_OUT2	Out		Scan output 2 used for automatic device testing. This pin should not be connected.
153	ST1_TM1			ST1_TM1 used for automatic device testing. This pin should always be tied to ground.
154	ST1_TM2			ST1_TM2 used for automatic device testing. This pin should always be tied to ground.

Table 6. VDD / VSS for Core Circuitry, Host Interface, and Panel/Memory Interface

Pins	Description
12, 33, 40, 60, 65, 108	RVDD1 ~ RVDD3, RVDD2A, RVDD2B and RVDD3A for panel / memory interface. Connect to +3.3V.
11,21, 58, 125	SRVDD2-1, CVDD2 and DVDD for core circuitry. Connect to +2.5V.
1, 5, 8, 18, 30, 41, 49, 59, 61, 72, 114, 126, 140, 147, 151, 158	Digital grounds for core circuitry and panel / memory interface. CVSS1, CVSS1A, RVSS1, SRVSS1, RVSS2, CVSS2, RVSS3, CVSS2A, RVSS4, CVSS3, CVSS4, DVSS, SVSS, CVSS5 SYN_VSS and SRVSS2

1.4 System-level Block Diagram

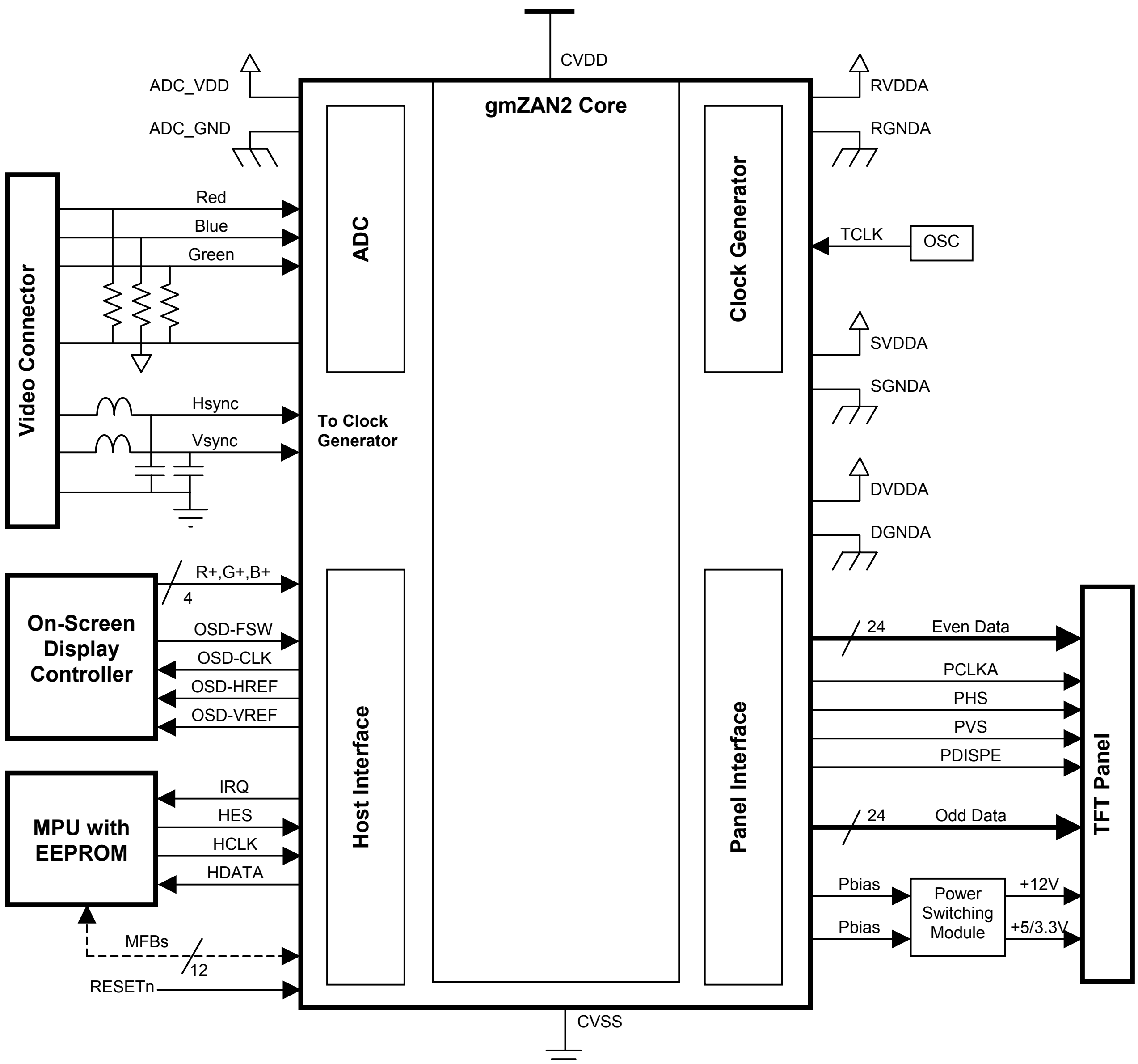


Figure 2. Typical Stand-alone Configuration

1.5 Operating Modes

The Source Clock (also called SCLK in this document) and the Panel Clock are defined as follows:

- The Source Clock is the sample clock regenerated from the input Hsync timing (called clock recovery) by SCLK DDS (direct digital synthesis) and the PLL.
- The Panel Clock is the timing clock for panel data at the single pixel per clock rate. The actual PCLK to the panel may be one-half of this frequency for double-pixel panel data format. When its frequency is different from that of source clock, the panel clock is generated by Destination Clock (or DCLK) DDS / PLL.

There are six display modes: Native, Slow DCLK, Zoom, Downscaling, Destination Stand Alone, and Source Stand Alone.

Each mode is unique in terms of:

- input video resolution vs. panel resolution,
- Source Clock frequency / Panel Clock frequency ratio,
- Source Hsync frequency / Panel Hsync frequency ratio,
- data source (analog RGB, panel background color, on-chip pattern generator)

1.5.1 Native

Panel Clock frequency = Source Clock frequency

Panel Hsync frequency = Input Hsync frequency

Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution and the input data clock frequency is within the panel clock frequency specification of the panel being used.

1.5.2 Slow DCLK

Panel Clock frequency < Source Clock frequency

Panel Hsync frequency = Input Hsync frequency

Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is the same as the panel resolution, but the input data clock frequency exceeds the panel clock frequency specification of the panel being used. The panel clock is scaled to the Source Clock, and the internal data buffers are used to spread out the timing of the input data by making use of the large CRT blanking time to extend the panel horizontal display time.

1.5.3 Zoom

Panel Clock frequency > Source Clock frequency

Panel Hsync frequency > Input Hsync frequency

Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is less than the panel resolution. The input data clock is then locked to the panel clock, which is at a higher frequency. The input data is zoomed to the panel resolution.

1.5.4 Downscaling (Recovery)

Panel Clock frequency < Source Clock frequency

Panel Hsync frequency < Input Hsync frequency

Panel Vsync frequency = Input Vsync frequency

This mode is used when the input resolution is greater than the panel resolution, to provide enough of a display to enable the user to recover to a supported resolution. The input clock is operated at a frequency less than that of the input pixel rate (under-sampled horizontally) and the scaling filter is used to drop input lines. In this mode, zoom scaling must be disabled.

1.5.5 Destination Stand Alone

Panel Clock = DCLK in open loop (not locked)

Panel Hsync frequency = DCLK frequency / (Destination Htotal register value)

Panel Vsync frequency = DCLK frequency / (Dest. Htotal register value * Dest. Vtotal register value)

This mode is used when the input is changing or not available. The OSD may still be used as in all other display modes and stable panel timing signals are produced. This mode may be automatically set when the gmZAN2 detects input timing changes that could cause out-of-spec operation of the panel.

1.5.6 Source Stand Alone

Panel Clock = DCLK in open loop (not locked to input Hsync)

Panel Hsync frequency = SCLK frequency / (Source Htotal register value)

Panel Vsync frequency = SCLK frequency / (Source Htotal register value * Source Vtotal register value)

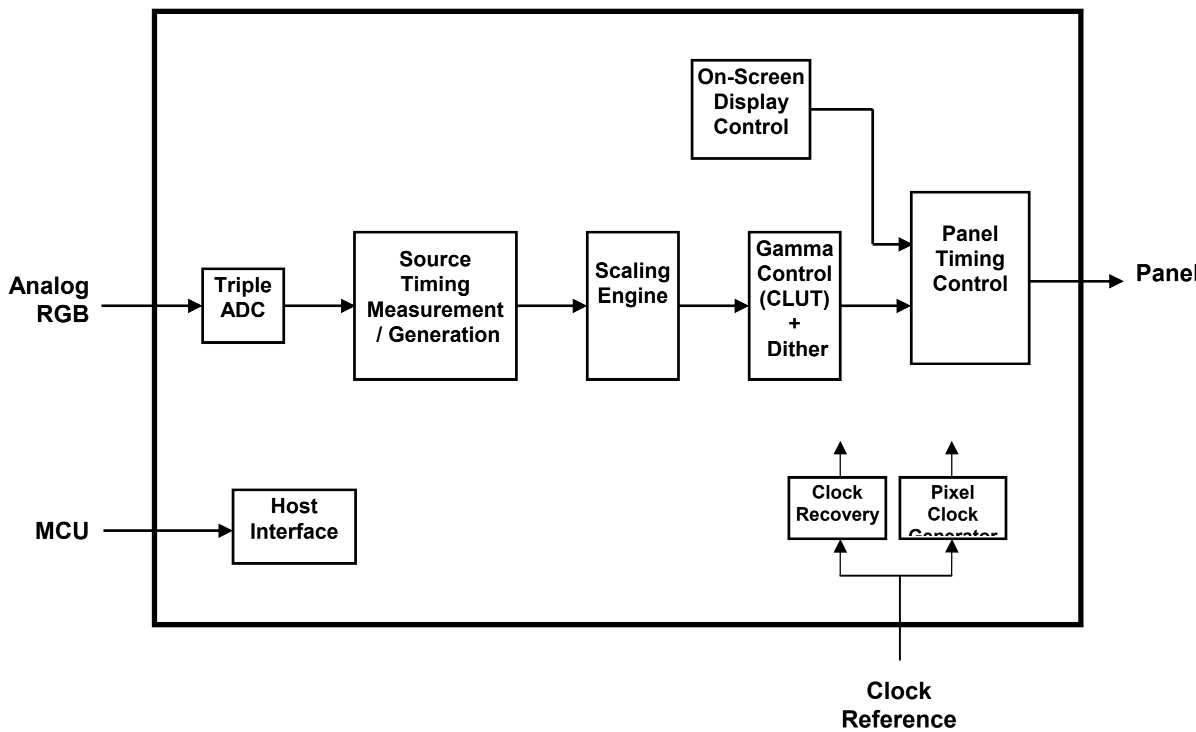
This mode is used to display the pattern generator data. This mode may be useful for testing an LCD panel on the manufacturing line (color temperature calibration, etc.).

2. FUNCTIONAL DESCRIPTION

Figure 3 below shows the main functional blocks inside the gmZAN2.

2.1 Overall Architecture

Figure 3. Block Diagram for gmZAN2



2.2 Clock Recovery Circuit

The gmZAN2 has a built-in clock recovery circuit. This circuit consists of a digital clock synthesizer and an analog PLL. The clock recovery circuit generates the clock used to sample analog RGB data (SCLK or source clock). This circuit is locked to the HSYNC of the incoming video signal. The RCLK generated from the TCLK input is used as a reference clock.

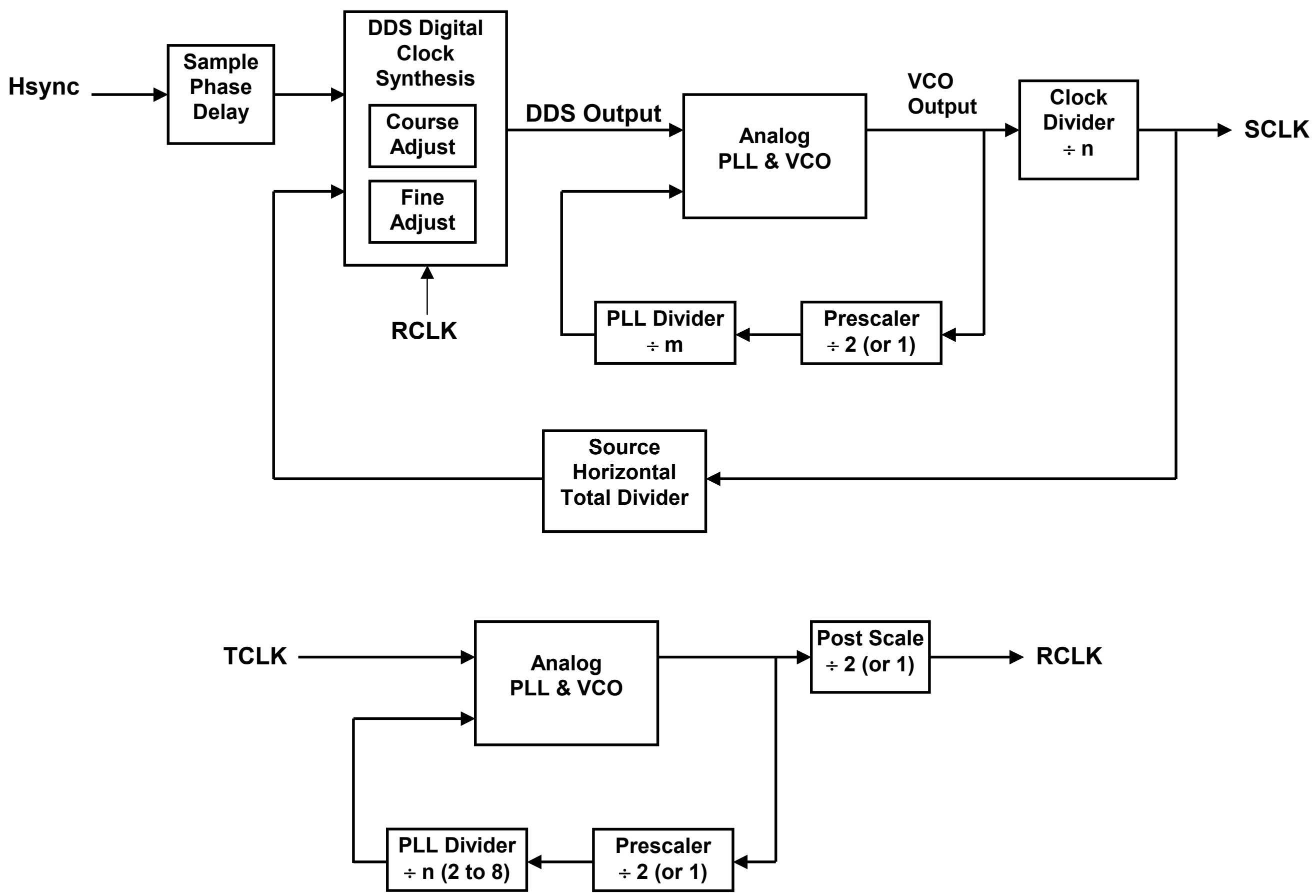
The clock recovery circuit adjusts the SCLK period so that the feedback pulse generated every SCLK period multiplied by the Source Horizontal Total value (as programmed into the registers) locks to the rising edge of the Hsync input. Even though the initial SCLK frequency and the final

SCLK frequency are as far apart as 60MHz, locking can be achieved in less than 1ms across the operating voltage/temperature range.

The SCLK frequency (1/SCLK period) can be set to the range of 10- to 135-MHz. Using the DDS (direct digital synthesis) technology the clock recovery circuit can generate any SCLK clock frequency within this range.

The pixel clock (DCLK or destination clock) is used to drive a panel when the panel clock is different from SCLK (or SCLK/2). It is generated by a circuit virtually identical to the clock recovery circuit. The difference is that DCLK is locked to SCLK while SCLK is locked to the Hsync input. DCLK frequency divided by N is locked to SCLK frequency divided by M. The values M and N are calculated and programmed in the register by firmware. The value M should be close to the Source Htotal value.

Figure 4. Clock Recovery Circuit



The table below summarizes the characteristics of the clock recovery circuit.

Table 7. Clock Recovery Characteristics

	Minimum	Typical	Maximum
SCLK Frequency	20 MHz		135 MHz
Sampling Phase Adjustment		0.5 ns/step, 64 steps	

Patented digital clock synthesis technology makes the gmZAN2 clock circuits very immune to temperature/voltage drift.

2.2.1 Reset

A reset pin (RESETn) sets the gmZAN2 to a known state when this pin is pulled low. The RESETn pin must be low for at least 100ns after the CVDD has become stable (between +2.4V and +2.75V) or until the oscillator used is stable or whichever takes longer in order to reset the gmZAN2 to a known state.

2.2.2 Sampling Phase Adjustment

The ADC sampling phase is adjusted by delaying the Hsync input at the programmable delay cell inside the gmZAN2. The delay value can be adjusted in 64 steps, 0.5 ns/step. The accuracy of the sampling phase is checked by the gmZAN2 and the "score" can be read in a register. This feature will enable accurate auto-adjustment of the ADC sampling phase.

2.2.3 Source Timing Generator

The STG module defines a capture window and sends the input data to the data path block. Figure 5 below shows how the window is defined.

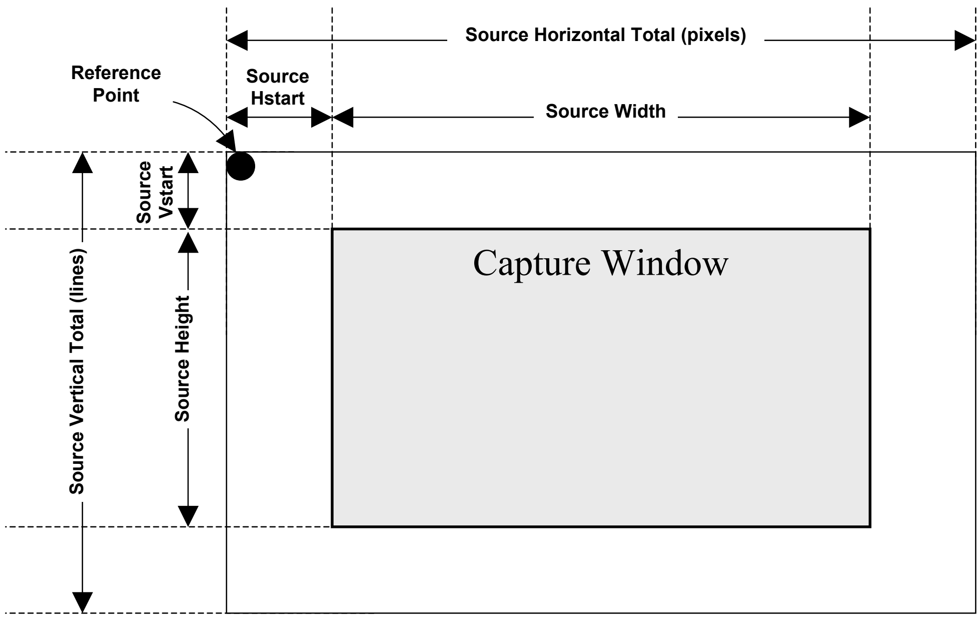
For the horizontal direction, it is defined in SCLKs (equivalent to a pixel count). For the vertical direction, it is defined in lines.

All the parameters in the figure that begin with "Source" are programmed into the gmZAN2 registers. Note that the vertical total is solely determined by the input.

The reference point is as follows:

- The first pixel of a line: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.
- The first line of a frame: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

Figure 5. Capture Window



2.3 Analog-to-Digital Converter

2.3.1 Pin Connection

The RGB signals are to be connected to the gmZAN2 chip as described in Table 8 and Table 9.

Table 8. Pin Connection for RGB Input with HSync/Vsync

gmZAN2 Pin Name (Pin Number)	CRT Signal Name
Red+(#95)	Red
Red- (#94)	N/A (Tie to Analog GND for Red on the board)
Green+ (#91)	Green
Green- (+90)	N/A (Tie to Analog GND for Green on the board)
Blue+ (#87)	Blue
Blue- (#86)	N/A (Tie to Analog GND for Blue on the board)
HSYNC/CS (#150)	Horizontal Sync
VSYNC (#148)	Vertical Sync

Table 9. Pin Connection for RGB Input with Composite Sync

gmZAN2 Pin Name (Pin Number)	CRT Signal Name
Red+ (#95)	Red
Red- (#94)	N/A (Tie to Analog GND for Red on the board)
Green+ (#91)	Green When using Sync-On-Green this signal also carries the sync pulse.
Green- (#90)	N/A (Tie to Analog GND for Green on the board)
Blue+ (#87)	Blue
Blue- (#86)	N/A (Tie to Analog GND for Blue on the board)
HSYNC/CS (#150)	Digital composite sync. Not applicable for Sync-On-Green

The gmZAN2 chip has three ADC's (analog-to-digital converters), one for each color (red, green, and blue). Table 10 summarizes the characteristics of the ADC.

Table 10. ADC Characteristics

	MIN	TYP	MAX	NOTE
RGB Track & Hold Amplifiers				
Band Width		160 MHz		
Settling Time to 1/2 %		8.5 ns		Full Scale Input = 0.75V, BW=160MHz (*)
Full Scale Adjust Range @ R,G,B Inputs	0.60 V		0.95 V	
Full Scale Adjust Sensitivity		+/- 1 LSB		Measured @ ADC Output (**)
Zero Scale Adjust Range				For a larger DC offset from an external video source, the AC coupling feature is used to remove the offset.
Zero Scale Adjust Sensitivity		+/- 1 LSB		Measured @ ADC Output
ADC + RGB Track & Hold Amplifiers				
Sampling Frequency (fs)	20 MHz		135 MHz	
DNL			+/- 0.9 LSB	fs = 80 MHz
INL		+/- 1.5 LSB		fs = 80 MHz
Channel to Channel Matching		+/- 0.5 LSB		
Effective Number of Bits (ENOB)		7 Bits		fin = 1 MHz, fs = 80 MHz Vin= -1 db below full scale = 0.75V
Power Dissipation		400 mW		fs = 110 MHz, Vdd = 3.3V
Shut Down Current			100uA	

(*) Guaranteed by design (**) Independent of full scale R,G,B input

The gmZAN2 ADC has a built-in clamp circuit. By inserting series capacitors (about 10 nF) the DC offset of an external video source can be removed. The clamp pulse position and width are programmable.

2.3.2 Display Mode Support

A mode calculation utility (MODECALC.EXE) provided by Genesis Microchip may be run before compilation of the firmware to determine which input modes can be supported. Refer to firmware documents for more details.

2.4 Input Timing Measurement

As described in section 2.2.3 above, input data is sent from the analog-to-digital converter to the source timing generator (STG) block. The STG block defines a capture window (Figure 5).

The input timing measurement block consists of the source timing measurement (STM) block and interrupt request (IRQ) controller. Input timing parameters are measured by the STM block and stored in registers. Some input conditions will generate an IRQ to an external micro-controller. The IRQ-generating conditions are programmable.

2.4.1 Source Timing Measurement

When it receives the active CRT signal (R, G, B and Sync signals) the Source Timing Measurement unit begins measuring the horizontal and vertical timing of the incoming signal using the sync signals and TCLKi as a reference. Horizontal measurement occurs by measuring a minimum and a maximum value for each parameter to account for TCLKi sampling granularity. The measured value is updated every line. Vertical parameters are measured in terms of horizontal lines. The trailing edge of the Hsync input is used to check the polarity of the Vsync input.

The table below lists all the parameters that may be read in the source timing measurement (STM) registers of the gmZAN2.

Table 11. Input Timing Parameters Measured by the STM Block

Parameter	Unit	Updated at:
HSYNC Missing	N/A	Every 4096 TCLKs and every 80ms (2-bits)
VSYNC Missing	N/A	Every 80 ms
HSYNC / VSYNC Timing Change	N/A	When the horizontal period delta or the vertical period delta to the previous line / frame exceeds the threshhold value (programmable).
HSYNC Polarity	Positive / Negative	After register read
VSYNC Polarity	Positive / Negative	Every frame
Horizontal Period Min / Max	TCLKs and SCLKs	After register read
HSYNC High Period Min / Max	TCLKs	After register read
Vertical Period	Lines	Every frame
VSYNC High Period	Lines	Every frame
Horizontal Display Start	SCLKs	Every frame

Parameter	Unit	Updated at:
Horizontal Display End	SCLKs	Every frame
Vertical Display Start	Lines	Every frame
Vertical Display End	Lines	Every frame
Interlaced Input Detect	N/A	Every frame
CRC Data / Line Data	N/A	Every frame
CSYNC Detect	N/A	Every 80 ms

The display start / end registers store the first and the last pixels / lines of the last frame that have RGB data above a programmed threshold.

The reference point of the STM block is the same as that of the source timing generator (STG) block:

- The first pixel: the pixel whose SCLK rising edge sees the transition of the HSYNC polarity from low to high.
- The first line: the line whose HSYNC rising edge sees the transition of the VSYNC polarity from low to high.

The CRC data and the line data are used to detect a test pattern image sent to the gmZAN2 input port.

2.4.2 IRQ Controller

Some input timing conditions can cause the gmZAN2 chip to generate an IRQ. The IRQ-generating conditions are programmable, as given in the following table.

Table 12. IRQ-Generation Conditions

IRQ Event	Remark
Timing Event	One of the following three events: • Leading edge of Vsync input, • Panel line count (the line count is programmable), • Every 10 ms Only one event may be selected at a time.
Timing Change	Any of the following timing changes: • Sync loss, • DDS tracking error beyond threshold, • Horizontal / vertical timing change beyond threshold. Threshold values are programmable.

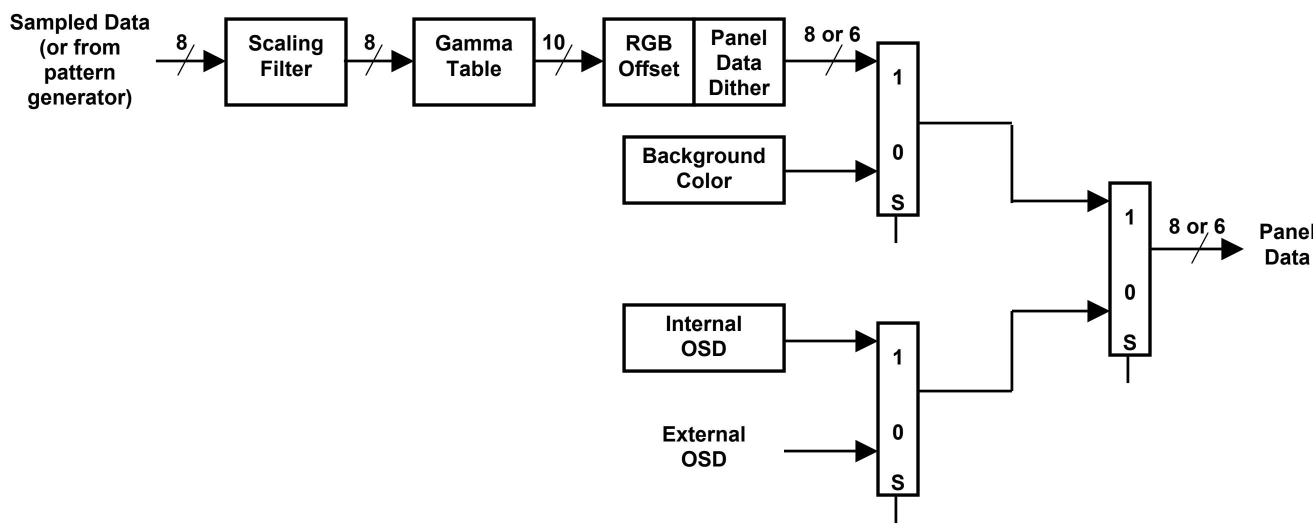
Reading the IRQ status flags will not affect the STM registers.

Note that if a new IRQ event occurs while the IRQ status register is being read, the IRQ signal will become inactive for a minimum of one TCLK period and then get re-activated. The polarity of the IRQ signal is programmable.

2.5 Data Path

The data path block of gmZAN2 is shown in Figure 6.

Figure 6. gmZAN2 Data Path



2.5.1 Scaling Filter

The gmZAN2 scaling filter uses an advanced adaptive scaling technique proprietary to Genesis Microchip Inc. and provides high-quality scaling of real time video and graphics images. This is Genesis' third generation scaling technology that benefits from the expertise and feedback gained by supporting a wide range of solutions and applications.

2.5.2 Gamma Table

The gamma table is used to adjust the RGB data for the individual display characteristics of the TFT panel. The overall gamma of the display may be set, as well as separate corrections for each of the three display channels. In addition, the gamma table may be used for contrast, brightness, and white balance (temperature) adjustments. The lookup table has an 8-bit input (256 different RGB entries) and produces a 10-bit output.

2.5.3 RGB Offset

The RGB offsets provide a simple shift (positive or negative) for each of the three color channels. This may be used as a simple brightness adjustment within a limited range. The data is clamped to zero for negative offsets, and clamped to FFh for positive offsets. This adjustment is much faster than recalculating the gamma table, and could be used with the OSD user controller to provide a quick brightness adjust. An offset range of plus 127*4 to minus 127*4 is available.

2.5.4 Panel Data Dither

For TFT panels that have fewer than eight bits for each R, G, B input, the gmZAN2 provides ordered and random dithering patterns to help smoothly shade colors on 6-bit panels.

2.5.5 Panel Background Color

A solid background color may be selected for a border around the active display area. The background color is most often set to black.

2.6 Panel Interface

The gmZAN2 chip interfaces directly with all of today's commonly used active matrix flat panels with 640x480, 800x600 and 1024x768 resolutions. The resolution and the aspect ratio are NOT limited to specific values.

2.6.1 TFT Panel Interface Timing Specification

The TFT panel interface timing parameters are listed in Table 13 below. Refer to the three timing diagrams of Figure 7 and Figure 8 for the timing parameter definition. All aspects of the gmZAN2 interface are programmable. For horizontal parameters, Horizontal Display Enable Start, Horizontal Display Enable End, Horizontal Sync Start and Horizontal Sync End are programmable. Vertical Display Enable Start, Vertical Display Enable End, Vertical Sync Start and Vertical Sync End are also fully programmable. In order to maximize panel data setup and hold time, the panel clock (PCLKA, PCLKB) output skew is programmable. In addition, the current drive strength of the panel interface pins is programmable.

Table 13. gmZAN2 TFT Panel Interface Timing

Signal Name			min	Typical	Max	unit
PVS	Period	t1	0	 16.67	2048 -	lines ms
	Frequency			60	-	Hz
	front porch	t2	0		2048	lines
	back porch	t3	0		2048	lines
	pulse width	t4	0		2048	lines
	PdispE	t5	0	Panel height	2048	lines
	Disp. start from VS	t6	0		2048	lines
	PVS set up to PHS	t18	1		2048	PCLK *1
	PVS hold from PHS	t19	1		2048	PCLK *1
PHS	Period	t7	0		2048 [1024]	PCLK *1
	front porch	t8	0		2048	PCLK *1
	back porch	t9	0		2048	PCLK *1
	pulse width	t10	0		2048	PCLK *1
	PdispE	t11	0	Panel width	2048 [1024]	PCLK *1
	Disp. start from HS	t12	0		2048	PCLK *1
PCLKA, PCLKB*4	Frequency	t13			120 [60]	MHz
	Clock (H) *2	t14	DCLK/2 - 3 [DCLK - 3]		DCLK/2 - 2 [DCLK - 2]	ns
	Clock (L) *2	t15	DCLK/2 - 3 [DCLK - 3]		DCLK/2 - 2 [DCLK - 2]	ns
	Type		-	One pxl/clock [two pxl/clock]	-	
Data	set up *3	t16	DCLK/2 - 5 [DCLK - 5]		DCLK/2 - 2 [DCLK - 2]	ns
	hold *3	t17	DCLK/2 - 5 [DCLK - 5]		DCLK/2 - 2 [DCLK - 2]	ns
	Width		3 bits	18bits [36 bits]	24bits [48bits]	bits/pixel

NOTE: Numbers in [ ] are for two pixels/clock mode.

NOTE: The drive current of the panel interface signals is programmable as shown in Table 1 on page 4. The drive current is to be programmed through the API upon chip initialization. Output current is programmable from 2 mA to 20 mA in increments of 2 mA. Drive strength should be programmed to match the load presented by the cable and input of the panel. Values shown are based on a loading of 20 pF and a drive strength of 8 mA.

NOTE *1:The PCLK is the panel shift clock.

NOTE *2: The DCLK stands for Destination Clock (DCLK) period. is equal to:
- PCLK period in one pixel/clock mode,
- twice the PCLK period in two pixels/clock mode.

NOTE *3: The setup/hold time spec. for PCLK also applies to PHS and PDispE. The setup time (t16) and the hold time (t17) listed in this table are for the case in which no clock-to-data skew is added. The PVS/PHS/ PDispE/PData signals are asserted on the rising edge of the PCLK. The polarity of the PCLK and its skew are programmable. Clock to Data skew can be adjusted in sixteen 800-ps increments. In combination with the PCLK polarity inversion, the clock-to-data phase can be adjusted in total of 31 steps.

NOTE *4: The polarity of the PCLKA and the PCLKB are independently programmable.

The microcontroller must have all the timing parameters of the panel used for the monitor. The parameters are to be stored in a non-volatile memory. As can be seen from this table, the wide range of timing programmability of the gmZAN2 panel interface makes it possible to support various kinds of panels known today.

Figure 7. Timing Diagrams of the TFT Panel Interface (one pixel per clock)

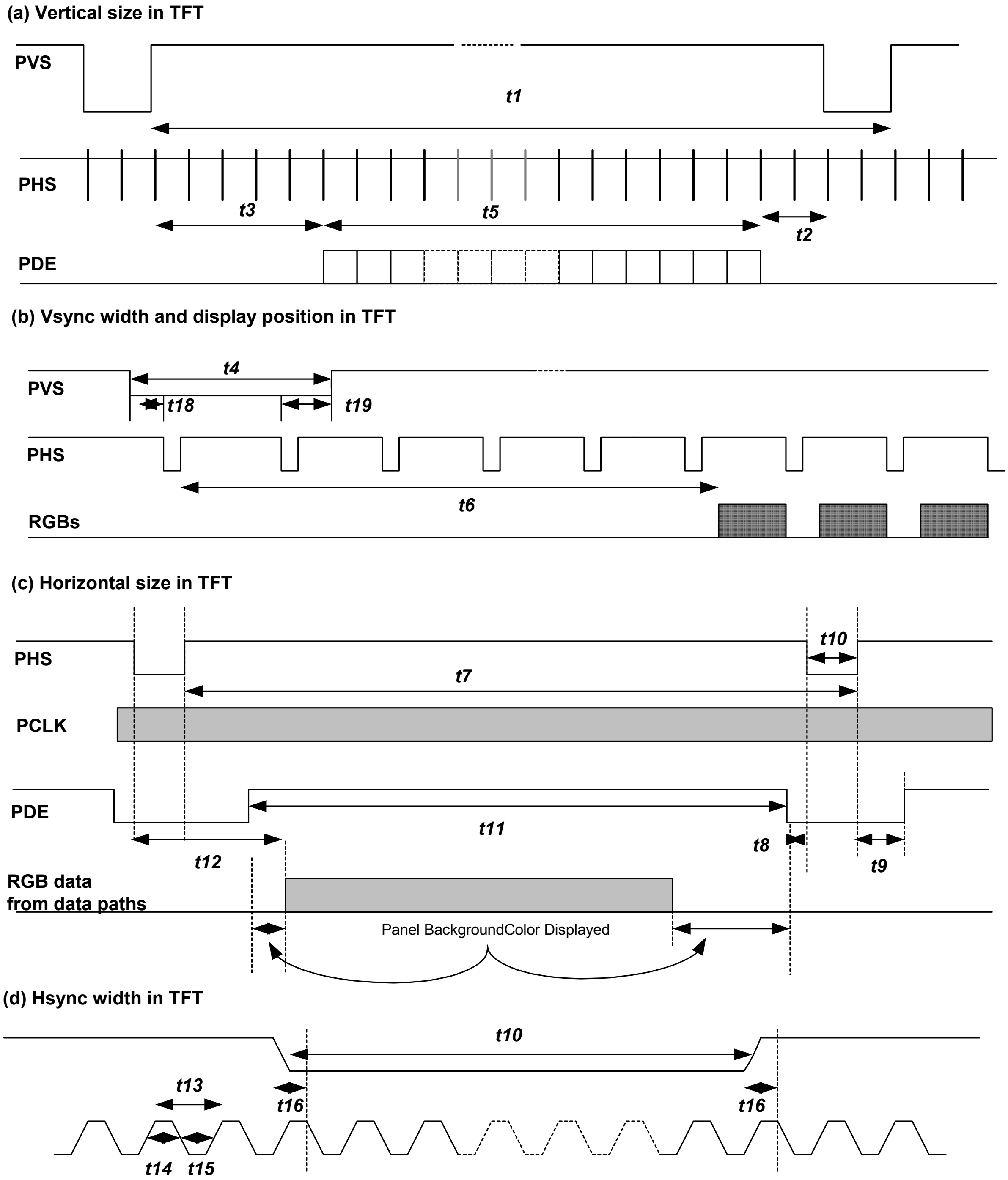
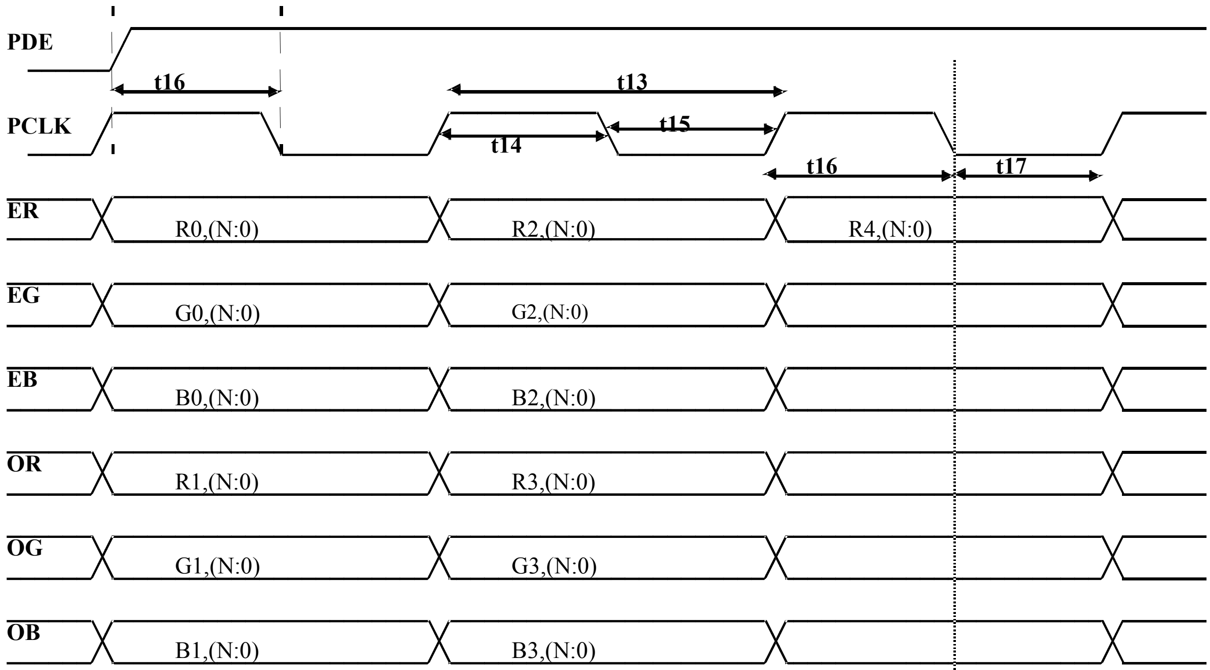
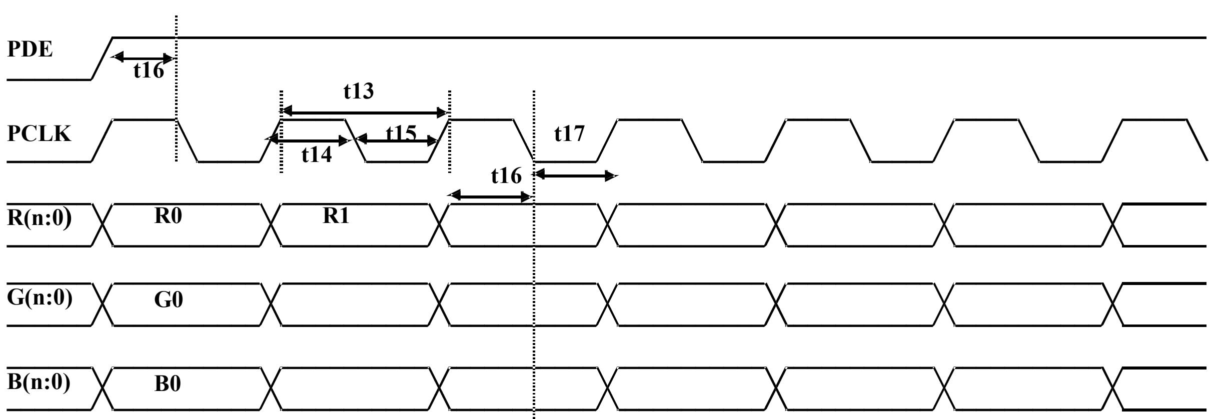


Figure 8. Data latch timing of the TFT Panel Interface

(a) Two pixel per clock mode in TFT



(b) One pixel per clock mode in TFT



2.6.2 Power Manager

LCD panels require logic power, panel bias power, and control signals to be sequenced in a specific order, otherwise severe damage may occur and disable the panel permanently. The gmZAN2 has a built-in power sequencer (Power Manager) that prevents this kind of damage.

The Power Manager controls the power up/down sequences for LCD panels within the four states described below. See the timing diagram Figure 9.

2.6.2.1 State 0 (Power Off)

The Pbias signal and Ppower signal are low (inactive). The panel controls and data are forced low. This is the final state in the power down sequence. PM is kept in state 0 until the panel is enabled.

2.6.2.2 State 1 (Power On)

Intermediate step 1. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is forced low (inactive).

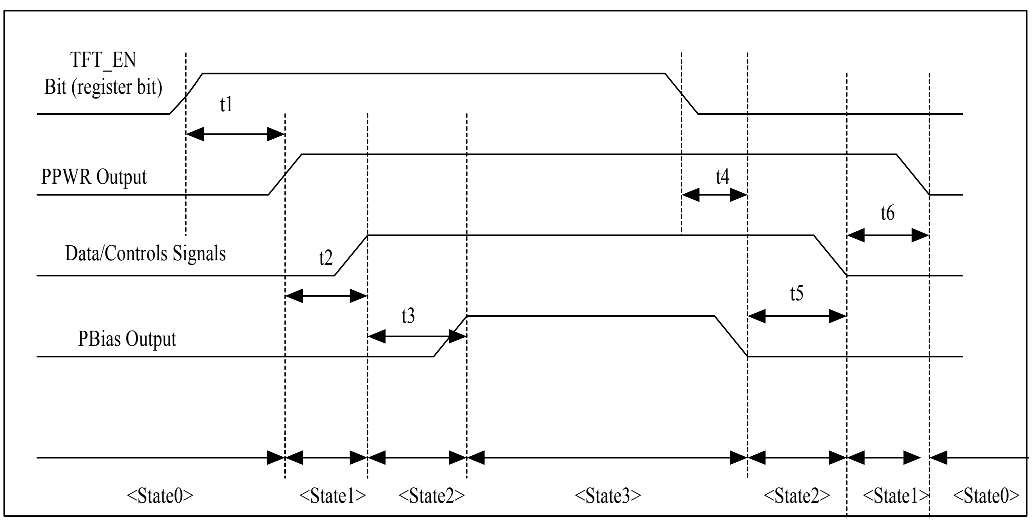
2.6.2.3 State 2 (Panel Drive Enabled)

Intermediate step 2. The Ppower is high (active), the Pbias is low (inactive), and the panel interface is active.

2.6.2.4 State 3 (Panel Fully Active)

This is the final step in the power up sequence, with Ppower and Pbias high (active), and the panel interface active. PM is kept in this state until the internal TFT_Enable signal controlled by Panel Control register is disabled. The panel can be disabled through either an API call under program control or automatically by the gmZAN2 to prevent damage to the panel.

Figure 9. Panel Power Sequence



In Figure 9 above, t2=t6 and t3=t5. t1, t2, t3 and t4 are independently programmable from one to eight steps in length. The length of each step is in the range of 511 * X * (TCLKi cycle) or (TCLKi cycle) * 32193 * X, where X is any positive integer value equal to or less than 256. TCLKi is the reference clock to the gmZAN2 chip, and ranges from 14.318 MHz to 50 MHz in frequency. This programmability provides enough flexibility to meet a wide range of power sequencing requirements by various panels.

2.6.3 Energy Spectrum Management (ESM)

High spikes in the electromagnetic interference (EMI) power spectrum can cause LCD monitor products to violate emissions standards. The Energy Spectrum Management in the gmZAN2 uses the following features to reduce EMI:

- ESM Clock Control
- Programmable Panel Interface Drive strength

These features eliminate the costs associated with EMI-reducing components and shielding. In particular, the use of parallel-to-serial transmitter and serial-to-parallel receiver devices may not be necessary.

2.6.4 Panel Interface Drive Strength

As mentioned previously, the gmZAN2 has programmable output pads for the TFT panel interface. Three groups of panel interface pads (panel clock, data, and control) are independently controllable and are programmable.

Table 14. Panel Interface Pad Drive Strength

Value (4 bits)	Drive Strength in mA
0	Outputs are in tri-state condition
1	2 mA
2	4 mA
3	6 mA
4	8 mA
5	10 mA
6	12 mA
7	14 mA
8	16 mA
9	18 mA
10,11,12,13,14,15	20 mA

2.7 Host Interface

The host microcontroller interface of the gmZAN2 has two modes of operation, a serial interface data transfer mode and a 4-bit parallel interface mode.

- Serial interface data transfer mode - Four signals consisting of 1 data bit, a frame synchronization signal, a clock signal and an Interrupt Request signal (IRQ). This mode is entered when a pull-down resistor is not connected to MFB6 (pin number 106).
- 4-bit parallel interface mode – Three additional data bits are used so that four data bits are transferred on each clock edge. The 4-bit port uses MFB [9:7] as HDATA [3:1] and HDATA is used as HDATA0. The HFS and HCLK are used to control the data transfers. This mode is entered when a pull-down resistor (10K ohm) is connected from MFB6 (pin number 106) to ground.

The host interface mode is selected when the gmZAN2's reset is asserted by sampling the state of MFB6 (pin number 106).

The gmZAN2 chip has an on-chip, pull-down resistor in the HFS input pad. The signal stays low until driven high by the microcontroller.

The burst mode operation then uses three clocks (instead of twelve) for each 12-bit data (or address) transmission.

In both modes, a reset pin sets the chip to a known state when the pin is pulled low. The RESETn pin must be low for at least 100ns after the CVDD has become stable (between +2.4V and +2.75V) or until the oscillator used is stable or whichever takes longer in order to reset the chip to a known state.

2.7.1 Serial Communication Protocol

In the serial communication between the microcontroller and the gmZAN2, the microcontroller always acts as an initiator while the gmZAN2 is always the target. The following timing diagram describes the protocol of the serial channel of the gmZAN2 chip. In the read operation, the microcontroller (Initiator) issues an instruction lasting 12 HCLKs. After the last bit of the command is transferred to the gmZAN2, on the 12th clock, the microcontroller must stop driving data before the next rising edge of HCLK at which point the gmZAN2 will start driving data at the 13th rising edge of HCLK.

Figure 10. Timing Diagram of the gmZAN2 Serial Communication

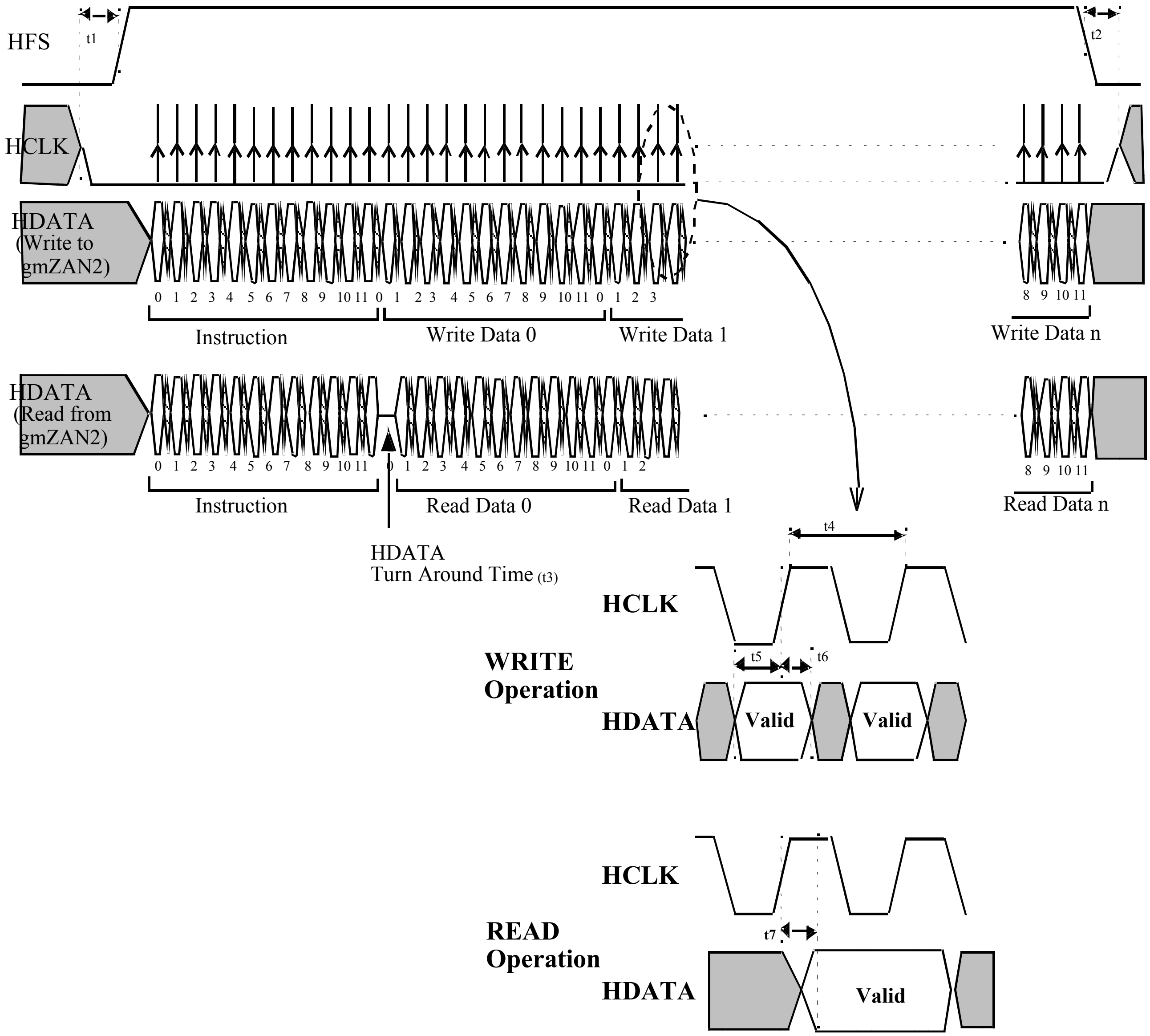


Table 15 summarizes the serial channel specification of the gmZAN2. Refer to Figure 10 for the timing parameter definition.

Table 15. gmZAN2 Serial Channel Specification

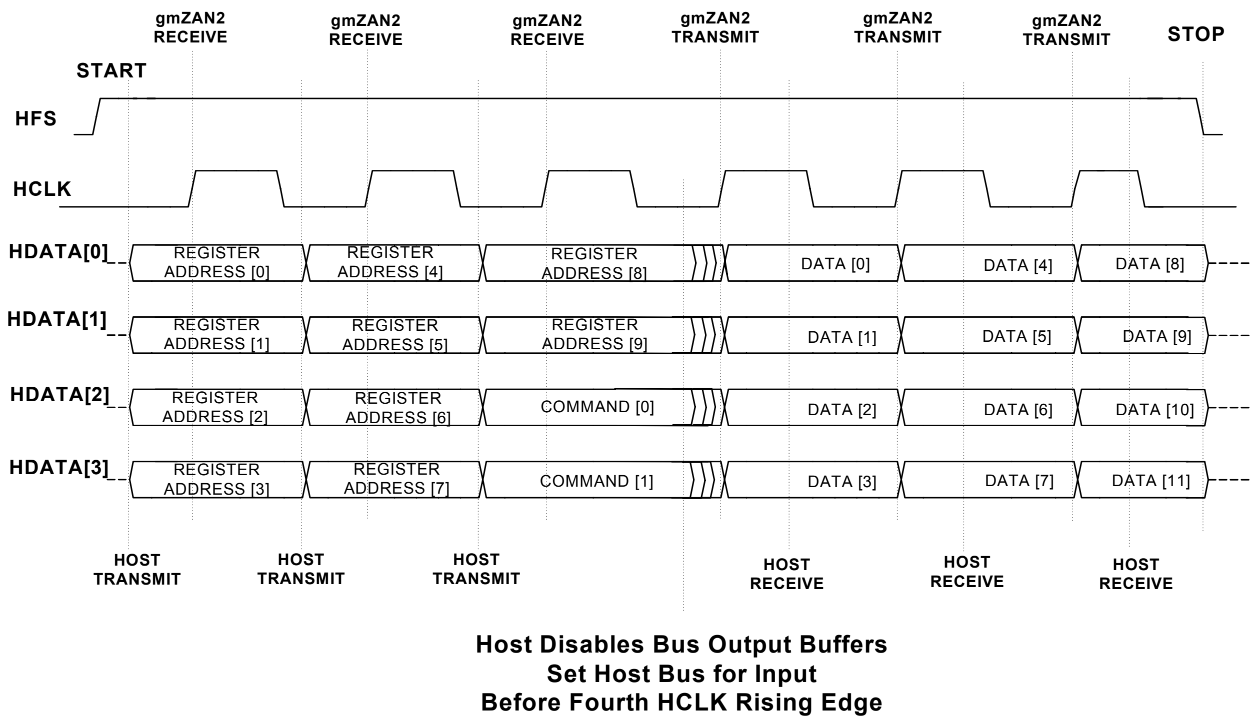
Parameter	min.	typ.	max.
Word Size (Instruction and Data)	---	12 bits	---
HCLK low to HFS high (t1)	100 ns		
HFS low to HCLK inactive (t2)	100 ns		
HDATA Write to Read Turnaround Time (t3)	1 HCLK cycle		1 HCLK cycle
HCLK cycle (t4)	100 ns		
Data in setup time (t5)	25 ns		
Data in hold time (t6)	25 ns		
Data out valid (t7)	5 ns		10

2.7.2 Four bit Parallel Host interface

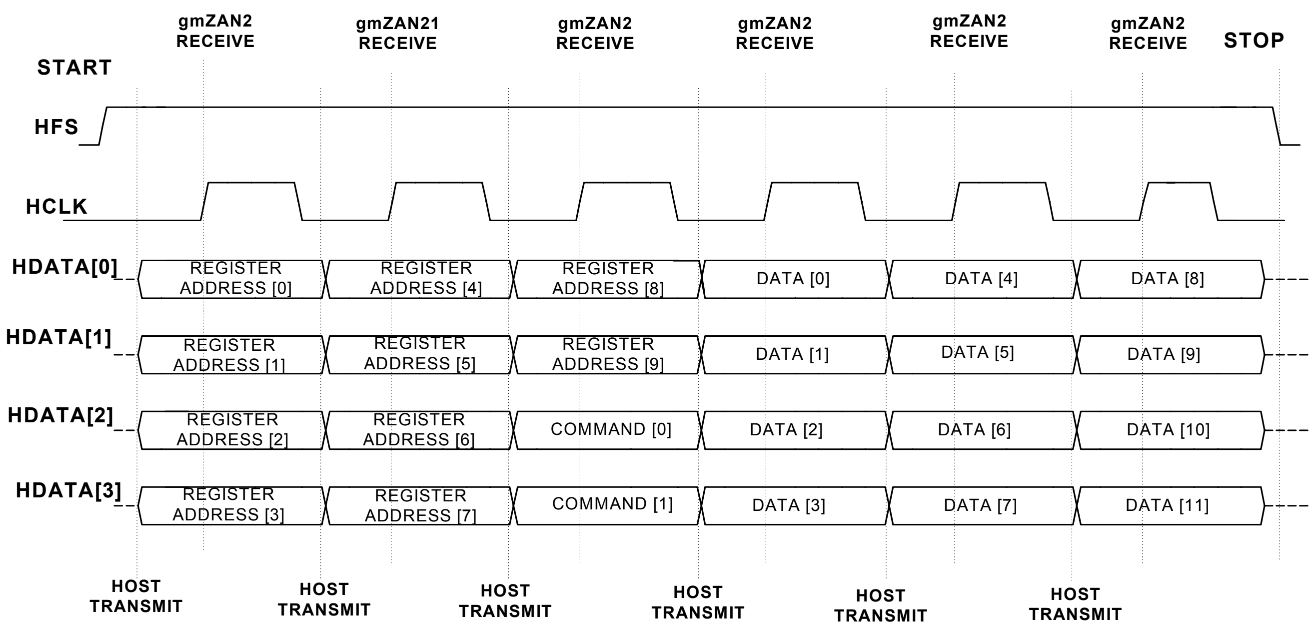
When the chip is configured for a 4-bit host interface, MFB[9:7] are used as HDATA[3:1] and HDATA is used as HDATA0. The command and address information are transferred as Address3:0 and Address7:4, and Command1:0 + Address9:8. The data information is transferred as Data3:0, Data7:4, Data11:8. The following diagrams illustrate the four-bit parallel read and write protocol. This is also referred to as the 6-wire mode.

Figure 11. Timing diagram for read/write using 4-bit Parallel Host Interface

Reading from gmZAN2



Writing to gmZAN2



2.7.3 Multi-Function Bus (MFB)

The Multi-Function Bus provides 12 additional pins that are used as general purpose input and output (GPIO) pins. Each pin can be independently configured as input or output.

MFB pins 9 through 5 have special functions:

- When a 10K ohm, pull-down resistor is connected to MFB6 (MFB6 has an internal pull-up resistor) MFB9:7 are used as host data bits HDATA3:1.
- When a 10K ohm, pull-down resistor is connected to MFB5 (MFB5 has an internal pull-up resistor) a crystal can be placed between XTAL and TCLK instead of using an external oscillator for the TCLK input.

Note that all pins on the multi-function bus MFB11:0 are internally pulled-up.

2.8 On-Screen Display Control

The gmZAN2 chip has a built-in OSD (On-Screen Display) controller with an integrated font ROM. The chip also supports an external OSD controller for monitor vendors to maintain a familiar user interface.

The internal and external OSD windows may be displayed anywhere the panel Display Enable is active, regardless of whether the panel would otherwise display panel background color or active data.

2.8.1 OSD Color Map

Both the internal and external OSD display use a 16-location SRAM block for the color programming. Each color location is a twelve-bit value that defines the upper four bits of each of the 8 bit Red, Blue and Green color components as follows:

- D3:0 Blue; D7:4 of blue component of color
- D7:4 Green; D7:4 of green component of color
- D11:8 Red; D7:4 of red component of color

To extend the 4-bit color value programmed to the full 8 bits, the following rule is applied: if any of the upper four color bits is a “1”, then R (G, B) data 3:0 = 1111b; otherwise R (G, B) data 3:0 = 0000b.

2.8.2 On-Chip OSD Controller

The internal OSD uses a block of SRAM of 1536x12 bits and a ROM of 1024x12 bits. The SRAM is used for both the font data and the character-codes while the ROM is used to store the bit data for 56 commonly used characters. The font data is for 12 pixel x 18 line characters, one bit per pixel. The font data starts at address zero. The character-codes start at any offset (with an address resolution of 16) that is greater than the last location at which font data has been written. It is the programmer’s responsibility to ensure that there is no overlap between fonts and character-codes. This implementation results in a trade-off between the number of unique fonts on-screen at any one time and the total number of characters displayed. For example, one configuration would be 98 font maps (56 fonts in ROM and 42 fonts in SRAM) and 768 characters (e.g. in a 24x32 array).

The on-chip OSD of the gmZAN2 can support a portrait mode (in which the LCD monitor screen is rotated 90 degrees). **In this portrait mode, all the fonts must be loaded in the SRAM, because the ROM stores fonts for a landscape mode (typical orientation) only**. The font size in the portrait mode is 12 pixels by 12 lines. As is the case in landscape mode, the SRAM is divided into a font storage area and a character code storage area. For example, 64 fonts can be stored in RAM and an OSD window of 768 characters (such as 24 x 32) can still be displayed.

The first address of SRAM to be read for the first character displayed (upper left corner of window) is also programmable, with an address resolution of 16 (8-bits as the top bits of the 12-bit SRAM address). The character-code is a 12-bit value used as follows:

- D6:0 font-map select, this is the top seven bits of the address for the first line of font bits
- D8:7 Background color, 00=bcolor0, 01=bcolor1, 10=bcolor2, 11=transparent background
- D10:9 Foreground color (0, 1, 2 or 3)
- D11 Blink enable if set to 1, otherwise no blink

Although the OSD color map has room for sixteen colors, only seven are used by the internal OSD: three background colors and four foreground colors.

The blink rate is based on either a 32 or 64 frame cycle and the duty cycle may be selected as 25/75 50/50% or 75/25%. The 2-bit foreground and background attributes directly select the color (there is no indirect “look-up”, i.e. there is no TMASK function). The 2560 addresses of the ROM/SRAM are mapped as 10 segments of 256 contiguous addresses each, to the OSD memory page of 100h – 1FFh in the host interface. A 4-bit register value selects the segment to map to the host R/W page.

The character cell height and width are programmable from 5-66 pixels or 2-65 lines. The X/Y offset of the font bit-map upper-left pixel relative to the upper-left pixel of the character cell is also programmable from 0-63 (pixels or lines). The OSD window height and width in characters/rows is programmable from 1-64.

The Start X/Y position for the upper left corner of the OSD window is programmable (in panel pixels and lines) from 0- 2047. There is an optional window border (equal width on all four sides of the window) or a window shadow (the window bottom and right side) the border is a solid color that is selected by an SRAM location as RGB444. The border width may be set as 1, 2, 4 or 8 pixels/lines. These parameters are summarized in Figure 12 and Table 16.

The Font Data D11:0 for each line is displayed with bit D11 first (leftmost) and D0 last.

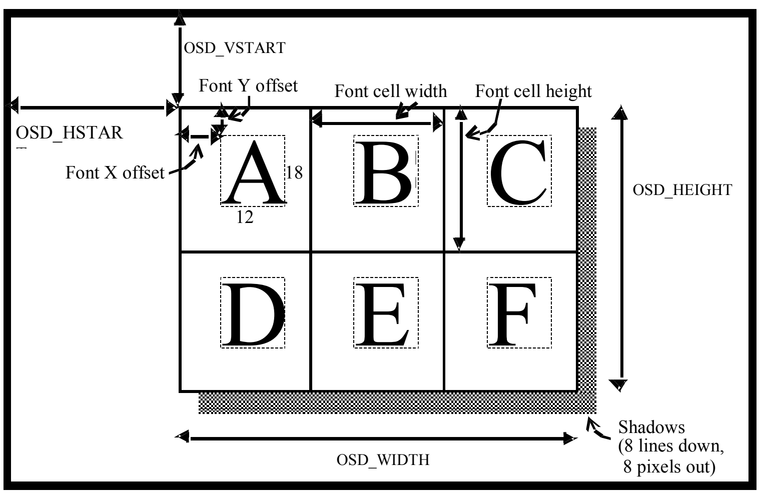
The reference point for the OSD start is always the upper left corner of the Panel display, which is the start (leading edge) of Panel Display Enable for both Horizontal and Vertical timing.

The OSD Window start position sets the location of the first pixel of the OSD to display, including any border. That is, if the border is enabled, the start of the character display of the OSD is offset from the OSD start position by the width/height of the border.

To improve the appearance and make it easy to find the OSD window on the screen, the user may select optional shadowing (3D effect). The “Shadow” feature operates in the same manner as in the gmZAN1; that is, it produces a region of half intensity (scaler data) pixels of the same width and height as the OSD window, but offset to the right and down by 8 pixels/lines (the border width setting has no effect). OSD foreground and background colors always cover the OSD window region of the “shadow”, but transparent background pixels in the OSD will show the half intensity panel data. Therefore, it is not recommended to use both the “shadow” feature and transparent background OSD pixels together. The “shadow” does **not** change the intensity of any panel background color over which it may be located. The border and shadow are mutually exclusive, only one may be selected at a time.

The OSD window is not affected by the scaling operation. The size will stay the same whether the source input data is scaled or not.

Figure 12. On-Chip OSD Window Location



OSD_HSTART: Starting pixel number 0-2047

OSD_VSTART: Starting line number 0-2047

Font X offset: Location of left pixel of font inside cell 0-63

Font Y offset: Location of top line of font inside cell 0-63

Font Cell Width: Cell width in pixels 5-66

Font Cell Height: Cell height in lines 2-65

OSD_Width: OSD Window Width in char cells 1-64

OSD_Height: OSD Window Height in char cells 1-64

OSD_Width x OSD_Height <= 32
(1x32, 2x16, 3x10, 4x8, 5x5, 6x5, etc.)

Font size = 12 pixels x 18 scanlines

Table 16. Programmability of On-chip OSD Locations

Parameter	Range	Reference Point
OSD Window Horizontal Start Position	0 ~ 2047 pixels	End-of-line pulse (internal signal)
OSD Window Vertical Start Position	0 ~ 2047 scanlines	End-of-frame pulse (internal signal)
Font X Offset	0 ~ 63 pixels	Upper-left corner of a screen location
Font Y Offset	0 ~ 63 scanlines	Upper-left corner of a screen location
Font Cell Width	5 ~ 66 pixels	
Font Cell Height	2 ~ 65 lines	
OSD Window Width	1 ~ 64 characters	
OSD Window Height	1 ~ 64 characters	
OSD Window Width x OSD Window Height	0 ~ 32 character locations (rectangle or square)	
Font Size	12 pixels wide x 16 scanlines high	

There is no hardware cursor supported. Character blinking can be done by changing the foreground and background colors in the character attribute table.

On-chip OSD as well as external OSD is controlled through the API calls. The external OSD is explained in section 2.8.4.

2.8.3 Built-in OSD Fonts

To minimize external memory requirements, the gmZAN2 has a set of commonly used characters stored on an on-chip ROM. The ROM contains bit data for the fonts shown in Figure 13. These are the set of alphanumeric characters minus the upper and lower case Q, W and Y.

Figure 13. Built-in OSD Fonts

Index	Font	Index	Font	Index	Font	Index	Font
00	0	10	G	20	Z	30	p
01	1	11	H	21	a	31	r
02	2	12	I	22	b	32	s
03	3	13	J	23	c	33	t
04	4	14	K	24	d	34	u
05	5	15	L	25	e	35	v
06	6	16	M	26	f	36	x
07	7	17	N	27	g	37	z
08	8	18	O	28	h	38	W *
09	9	19	P	29	i	39	N/A
0A	A	1A	R	2A	j	3A	N/A
0B	B	1B	S	2B	k	3B	N/A
0C	C	1C	T	2C	l	3C	N/A
0D	D	1D	U	2D	m	3D	N/A
0E	E	1E	V	2E	n	3E	N/A
0F	F	1F	X	2F	o	3F	N/A

* Last two lines overlap into SRAM and must be cleared to use this character.

2.8.4 External OSD Support

The gmZAN2 supports an external OSD controller for monitor vendors who wish to maintain a specific user interface, or the look and feel consistent with some previous device. Only those OSD controllers that are developed for a flat-panel monitor application and have a pixel-clock input pin are supported. As is the case with an on-chip OSD, the OSD window size is not affected by scaling.

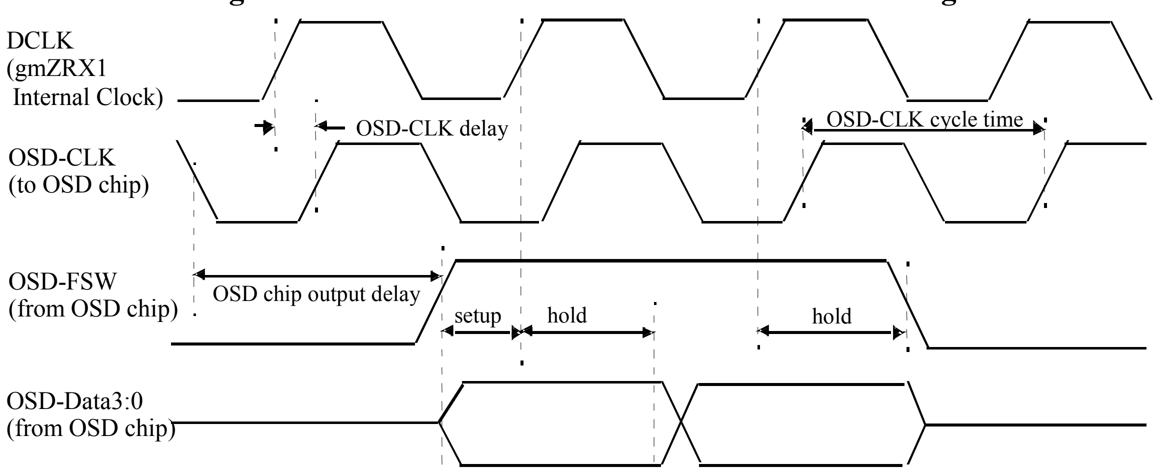
An external OSD controller is connected to the gmZAN2 chip as shown in Table 17.

Table 17. Pin Connection Between the gmZAN2 and an External OSD controller

gmZAN2 Pin Name (Pin#, in/out)	External OSD Controller Pin (in/out)	Polarity	Position
OSD-HREF (#115, output)	HSync (input)	Programmable	Active during horizontal blanking period.
OSD-VREF (#116, output)	VSync (input)	Programmable	Active during vertical blanking period.
OSD-CLK (#117, output)	Pixel Clock (input)		
OSD-FSW (#122, input)	OSD Window Indicator (output)	Programmable	Horizontal: M OSD-CLK cycles after the HREF for N pixels. Vertical: M' HREF pulses after the VREF for N' lines (M, N, M',N' programmed to external OSD chip)
OSD-DATA[3:0] (#118~#121, inputs)	Intensity, R, G, and B (outputs)		

The four-bit data from an external OSD controller becomes one of the 16 entries to the OSD look-up table (LUT), which is 12 bits wide (4 bits/color).

Figure 14. External OSD Interface Data Latch Timing



OSD-CLK delay = 3 ns default. Additional 0 ~ 12 ns delay can be added.

OSD-FSW/OSD-DATA setup/hold time = 1.5 ns min.

OSD-CLK cycle time = 80 MHz max.

When the external OSD controller interface is enabled, data from the OSD LUT is displayed on a TFT panel instead of the ADC output whenever the OSD-FSW signal is active.

The OSD-CLK output to an external OSD controller chip is derived from the DCLK (destination clock) whose clock frequency is the same as the panel clock in frequency (or twice the panel clock frequency on a two-pixels-per-clock panel). The maximum frequency is 80MHz.

Both the OSD Data and OSD-FSW signals are latched by gmZAN2 on the rising edge of the DCLK. To maximize the setup/ hold time for the OSD-Data and OSD-FSW signal, a delay of up to 6 ns can be added to the OSD-CLK.

Table 18. External OSD Interface Timing Parameters

Parameter	minimum	typical	maximum
OSD-CLK Frequency			80 MHz
OSD-FSW/OSD-DATA setup time	1.5 ns		
OSD-FSW/OSD-DATA hold time	1.5 ns		
OSD-CLK delay from DCLK		0 ~ 5.6 ns, programmable in 800-ps increment	
OSD-HREF delay from DCLK		0 ~ 12 ns, programmable in 800-ps increment	
OSD-CLK/DCLK ratio		1/4x, 1/2x, 1x, programmable	

The external-OSD window position is referenced to the edge of the OSD-HREF and OSD-VREF. The horizontal start position is defined in terms of OSD-CLK pulse counts. The vertical position is defined in terms of OSD-HREF pulse counts. These values must be programmed into an external OSD controller chip.

The trailing edge of OSD-HREF and OSD-VREF are always positioned at the beginning of a display period. Thus, the external OSD window position will stay at the same place regardless of input resolution and refresh rate.

Enabling and configuring the external OSD interface and writing to the OSD LUT is achieved using API calls.

2.9 On-chip TCLK Oscillator

The gmZAN2 on-chip TCLK oscillator circuitry is a custom-designed circuit that supports the use of an external oscillator or an external crystal resonator to generate a reference frequency source for the gmZAN2 device. When used with an external crystal resonator, the oscillator circuit provides a very low jitter and very low harmonic clock to the internal circuitry of the gmZAN2. The on-chip oscillator circuit also minimizes the overdrive of the crystal, which reduces the aging of the crystal.

The requirements for the TCLK signal are shown below.

Table 19. TCLK Specification

Frequency	20 MHz to 50 MHz
Jitter	250 ps maximum
Rise Time (10% to 90%)	5 ns
Duty Cycle	40-60

2.9.1 External Oscillator mode

The first mode of operation of the TCLK circuitry is the external oscillator mode. When the gmZAN2 is in reset, the state of the MFB5 (pin 107) is sampled. If the pin is pulled high to Vdd (there is an internal 60K Ohm pull up resistor on this pin) the external oscillator mode is enabled.

In this mode the internal oscillator circuit is disabled and the external oscillator signal that is connected to the TCLK (pin 141) is routed to an internal clock buffer as shown in figure 15.

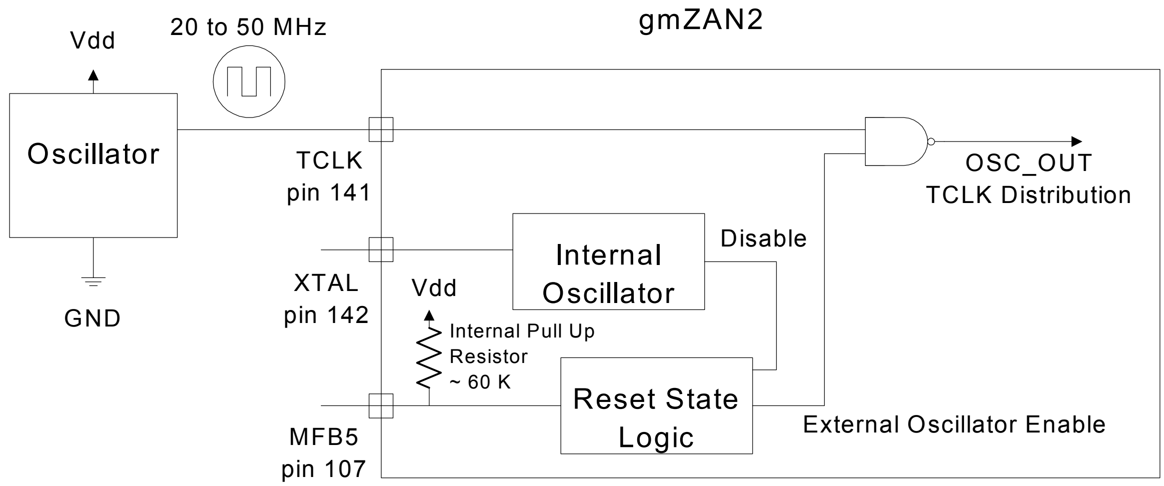


Figure 15. Using an External Oscillator

2.9.2 Internal Oscillator mode

The second mode of operation for the TCLK circuitry is the internal oscillator mode. When the gmZAN2 is in reset, the state of the pin MFB5 (pin 107) is sampled. If the pin is pulled low by connecting the pin directly to GND, or by connecting the pin to GND through a pull down resistor, the internal oscillator is enabled. The maximum value of the pull down resistor is 15K Ohm. In this mode, an external crystal resonator is connected between the XTAL (pin 142) and the TCLK (pin 141) with the appropriately sized loading capacitors C_{L1} and C_{L2}. The sizes of C_{L1} and C_{L2} are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the gmZAN2 device and the printed circuit board traces. The loading capacitors are terminated to the Vdda power supply. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to ground.

The oscillator circuit is a Pierce Oscillator circuit and a simplified schematic is shown in Figure 16. The output of the oscillator circuit, measured at the TCLK (pin 141), is an approximate sine wave with a bias of about 2 volts above ground (see Figure 17). The peak-to-peak voltage of the output can range from 250 mV to 1000 mV depending on the specific characteristics of the external crystal used and variation in the oscillator characteristics. The output of the oscillator is connected to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50mV peak-to-peak to function correctly. The output of the comparator is buffered and is then distributed to the gmZAN2 circuits.

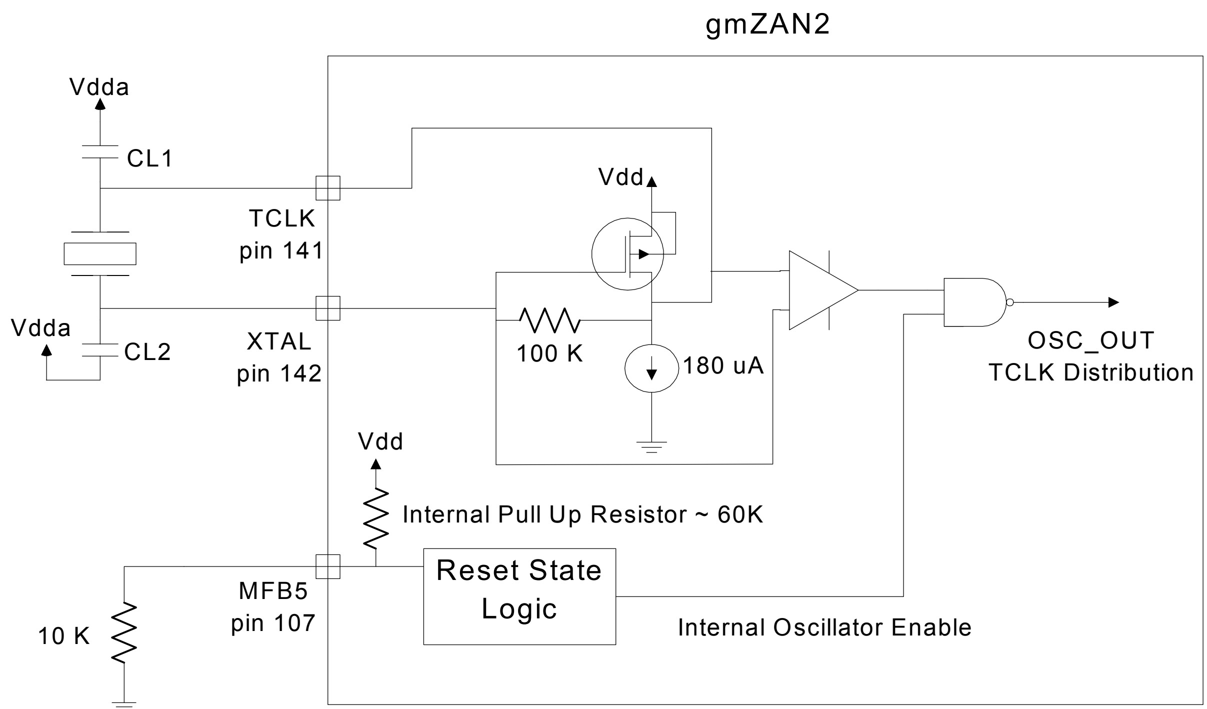


Figure 16. Using an Internal Oscillator

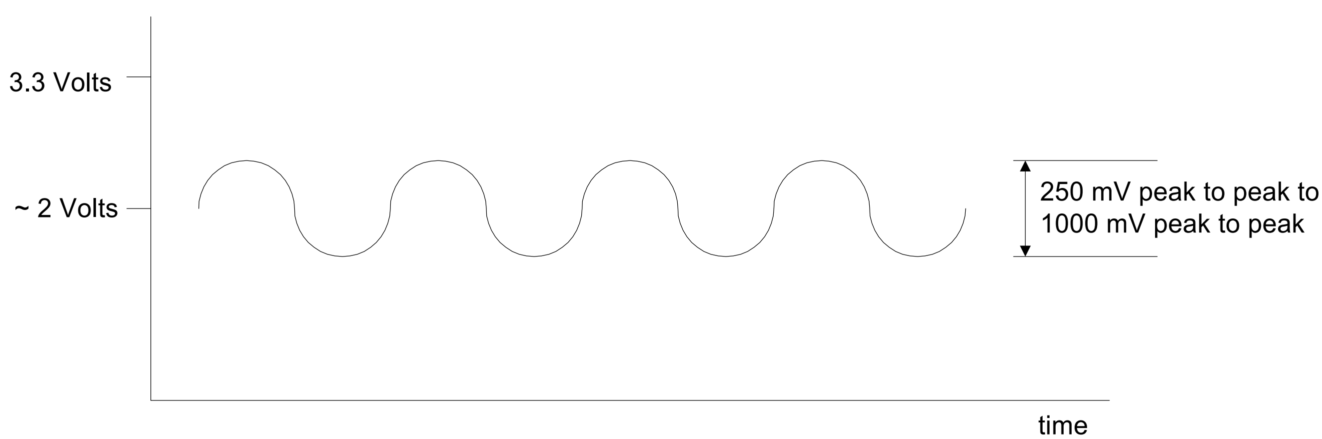


Figure 17. Internal Oscillator output at TCLK

One of the design parameters that must be given some consideration is the value of the loading capacitors used with the crystal.

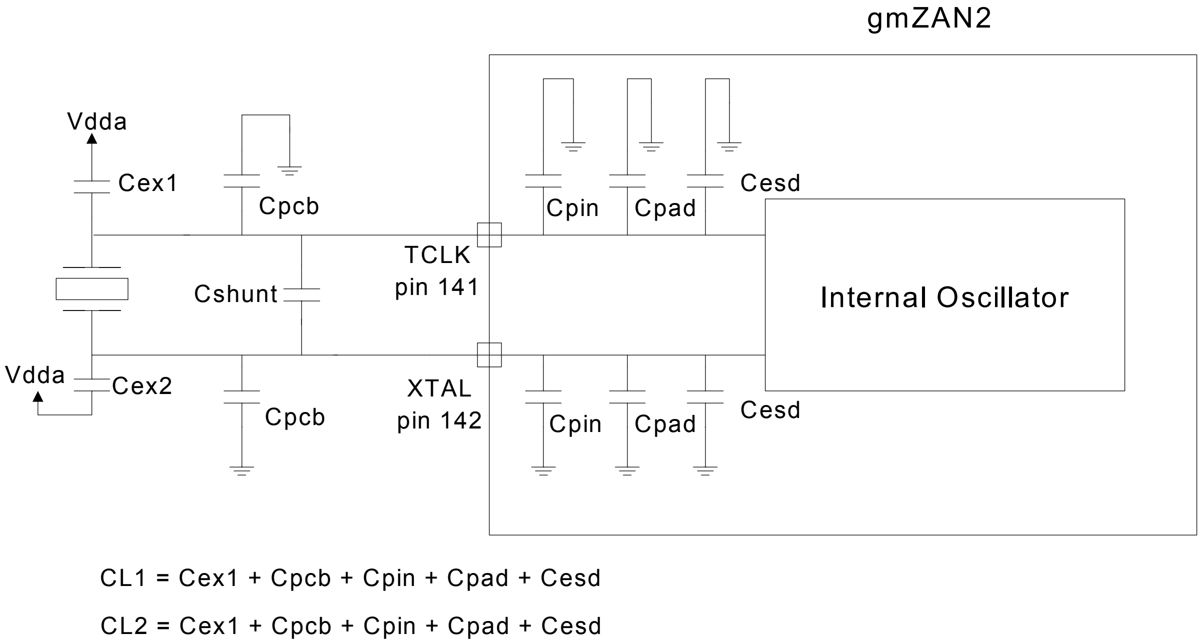


Figure 18. Parasitic Capacitance Sources

The loading capacitance (C_{load}) on the external crystal is the combination of C_{L1} and C_{L2} and is calculated by: $C_{load} = ((C_{L1} * C_{L2}) / (C_{L1} + C_{L2})) + C_{shunt}$.

The shunt capacitance C_{shunt} is the effective capacitance between the XTAL and TCLK pins. For the gmZAN2 this is approximately 9 pF.

C_{L1} and C_{L2} are a parallel combination of the external loading capacitors (C_{ex}), the PCB board capacitance (C_{PCB}), the pin capacitance (C_{pin}), the pad capacitance (C_{pad}), and the ESD protection capacitance (C_{ESD}). The capacitances are symmetrical so that $C_{L1} = C_{L2} = C_{ex} + C_{PCB} + C_{pin} + C_{pad} + C_{ESD}$ The correct value of C_{ex} must be calculated given the value of the parasitics.

C_{PCB} ~ Layout dependent. Approximately 2 pF to 10 pF

C_{pin} ~ 1.1 pF

C_{pad} ~ 1 pF

C_{ESD} ~ 5.3 pF

C_{shunt} ~ 9 pF

Some attention must be given to the details of the oscillator circuit when used with an external crystal resonator. The value of C_{load} that is specified by the manufacturer should not be exceeded because of potential start up problems with the oscillator. Additionally, the external crystal used should be a parallel resonate cut and the value of the equivalent series resistance must be less than 90 Ohms.

2.10 Sleep Mode Power Down

Recent energy efficiency requirements, based on various standards, specify a low power standby mode when the monitor is not in use. To support these standards, the gmZAN2 incorporates control bits that provides selective disabling of the core modules in the gmZAN2 This is under firmware control. The selective enabling and disabling of the various cores give the firmware designer the flexibility to adjust the power consumption of the gmZAN2 device based on the task required.

Power consumption in a CMOS device is the sum of the leakage currents plus switching currents of the logic. If all the logic switching is stopped, the current consumption of the gmZAN2 is reduced to a few milli-amperes which is being used for the analog inputs. The philosophy for the gmZAN2 sleep mode programming is to turn off all possible sources of switching logic when no video signal is present.

The gmZAN2 is configured for sleep mode operation by a register programming sequence that disables the SCLK, DCLK PLL's, turning off the ADC, the panel drivers and establishing other conditions to minimize the power consumption of the gmZAN2. The register programming sequence is to disable the high frequency clocks and places the remaining logic into a state that minimizes any logic switching. In this condition, only the TCLK is running with the Source Timing Measurement (STM) logic active (Registers 0x60 to 0x7F), and the gmZAN2 can be polled for input signal activity to determine when to exit the standby mode. For more detailed information on this programming sequence please refer to Appendix A of the gmZAN2 Register Programming Guide.

Sleep Mode Current Specification: Register programming as specified in the Appendix A of the gmZAN2 Register Programming Guide.	
TCLK Frequency	Sleep Mode Current
50 MHz	< 40 mA
14.3 MHz	< 10 mA
0 MHz	< 5 mA

3. ELECTRICAL CHARACTERISTICS

Table 20. Absolute Ratings

Parameter	Min.	Typ.	Max.	Note
RVDD1, RVDD2, RVDD2A, RVDD2B, RVDD3, RVDD3A, DAC_DVDDA, PLL_DVVDA, PLL_SVDDA, DAC_SVDDA, PLL_RVDDA, ADC_RVDDA, ADC_GVDDA, ADC_BVDDA, ADC_VDDA	-0.3		3.6 volts	
SRVDD1, SRVDD2, CVDD2, DVDD, SVDD, SYN_VDD, ADC_VDD1, ADC_VDD2	-0.25		2.75 volts	
Vin	Vss - 0.5volt		Vcc + 0.5V	
Operating temperature	0 degreeC		70 degreeC	
Maximum power consumption at XGA 75Hz output resolution			1.28 watts	(4)
Maximum power consumption at XGA 85Hz output resolution			1.35 watts	(4)

Table 21. DC Electrical Characteristic

Parameter	Min.	Typ.	Max.	Note
RVDD1, RVDD2, RVDD2A, RVDD2B, RVDD3, RVDD3A, DAC_DVDDA, PLL_DVVDA, PLL_SVDDA, DAC_SVDDA, PLL_RVDDA, ADC_RVDDA, ADC_GVDDA, ADC_BVDDA, ADC_VDDA	3.0 volts	3.3 volts	3.6 volts	
SRVDD1, SRVDD2, CVDD2, DVDD, SVDD, SYN_VDD, ADC_VDD1, ADC_VDD2	2.25 volts	2.5 volts	2.75 volts	
Vil (TTL inputs)	GND		0.8 volts	
Vih (TTL inputs)	2.0 volts		2.5 volts	(1)
Voh	2.4 volts		2.5 volts	
Vol	GND		0.4 volts	
Input Current	-10 uA		10 uA	
3.3 volt operating supply current	0 mA		20 mA/pad @ 10pF	(2)
2.5 volt operating supply current	0 mA	400mA		(3)

NOTE 1: 5V-Tolerent TTL Input pads are as follows:

- **CRT Interface:** HSYNC (pin #150),VSYNC (#148)
- **Host Interface:** HFS (#98), HCLK (#103), HDATA (#99), RESETN (#100), MFB[11:0]: MFB11 (#123), MFB10 (#124), MFB9 (#102), MFB8 (#104), MFB7 (#105), MFB6 (#106), MFB5(#107),MFB4 (#109), MFB3 (#110), MFB2 (#111), MFB1 (#112), MFB0 (#113)
- **OSD Interface:** OSD_DATA3 (#121), OSD_DATA2 (#120), OSD_DATA1 (#119), OSD_DATA0 (#118), OSD_FSW (#122)
- **Non-5V-Tolerant TTL Input Pad is:** TCLK (#141)

NOTE 2: When the panel interface is disabled, the supply current is 0 mA. The drive current of each pad can be programmed in the range of 2 mA to 20 mA (@capacitive loading = 10 pF).

NOTE 3: When all circuits are powered down and TCLK is stopped, the CVDD supply current becomes 0mA.

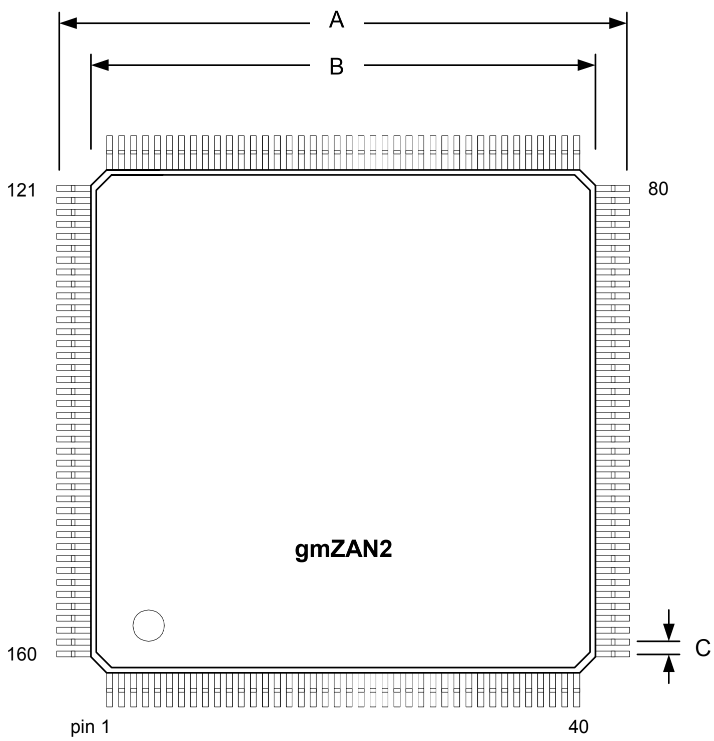
NOTE 4: This depends on the refresh rate supported by the LCD panel chosen.

4. ORDERING INFORMATION

Order Code	Package	Temperature Rating
gmZAN2	160-pin PQFP	Commercial 0°C to 70°C

5. MECHANICAL DIMENSIONS

Figure 19. 160 pin PQFP Package Dimensions



Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A	30.95	31.20	31.45	1.218	1.228	1.238
B	27.90	28.00	28.10	1.098	1.102	1.106
C		0.65			0.026	
D			4.25			0.167
E		1.60			0.063	
G	3.17	3.32	3.47	0.125	0.131	0.137
H	0.65	0.80	0.95	0.025	0.031	0.037
I	0.05	0.25	0.50	0.002	0.010	0.020
J	0		7	0		7
L	0.20	0.30	0.40	0.008	0.012	0.016
M	0.10	0.15	0.20	0.004	0.006	0.008

Depressed dot on package indicates pin 1 (lower left corner)