SONY

CXP874P60

CMOS 8-bit Single Chip Microcomputer

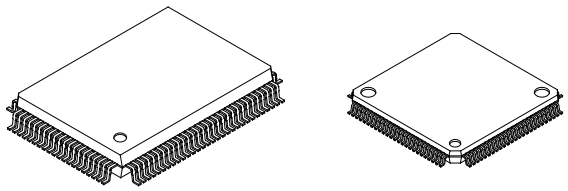
Description

The CXP874P60 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface (2ch independently), timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit (PPG 2ch independently, RTG 2ch independently), PWM generator, general purpose prescaler, PWM for tuner, VCR vertical sync separation circuit and the measuring circuit which measure signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, PROM, RAM and I/O port. They are integrated into a single chip.

Also CXP874P60 provides power on reset function, sleep/stop function which enables to lower power consumption .

CXP874P60 is the PROM-incorporated version of the CXP87452/87460 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

100 pin QFP (Plastic) 100 pin LQFP (Plastic)



Structure

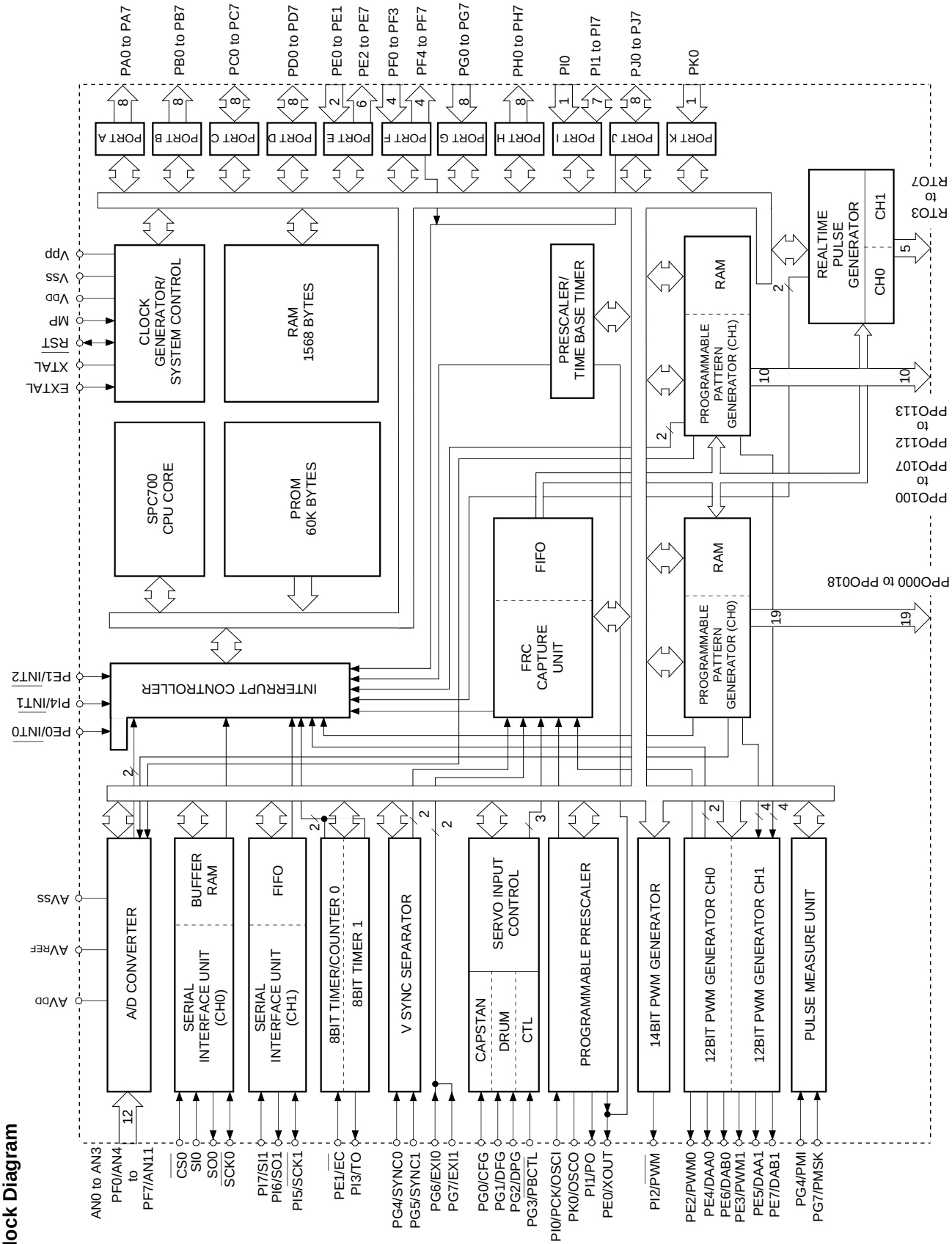
Silicon gate CMOS IC

Features

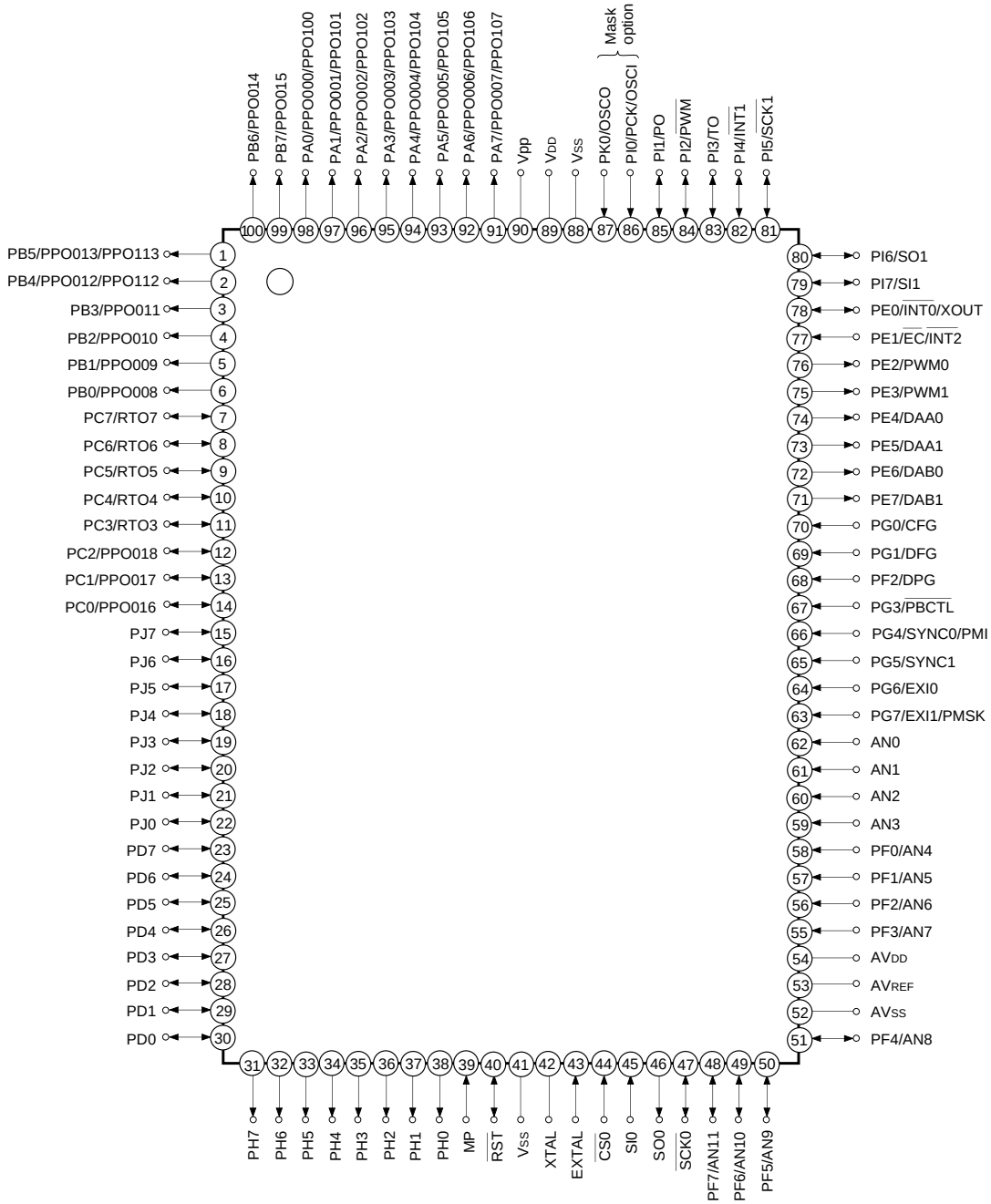
- A wide instruction set (213 instructions) which cover various types of data
  — 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle — During operation 333ns/12MHz (3.0 to 5.5V)
  During operation 250ns/16MHz (4.5 to 5.5V)
- Incorporated PROM capacity — 60K bytes
- Incorporated RAM capacity — 1568 bytes
- Peripheral functions
  - — A/D converter — 8-bit, 12-channel, successive approximation system (Conversion time: 20µs/16MHz)
  - — Serial interface — Incorporated buffer RAM (1 to 32 bytes auto transfer) 1-channel
    Incorporated 8-bit and 8-stage FIFO (1 to 8 bytes auto transfer) 1-channel
  - — Timer — 8-bit timer, 8-bit timer/counter, 19-bit time base timer
  - — High precision timing pattern generator — PPG 19 pins 32-stage programmable
    PPG 10 pins 21-stage programmable
    RTG 5 pins 2-channel
  - — PWM/DA gate output — PWM 12-bit, 2-channel (Repetitive frequency 62.5kHz/16MHz)
    DA gate pulse 12-bit, 4-channel
  - — Servo input control — Capstan FG, Drum FG/PG, CTL input
  - — VSYNC separator
  - — FRC capture unit — Incorporated 26-bit and 8-stage FIFO
  - — PWM output — 14-bit, 1-channel
  - — General purpose prescaler — 10-bit (System clock asynchronous)
  - — Pulse cycle measurement circuit
- Interruption — 18 factors, 14 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- Package — 100-pin plastic QFP/LQFP

E95112-ST

Block Diagram

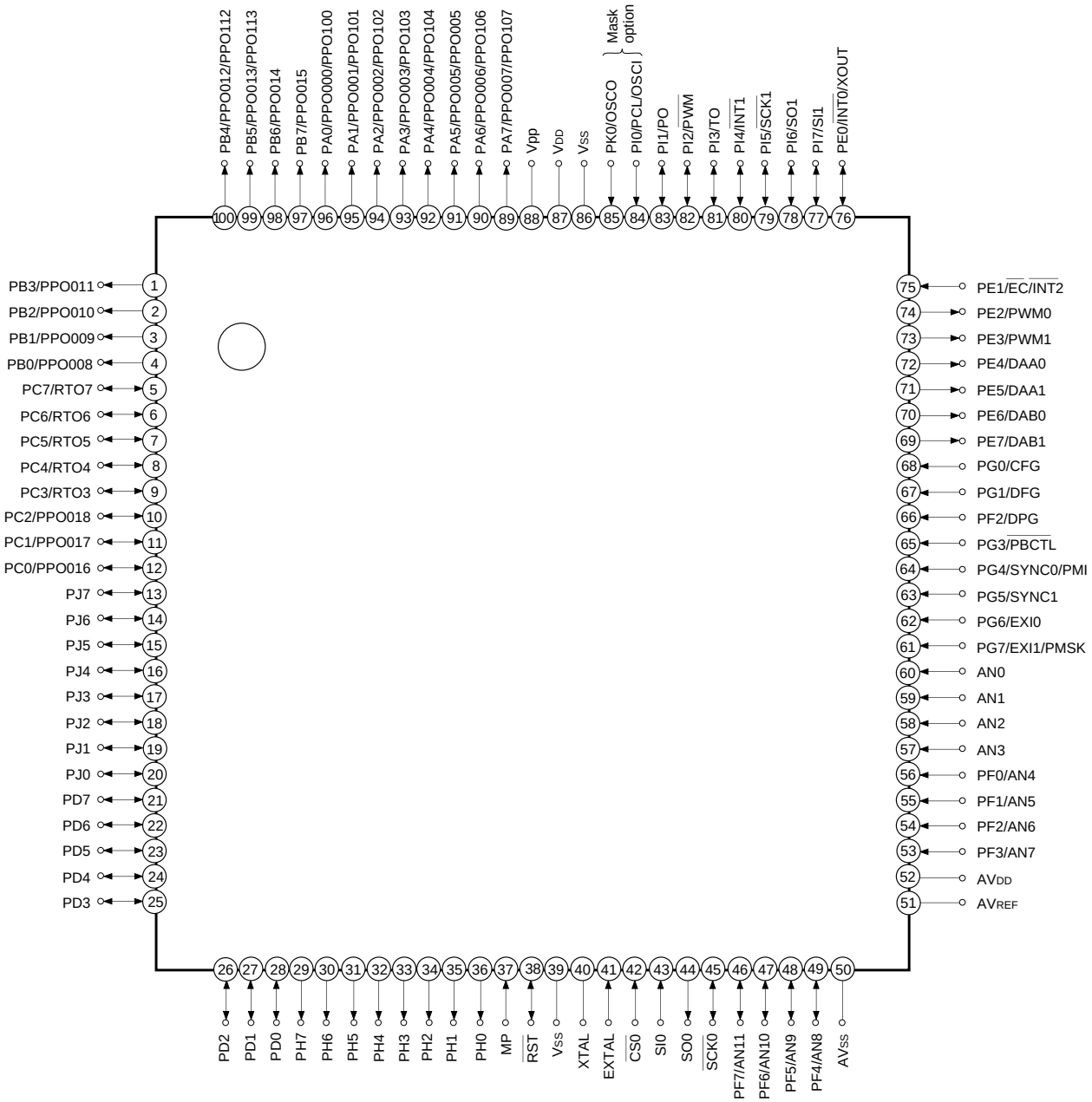


Pin Configuration 1 (Top View) 100-pin QFP Package



Note) 1. Vpp (Pin 90) is always connected to V_{DD}.
2. Vss (Pins 41 and 88) are both connected to GND.

Pin Configuration 2 (Top View) 100-pin LQFP Package



Note) 1. Vpp (Pin 88) is always connected to V_{DD}.
2. Vss (Pins 39 and 86) are both connected to GND.

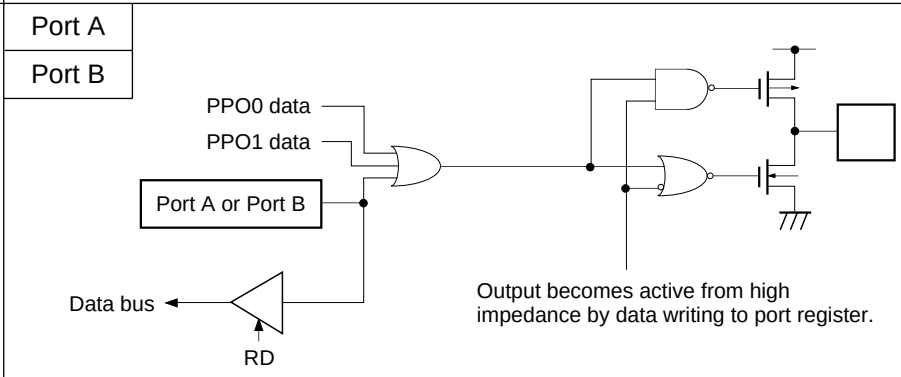
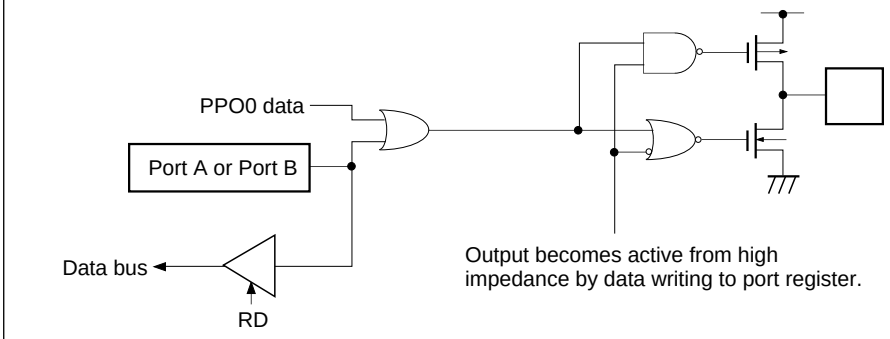
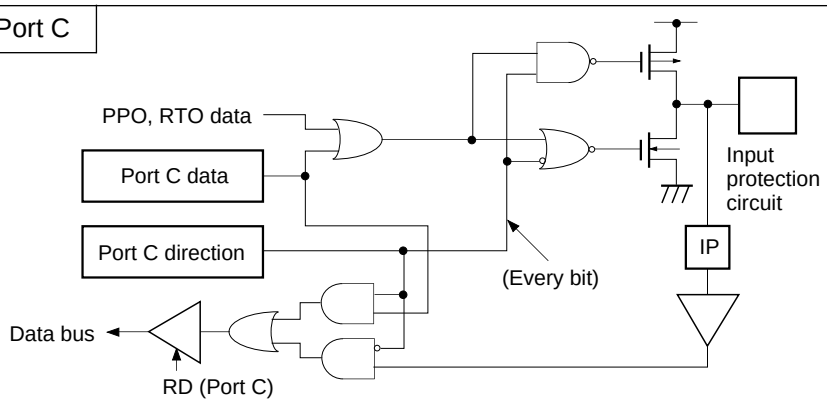
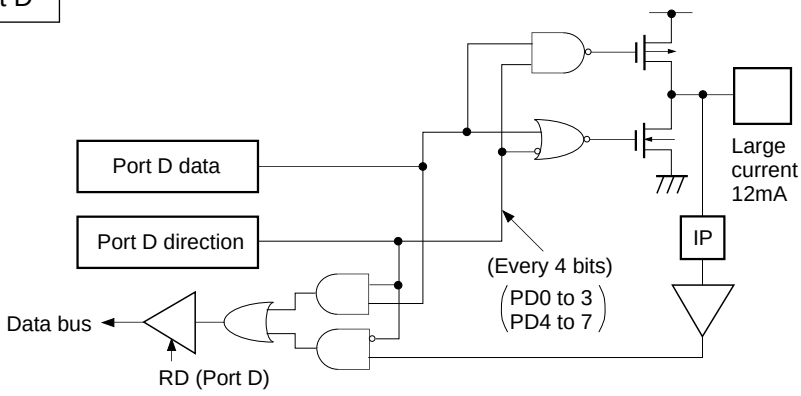
Pin Description

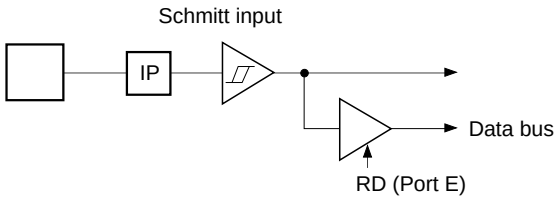
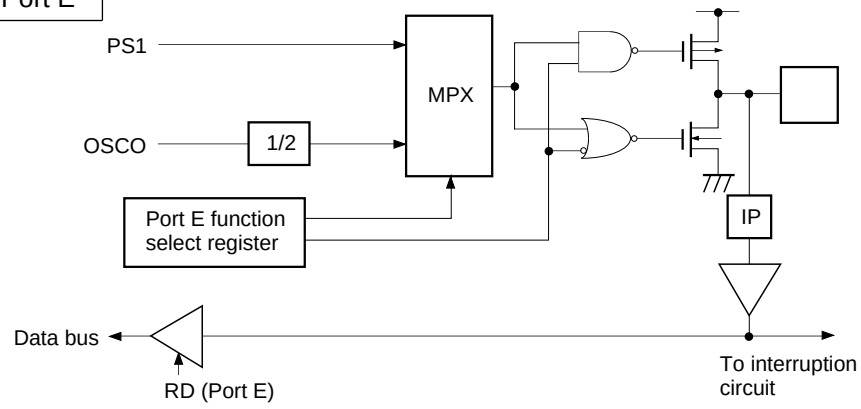
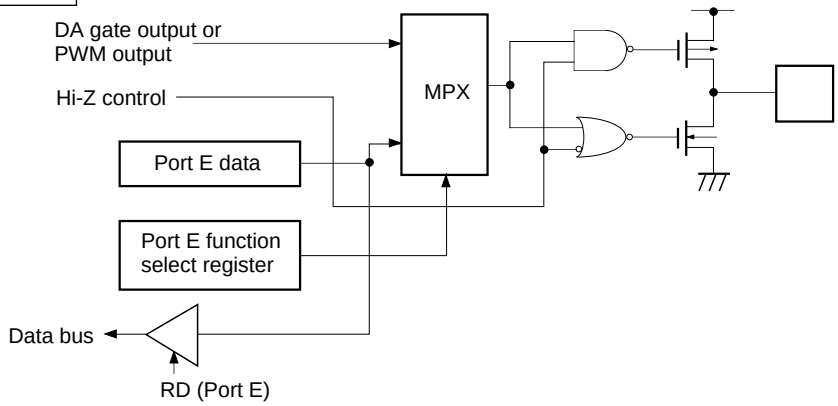
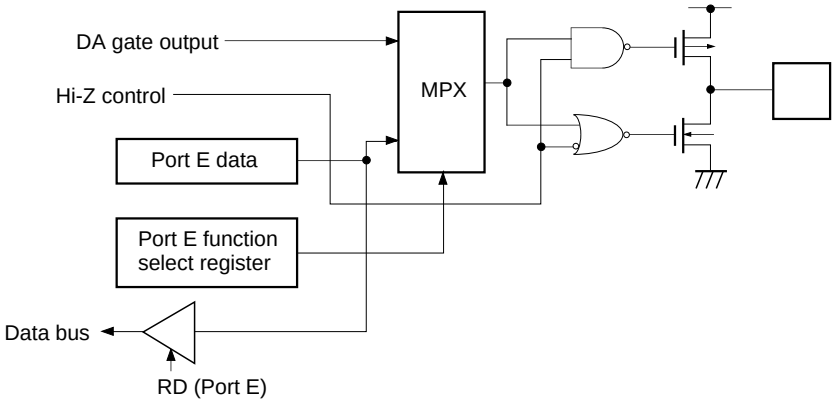
<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td>PA0/PPO000
/PPO100
to
PA7/PPO007
/PPO107</td><td>Output/
Real time
output</td><td>(Port A)
8-bit output port. Data is gated with PPO0 and PPO1 contents by OR-gate and they are output.
(8 pins)</td><td colspan="2" rowspan="2">Programmable pattern generator (PPG0, PPG1) output.
Functions as high precision real time pulse output port.
(PPG0 19 pins
PPG1 10 pins)</td></tr>
<tr><td>PB0/PPO008
to
PB7/PPO015</td><td>Output/
Real time
output</td><td>(Port B)
8-bit output port. Data is gated with PPO0 and PPO1 contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC0/PPO016
to
PC2/PPO018</td><td>I/O/
Real time
output</td><td rowspan="2">(Port C)
8-bit I/O port. Enables to specify I/O by bit unit.
Data is gated with PPO or RTO contents by OR-gate and they are output.
(8 pins)</td><td colspan="2" rowspan="2">Programmable pattern generator (PPG0, PPG1) output.
Functions as high precision real time pulse output port.
(PPG0 19 pins
PPG1 10 pins)</td></tr>
<tr><td>PC3/RTO3
to
PC7/RTO7</td><td>I/O/
Real time
output</td><td colspan="2">Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)</td></tr>
<tr><td>PD0 to PD7</td><td>I/O</td><td colspan="3">(Port D)
8-bit I/O port. Enable to specify I/O by 4-bit unit.
Enables to drive 12mA sink current. (During 5V±0.5V operation)
(8 pins)</td></tr>
<tr><td>PE0/$\overline{\text{INT0}}$
/XOUT</td><td>Input/Input/Output</td><td rowspan="8">(Port E)
8-bit port. Lower 2 bits are input port and upper 6 bits are output port.
(8 pins)</td><td>Input pin to request external interruption.
Active when falling edge.</td><td>1/2 dividing clock output of XTAL or OSCO.</td></tr>
<tr><td>PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$</td><td>Input/Input/Input</td><td>External event input pin for timer/counter.</td><td>Input pin to request external interruption.
Active when falling edge.</td></tr>
<tr><td>PE2/PWM0</td><td>Output/Output</td><td colspan="2" rowspan="2">PWM output pins.
(2 pins)</td></tr>
<tr><td>PE3/PWM1</td><td>Output/Output</td></tr>
<tr><td>PE4/DAA0</td><td>Output/Output</td><td colspan="2" rowspan="4">DA gate pulse output pins.
(4 pins)</td></tr>
<tr><td>PE5/DAA1</td><td>Output/Output</td></tr>
<tr><td>PE6/DAB0</td><td>Output/Output</td></tr>
<tr><td>PE7/DAB1</td><td>Output/Output</td></tr>
<tr><td>AN0 to AN3</td><td>Input</td><td colspan="3">Analog input pins to A/D converter. (12 pins)</td></tr>
<tr><td>PF0/AN4
to
PF3/AN7</td><td>Input/Input</td><td colspan="3" rowspan="2">(Port F)
Lower 4 bits are input port and upper 4 bits are output port.
Lower 4 bits also serve as standby release input pin.
(8 pins)</td></tr>
<tr><td>PF4/AN8
to
PF7/AN11</td><td>Output/Input</td></tr>
<tr><td>$\overline{\text{SCK0}}$</td><td>I/O</td><td colspan="3">Serial clock (CH0) I/O pin.</td></tr>
<tr><td>SO0</td><td>Ouput</td><td colspan="3">Serial data (CH0) output pin.</td></tr>
<tr><td>SI0</td><td>Input</td><td colspan="3">Serial data (CH0) input pin.</td></tr>
<tr><td>$\overline{\text{CS0}}$</td><td>Input</td><td colspan="3">Serial chip select (CH0) input pin.</td></tr>
</table>

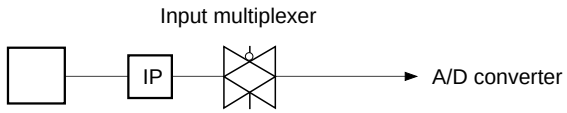
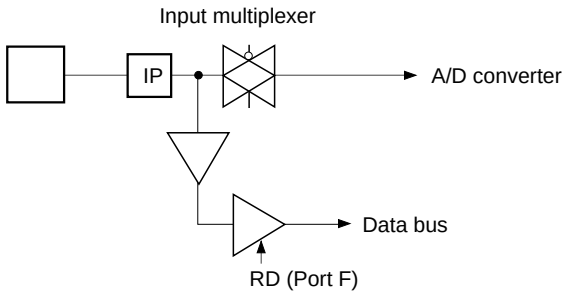
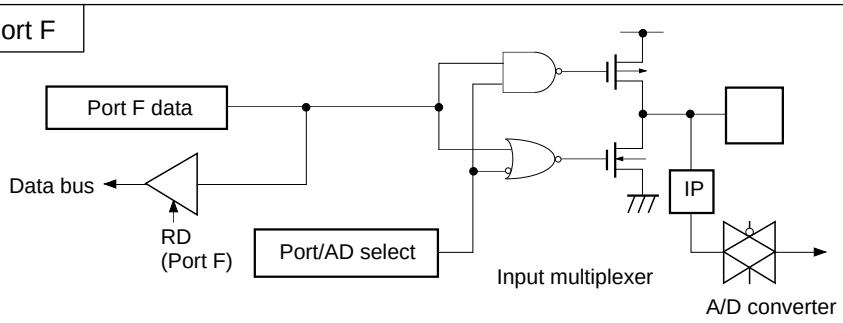
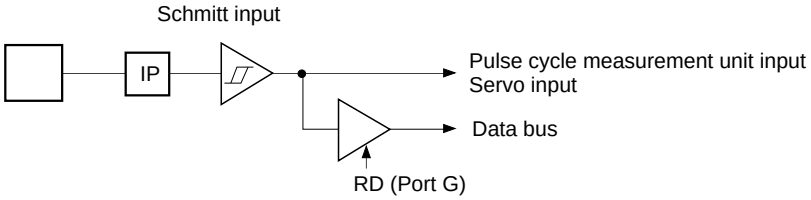
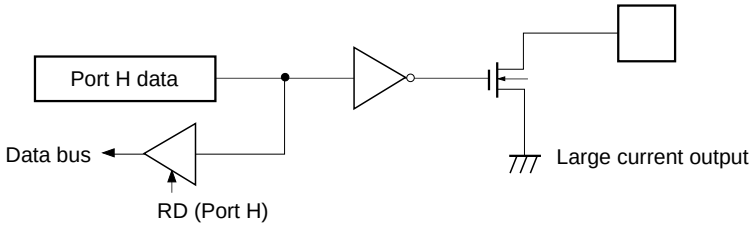
Symbol	I/O	Description		
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input pin.	
PG1/DFG	Input/Input		Drum FG input pin.	
PG2/DPG	Input/Input		Drum PG input pin.	
PG3/$\overline{\text{PBCTL}}$	Input/Input		Playback CTL pulse input pin.	
PG4/SYNC0 /PMI	Input/Input/Input		Composite sync signal input pin.	Measuring pulse signal input pin of pulse cycle measuring unit.
PG5/SYNC1	Input/Input			
PG6/EXI0	Input/Input		External input pin to FRC capture unit.	
PG7/EXI1/ PMSK	Input/Input/Input			Measuring enable signal input pin of pulse cycle measuring unit.
PH0 to PH7	Output	(Port H) 8-bit output port; large current, N-ch open drain output. (8 pins)		
PI0/PCK /OSCI	Input/Input/Input	(Port I) Lower 1 bit is input port (mask option) and upper 7 bits are I/O port. I/O port can be specified by bit unit. (8 pins)	External clock input pin of general purpose prescaler.	Connecting pin of crystal oscillation circuit for general purpose prescaler. (Mask option)
PI1/PO	I/O/Output		General purpose prescaler output pin.	
PI2/$\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.	
PI3/TO	I/O/Output		Timer/counter, output pin. (duty=50%)	
PI4/$\overline{\text{INT1}}$	I/O/Input		Input pin to request external interruption. Active when falling edge.	
PI5/$\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O pin.	
PI6/SO1	I/O/Output		Serial data (CH1) output pin.	
PI7/SI1	I/O/Input		Serial data (CH1) input pin.	
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. Function as standby release input can be specified by bit unit. I/O can be specified by bit unit.		

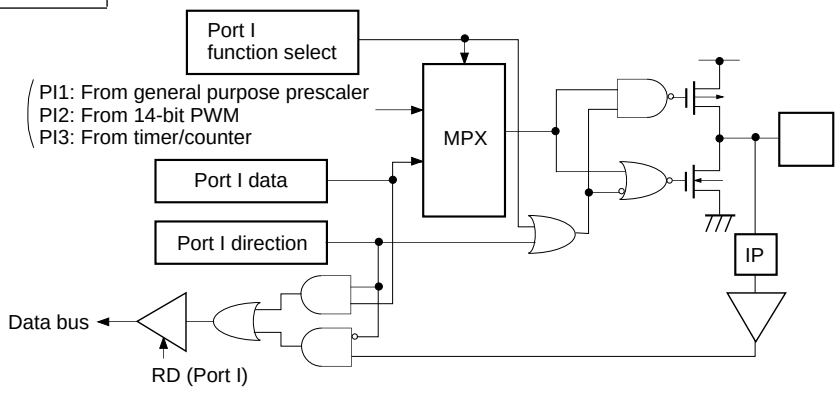
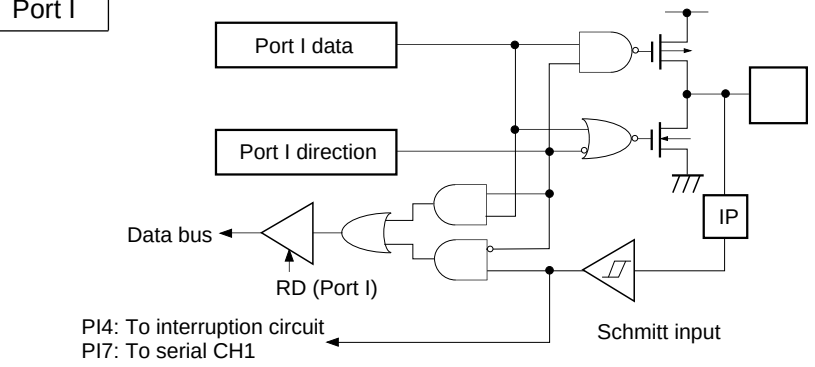
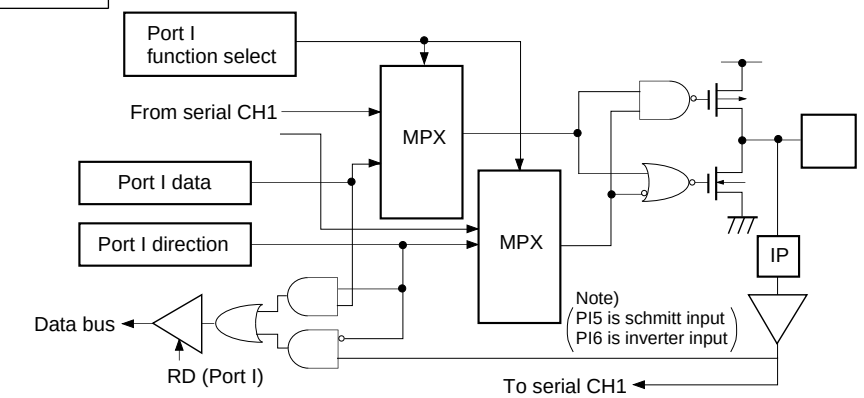
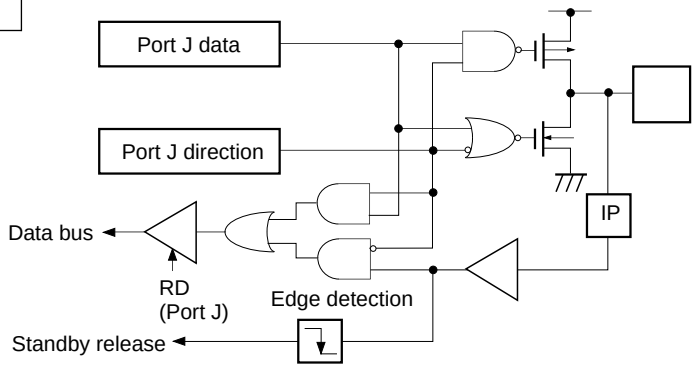
Symbol	I/O	Description	
PK0/OSCO	Input/Output	Input port. (Mask option)	Connecting pin of crystal oscillation circuit for general purpose prescaler. (Mask opiton)
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and input opposite phase clock to XTAL pin.	
XTAL	Output		
$\overline{RST}$	I/O	System reset pin of active "L" level. $\overline{RST}$ pin is I/O pin, which output "L" level by incorporated power on reset function when power on. (Mask option)	
MP	Input	Microprocessor mode input pin. Always connect to GND.	
AV_{DD}		Positive power supply pin of A/D converter.	
AV_{REF}	Input	Reference voltage input pin of A/D converter.	
AV_{SS}		GND pin of A/D converter.	
V_{DD}		Positive power supply pin.	
Vpp		Positive power supply pin for built-in PROM writing. Connect to V_{DD} for normal operation.	
V_{SS}		GND pin. Connect two Vss pins to GND.	

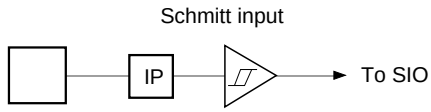
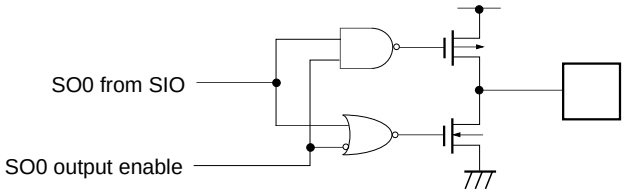
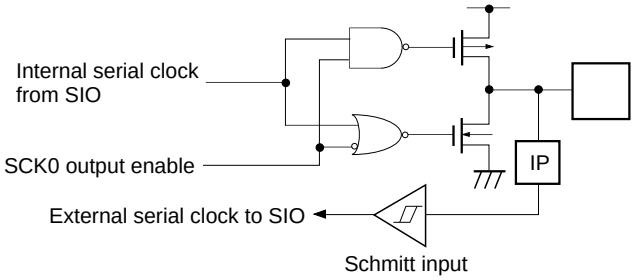
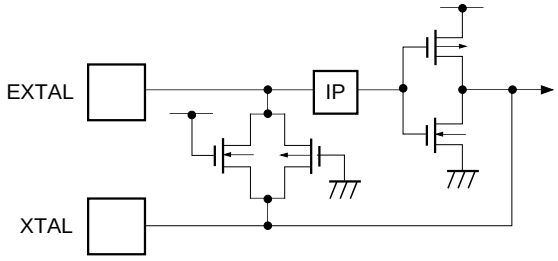
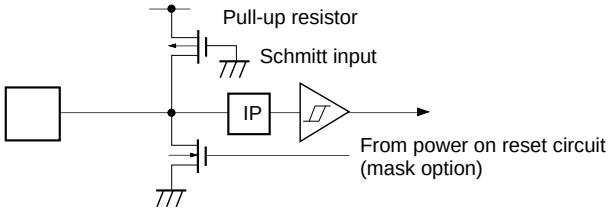
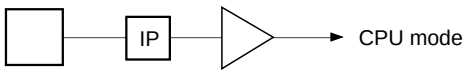
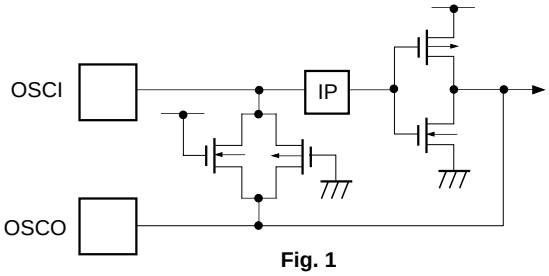
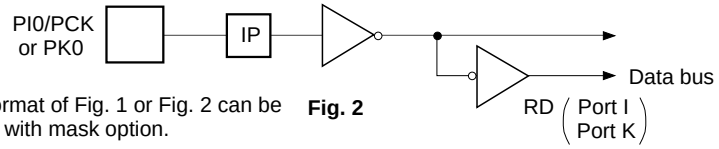
Input/Output Circuit Format for Pins

Pin	Circuit format	When reset
PA0/PPO000 /PPO100 to PA7/PPO007 /PPO107 PB4/PPO012 /PPO112 to PB5/PPO013 /PPO113 10 pins	Port A Port B 	Hi-Z
PB0/PPO008 to PB3/PPO011 PB6/PPO014 to PB7/PPO015 6 pins	Port B 	Hi-Z
PC0/PPO016 to PC2/PPO018 PC3/RTO3 to PC7/RTO7 8 pins	Port C 	Hi-Z
PD0 to PD7 8 pins	Port D 	Hi-Z

Pin	Circuit format	When reset
PE1/$\overline{EC}$/$\overline{INT2}$ 1 pin	Port E 	Hi-Z
PE0/$\overline{INT0}$ /XOUT 1 pin	Port E 	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E 	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E 	H level

Pin	Circuit format	When reset
AN0 to AN3 4 pins		Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z
PF4/AN8 to PF7/AN11 4 pins	Port F 	Hi-Z
PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0/PMI PG5/SYNC1 PG6/EXI0 PG7/EXI1/PMSK 8 pins	Port G  Note) For PG4 and PG5 input format, there are CMOS schmitt input and TTL schmitt input with product.	Hi-Z
PH0 to PH7 8 pins	Port H 	Hi-Z

Pin	Circuit format	When reset
PI1/PO PI2/$\overline{\text{PWM}}$ PI3/TO 3 pins	Port I 	Hi-Z
PI4/$\overline{\text{INT1}}$ PI7/SI1 2 pins	Port I 	Hi-Z
PI5/$\overline{\text{SCK1}}$ PI6/SO1 2 pins	Port I 	Hi-Z
PJ0 to PJ7 8 pins	Port J 	Hi-Z

Pin	Circuit format	When reset
$\overline{CS0}$ SI0 2 pins		Hi-Z
SO0 1 pin		Hi-Z
$\overline{SCK0}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins		Oscillation
$\overline{RST}$ 1 pin		L level
MP 1 pin		Hi-Z
PI0/PCK/OSCI PK0/OSCO 2 pins	Port I Port K  **Fig. 1**  **Fig. 2** Note) Circuit format of Fig. 1 or Fig. 2 can be selected with mask option.	Oscillation Hi-Z

Absolute Maximum Ratings (Vss=0V)

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13.0	V	Incorporated PROM
	AV_{DD}	AVss to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than large current output pins: per pin
	I_{OLC}	20	mA	Large current output pin*3: per pin
Low level total output current	$\sum I_{OL}$	130	mA	Total of output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP
		380		LQFP

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V. ($\overline{CS0}$, $\overline{SI0}$, PG and PH excluded.)

*3 The large current operation transistors are the N-CH transistors of the PD and PH ports.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V_{DD}	3.0	5.5	V	Guaranteed range during high speed mode (1/2 dividing clock) operation
		2.7	5.5	V	Guaranteed range during low speed mode (1/16 dividing clock) operation
		2.5	5.5	V	Guaranteed data hold operation range during STOP
	Vpp	Vpp = V_{DD}		V	*9
Analog power supply	AV_{DD}	3.0	5.5	V	*1
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS schmitt input*3 and PE0/$\overline{INT0}$ pins
			5.5	V	CMOS schmitt input*4
	V_{IHTS}	2.2	5.5	V	TTL schmitt input*5, *8
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*6, *8
		V_{DD} – 0.2	V_{DD} + 0.2	V	EXTAL pin*6, *7
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*2, *8
			0.2V_{DD}	V	*2, *7
	V_{ILS}	0	0.2V_{DD}	V	CMOS schmitt input*3, *4 and PE0/$\overline{INT0}$ pins
	V_{ILTS}	0	0.8	V	TTL schmitt input*5, *8
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*6, *8
		–0.3	0.2	V	EXTAL pin*6, *7
Operating temperature	Topr	–10	+75	°C	

*1 AV_{DD} and V_{DD} should be set to a same voltage.

*2 Normal input port (each pin of PC, PD, PF0 to PF3, PI PJ, and PK), MP pin.

*3 Each pin of $\overline{SCK0}$, $\overline{RST}$, PE1/$\overline{EC}$/$\overline{INT2}$, PI1/PO, PI4/$\overline{INT1}$, PI5/$\overline{SCK1}$ and PI7/SI1.

*4 Each pin of $\overline{CS0}$, SI0, and PG (for PG4 and PG5, when CMOS schmitt input is selected for the product.)

*5 Each pin of PG4 and PG5 (When TTL schmitt input is selected for the product)

*6 It specifies only when the external clock is input.

*7 In case of 3.0 to 3.6V supply voltage (V_{DD}).

*8 In case of 4.5 to 5.5V supply voltage (V_{DD}).

*9 Vpp and V_{DD} should be set to a same voltage.

Electrical Characteristics

DC Characteristics

Supply voltage (V_{DD}) 4.5 to 5.5V (Ta = –10 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PE, PF4 to PF7, PH (V_{OL} only) PI1 to PI7, PJ, SO, $\overline{SCK}$, $\overline{RST}$ (V_{OL} only)	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{ILR}	$\overline{RST}$	V_{DD} =5.5V, V_{IL} = 0.4V	–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PK, MP, AN0 to AN3, $\overline{CS}$, SI, SO, $\overline{SCK}$	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Supply current*1	I_{DD1}	V_{DD}	Crystal oscillation (C_1 = C_2 = 15pF) of 16MHz, V_{DD} = 5V ± 0.5V*2		28	50	mA
	I_{DDS1}		SLEEP mode, V_{DD} = 5V ± 0.5V		1.7	8.0	mA
	I_{DDS3}		STOP mode, V_{DD} = 5.5V			30	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, and AVss pins	Clock 1MHz, 0V other than the measured pins		10	20	pF

*1 When entire output pins are open.

*2 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE$_H$) to "00" and operating in high speed mode (1/2 dividing clock).

Supply voltage (V_{DD}) 3.0 to 3.6V (Ta = –10 to +75°C, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PE, PF4 to PF7, PH (V_{OL} only) PI1 to PI7, PJ, SO, $\overline{SCK}$, $\overline{RST}$ (V_{OL} only)	V_{DD} = 3.0V, I_{OH} = –0.15mA	2.7			V
			V_{DD} = 3.0V, I_{OH} = –0.5mA	2.3			V
Low level output voltage	V_{OL}		V_{DD} = 3.0V, I_{OL} = 1.2mA			0.3	V
			V_{DD} = 3.0V, I_{OL} = 1.6mA			0.5	V
		PD, PH	V_{DD} = 3.0V, I_{OL} = 5.0mA			1.0	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.6V, V_{IH} = 3.6V	0.3		20	µA
	I_{ILE}		V_{DD} = 3.6V, V_{IL} = 0.3V	–0.3		–20	µA
	I_{ILR}	$\overline{RST}$	V_{DD} = 3.6V, V_{IL} = 0.3V	–0.9		–200	µA
I/O leakage current	I_{IZ}	PA to PK, MP, AN0 to AN3, $\overline{CS}$, SI, SO, $\overline{SCK}$	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Supply current*1	I_{DD2}	V_{DD}	Crystal oscillation (C_1 = C_2 = 15pF) of 12MHz, V_{DD} = 3.3V ± 0.3V*2		12	30	mA
	I_{DDS2}		SLEEP mode, V_{DD} = 3.3V ± 0.3V		0.8	2.5	mA
	I_{DDS3}		STOP mode, V_{DD} = 5.5V			30	µA
Input capacity	C_{IN}	Other than V_{DD}, Vss, AV_{DD}, and AVss pins	Clock 1MHz, 0V other than the measured pins		10	20	pF

*1 When entire output pins are open.

*2 When setting upper 2 bits (CPU clock selection) of clock control register CLC (address: 00FE$_H$) to "00" and operating in high speed mode (1/2 dividing clock).

AC Characteristics

(1) Clock timing

(Ta = –10 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2 V_{DD} = 4.5 to 5.5V	1	16	MHz
			Fig. 1, Fig. 2	1	12	
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, V_{DD} = 4.5 to 5.5V	28		ns
			Fig. 2 (External clock drive)	37.5		
System clock input rising and falling times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)		200	ns
Event count clock input pulse width	t_{EL}, t_{EH}	PE1/$\overline{EC}$	Fig. 3	$t_{sys} \times 4$*		ns
Event count clock input rising and falling times	t_{ER}, t_{EF}	PE1/$\overline{EC}$	Fig. 3		20	ms

* tsys indicates three values according to the contents of the clock control register (address; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

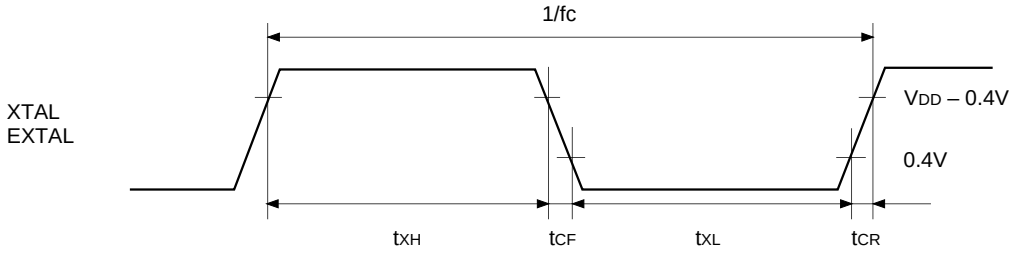


Fig. 2. Clock applied condition

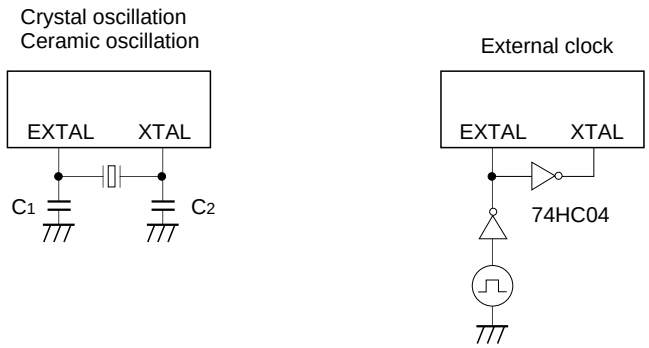
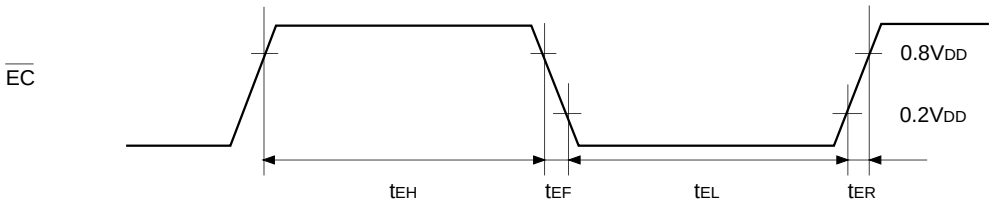


Fig. 3. Event count clock timing



(2) Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS}\downarrow\rightarrow\overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS}\uparrow\rightarrow\overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS}\downarrow\rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}\downarrow\rightarrow$ SO floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 100		ns
SI input setup time (against $\overline{SCK}\uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}\uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow\rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO means each pin of $\overline{CS}\rightarrow\overline{CS0}$, $\overline{SCK}\rightarrow$ SCK0, SI → SI0, and SO → SO0 respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V)

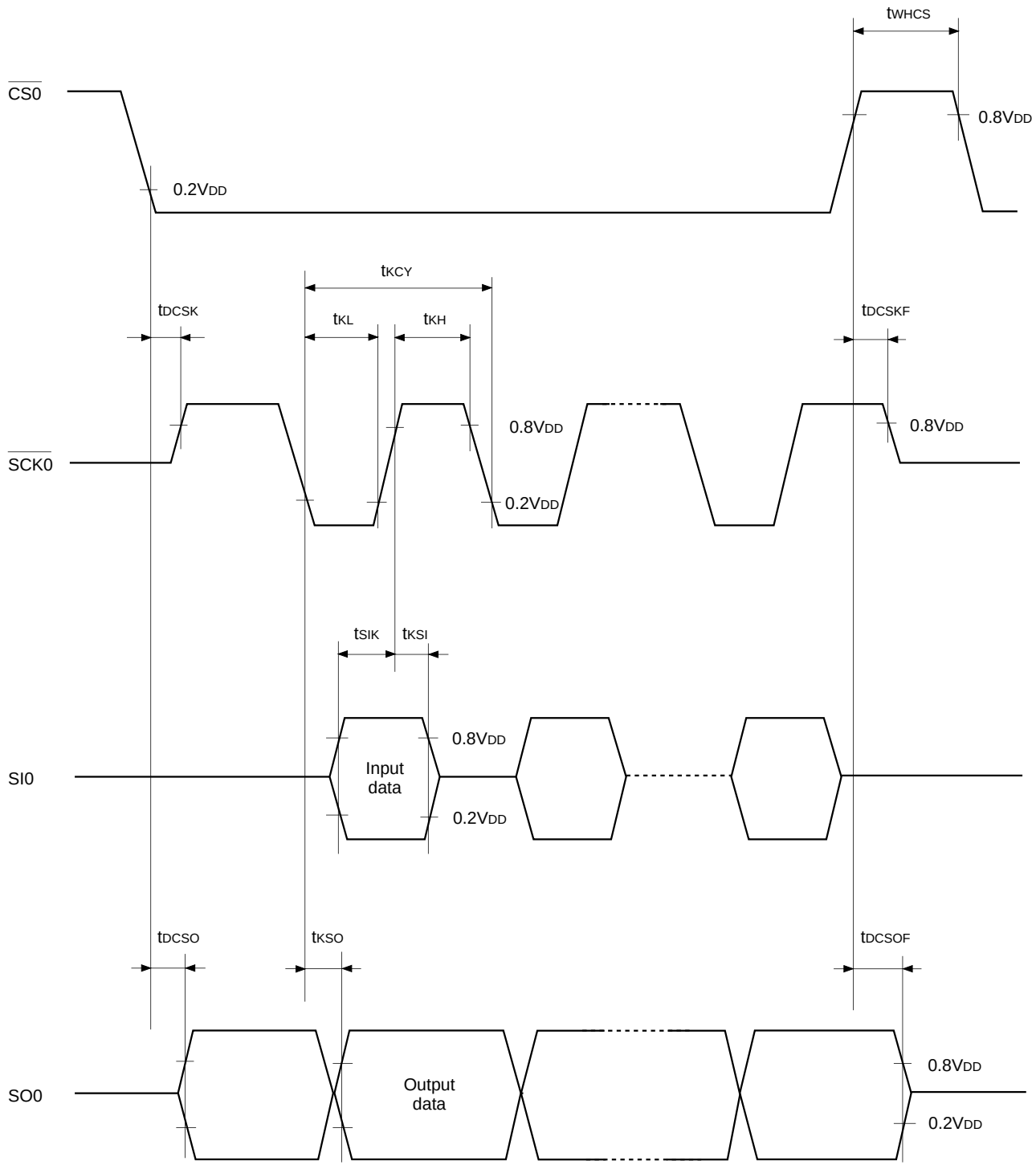
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS}\downarrow\rightarrow\overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 250	ns
$\overline{CS}\uparrow\rightarrow\overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS}\downarrow\rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 250	ns
$\overline{CS}\downarrow\rightarrow$ SO floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 150		ns
SI input setup time (against $\overline{SCK}\uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}\uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow\rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO means each pin of $\overline{CS}\rightarrow\overline{CS0}$, $\overline{SCK}\rightarrow$ SCK0, SI → SI0, and SO → SO0 respectively.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF.

Fig. 4. Serial transfer timing (CH0)



Serial transfer (CH1) (SIO mode) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	SCK1	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	SCK1	Input mode	tsys + 100		ns
			Output mode	8000/fc – 100		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	tsys + 200		ns
			$\overline{SCK1}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		tsys + 200	ns
			$\overline{SCK1}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.

Serial transfer (CH1) (SIO mode) (Ta = –10 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V)

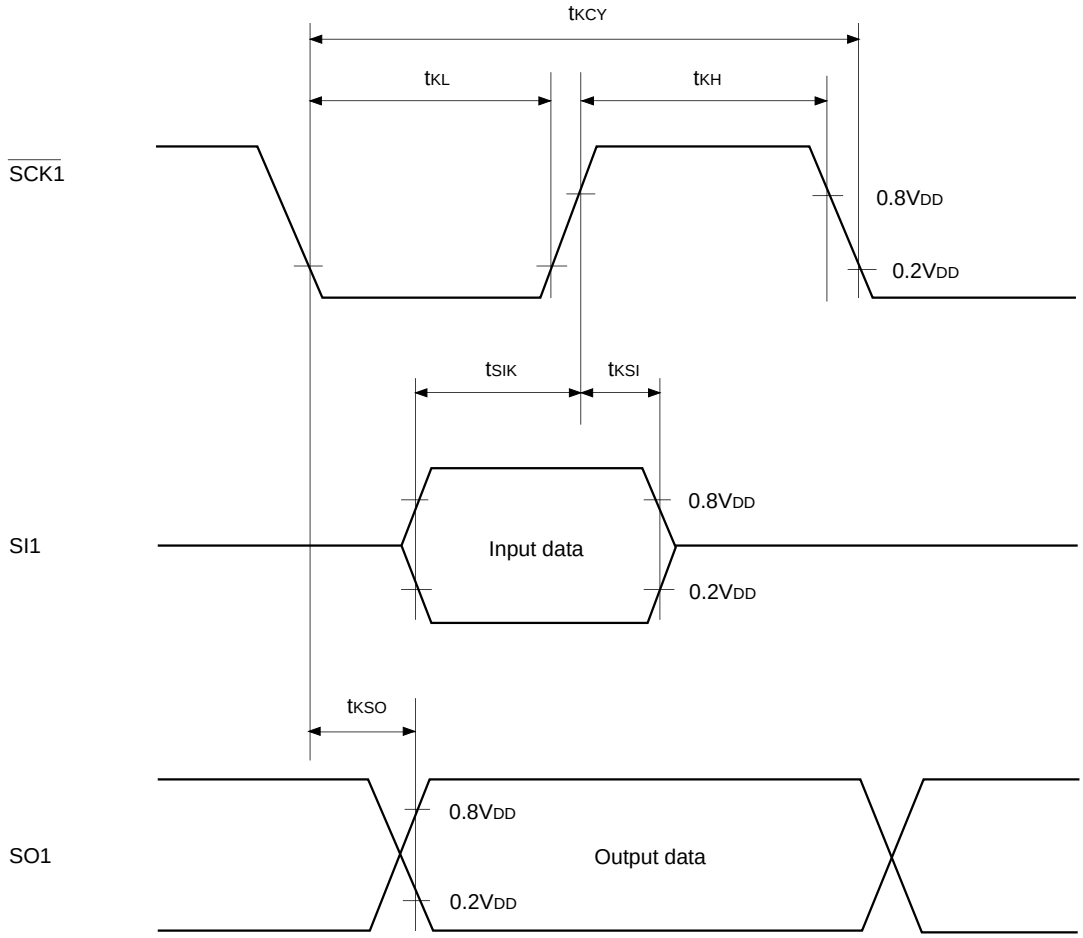
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	SCK1	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	SCK1	Input mode	tsys + 100		ns
			Output mode	8000/fc – 150		ns
SI1 input setup time (against $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (against $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	tsys + 200		ns
			$\overline{SCK1}$ output mode	100		ns
SCK1 ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		tsys + 250	ns
			$\overline{SCK1}$ output mode		125	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; 00FE$_H$) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF.

Fig. 5. Serial transfer CH1 timing (SIO mode)



Serial transfer (CH1) (Special mode) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	Note 1)		104		µs
SI1 data setup time	t_{LSU}	SI1		2			µs
SI1 data hold time	t_{LHD}	SI1		2			µs

Note 1) t_{LCY} specifies only serial mode register (CH1) (SIOM1: Address 01FA$_H$) lower 2 bits (SO1 clock selection) has been set at 104µs.

Note 2) The load of SO1 pin is 50pF + 1TTL.

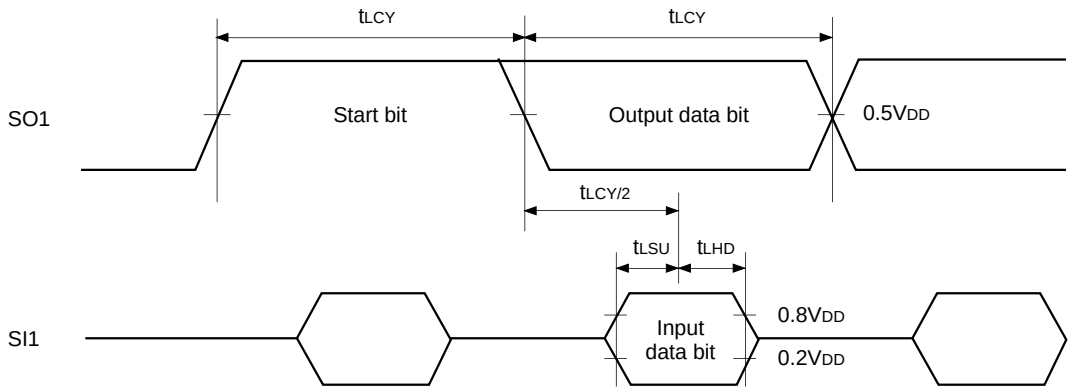
Serial transfer (CH1) (Special mode) (Ta = –10 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	Note 1)		104		µs
SI1 data setup time	t_{LSU}	SI1		2			µs
SI1 data hold time	t_{LHD}	SI1		2			µs

Note 1) t_{LCY} specifies only serial mode register (CH1) (SIOM1: Address 01FA$_H$) lower 2 bits (SO1 clock selection) has been set at 104µs.

Note 2) The load of SO1 pin is 50pF.

Fig. 6. Serial transfer CH1 timing (Special mode)



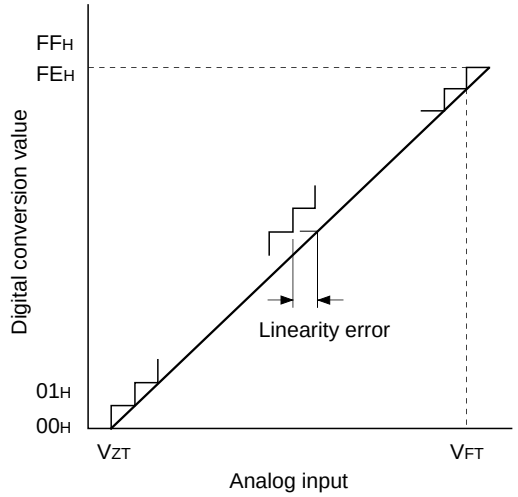
(3) A/D converter characteristics ($Ta = -10$ to $+75°C$, $V_{DD} = AV_{DD} = 4.5$ to $5.5V$, $AV_{REF} = 4.0$ to AV_{DD}, $V_{SS} = AV_{SS} = 0V$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation Ta = 25°C $V_{DD} = AV_{DD} = AV_{REF} = 5.0V$ $V_{SS} = AV_{SS} = 0V$			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}			µs
Sampling time	t_{SAMP}			12/f_{ADC}			µs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 4.5$ to $5.5V$	$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode $AV_{REF} = 4.0$ to $5.5V$		0.6	1.0	mA
			SLEEP mode STOP mode			10	µA

A/D converter characteristics ($Ta = -10$ to $+75°C$, $V_{DD} = AV_{DD} = 3.0$ to $3.6V$, $AV_{REF} = 2.7$ to AV_{DD}, $V_{SS} = AV_{SS} = 0V$)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Only for A/D converter operation Ta = 25°C $V_{DD} = AV_{DD} = AV_{REF} = 3.3V$ $V_{SS} = AV_{SS} = 0V$			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}			µs
Sampling time	t_{SAMP}			12/f_{ADC}			µs
Reference input voltage	V_{REF}	AV_{REF}	$V_{DD} = AV_{DD} = 3.0$ to $3.6V$	$AV_{DD}-0.3$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode $AV_{REF} = 2.7$ to $3.6V$		0.4	0.7	mA
			SLEEP mode STOP mode			10	µA

Fig. 7. Definitions of A/D converter terms



* The value of f_{ADC} is as follows by selecting ADC operation clock (MSC: Address 01FFH bit 0).
When PS2 is selected, $f_{ADC} = fc/2$
When PS1 is selected, $f_{ADC} = fc$

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ PJ0 to PJ7		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 8. Interruption input timing

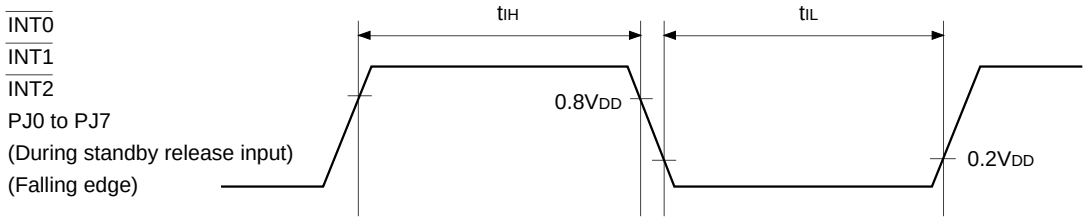
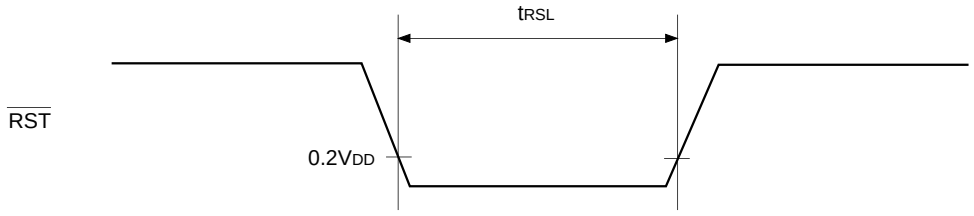


Fig. 9. Reset input timing



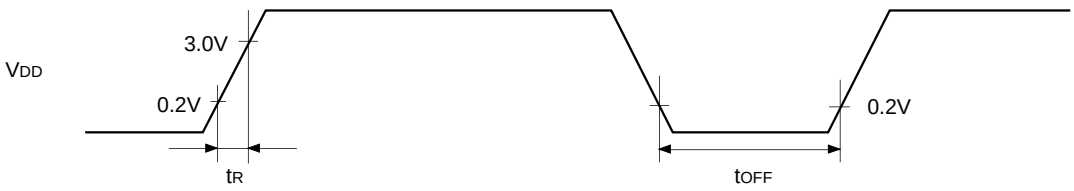
(5) Power on reset

Power on reset* (Ta = –10 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising edge	t_R	V_{DD}	Power on reset	0.05	30	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

* Specifies only when power on reset function is selected.

Fig. 10. Power on reset



The power supply should rise smoothly.

(6) General purpose prescaler (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	f_{PCK}	PCK				12	MHz
External clock input pulse width	t_{WH}, t_{WL}	PCK		33			ns
External clock input rising and falling times	t_R, t_F	PCK				200	ns
Prescaler output delay time (against PCK ↑)	t_{PLH}	PO	External clock input PCK $t_R = t_F$ = 6ns		80	130	ns
	t_{PHL}				60	100	ns
Prescaler output rising and falling times	t_{TLH}	PO	External clock input PCK $t_R = t_F$ = 6ns		50	100	ns
	t_{THL}				20	40	ns

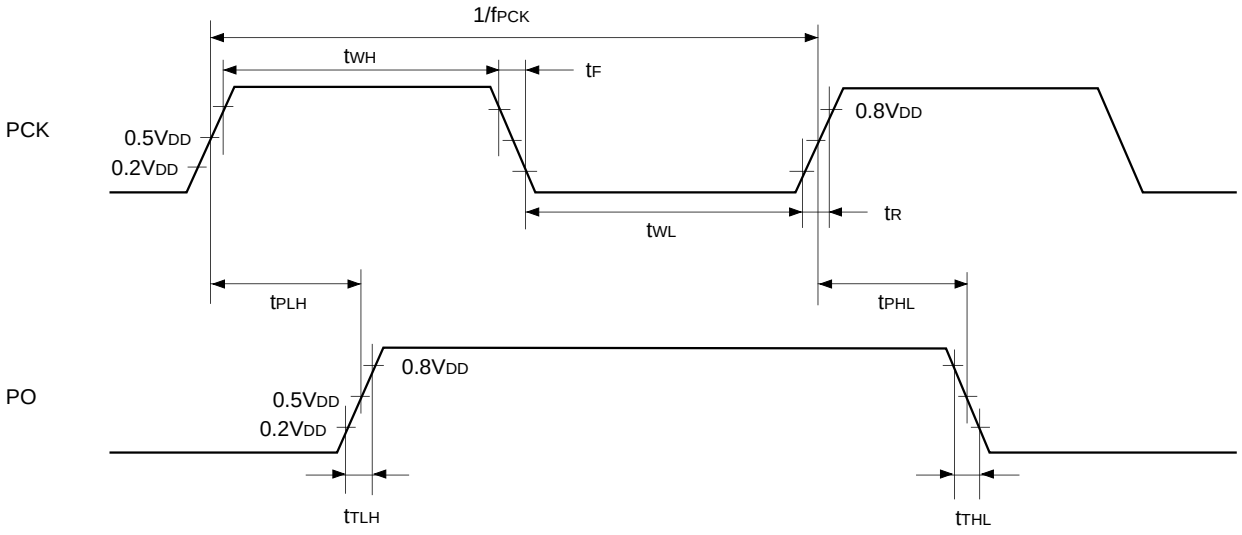
Note) The load of PO pin is 50pF.

General purpose prescaler (Ta = –10 to +75°C, V_{DD} = 3.0 to 3.6V, Vss = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	f_{PCK}	PCK				12	MHz
External clock input pulse width	t_{WH}, t_{WL}	PCK		33			ns
External clock input rising and falling times	t_R, t_F	PCK				200	ns
Prescaler output delay time (against PCK ↑)	t_{PLH}	PO	External clock input PCK $t_R = t_F$ = 6ns		130	220	ns
	t_{PHL}				90	150	ns
Prescaler output rising and falling times	t_{TLH}	PO	External clock input PCK $t_R = t_F$ = 6ns		100	280	ns
	t_{THL}				30	70	ns

Note) The load of PO pin is 50pF.

Fig. 11. General purpose prescaler timing



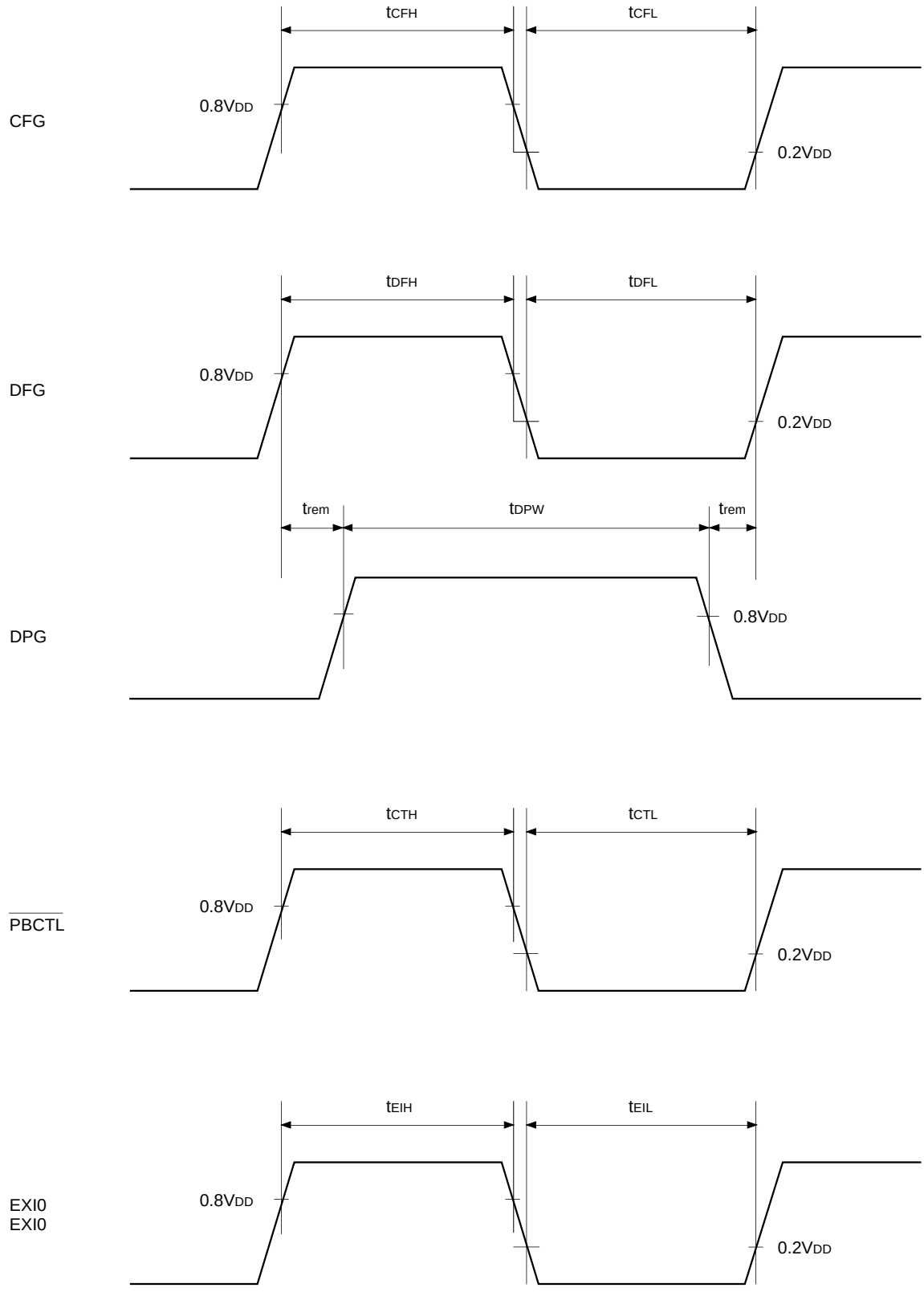
(7) Others (Ta = –10 to +75°C, V_{DD} = 3.0 to 5.5V, Vss = 0V)

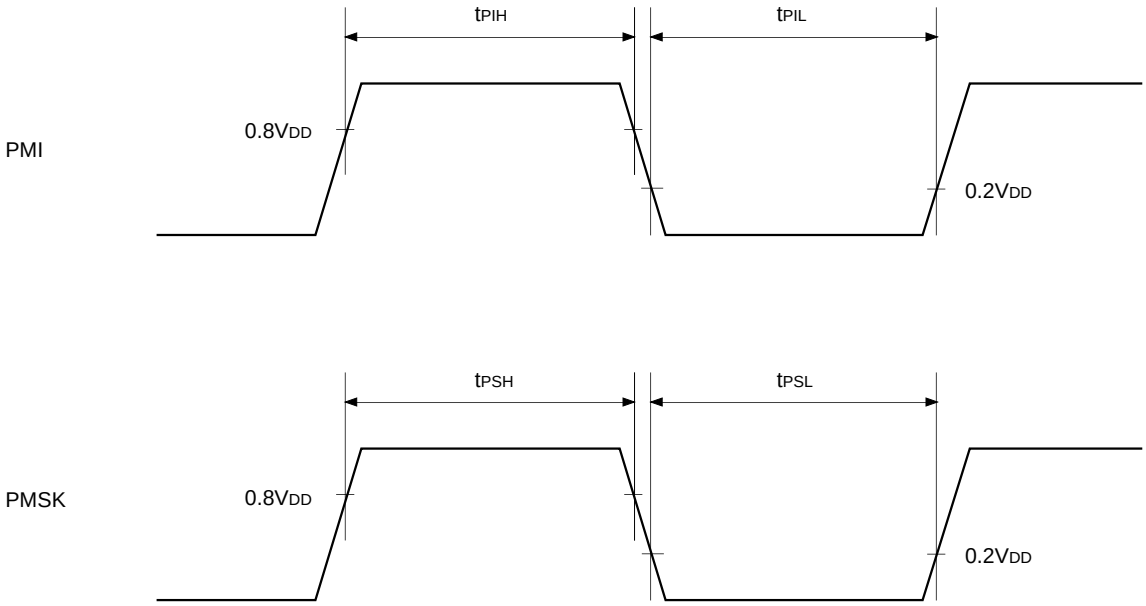
Item	Symbol	Pin	Condition	Min.	Max.	Unit
CFG input high and low level widths	t_{CFH} t_{CFL}	CFG		$t_{FRC} \times 24 + 200$		ns
DFG input high and low level widths	t_{DFH} t_{DFL}	DFG		$t_{FRC} \times 8 + 200$		ns
DPG minimum pulse width	t_{DPW}	DPG		50		ns
DPG minimum removal time	trem	DPG		50		ns
$\overline{\text{PBCTL}}$ input high and low level widths	t_{CTH} t_{CTL}	$\overline{\text{PBCTL}}$	tsys = 2000/fc	$t_{FRC} \times 8 + t$sys + 200		ns
EXI input high and low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	tsys = 2000/fc	$t_{FRC} \times 8 + t$sys + 200		ns
PMI input high and low level widths	t_{PIH} t_{PIL}	PMI		tsys + 200		ns
PMSK input high and low level widths	t_{PSH} t_{PSL}	PMSK		tsys + 200		ns

Note 1) tsys indicates three values according to the contents of the clock control register (address; $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The value of t_{FRC} is as follows by selecting FRC clock (FRCS: $01EE_H$ bit 7)
When PS0 is selected, t_{FRC} = 1000/fc [ns]
When PS1 is selected, t_{FRC} = 2000/fc [ns]

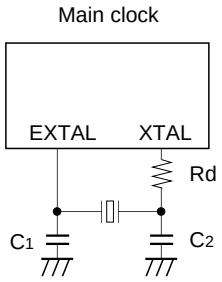
Fig. 12. Other timings




tPIH
tPIL
PMI
0.8VDD
0.2VDD
tPSH
tPSL
PMSK
0.8VDD
0.2VDD

Supplement

Fig. 13. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	22 (15)	22 (15)	0	(i)
		10.00				
		12.00	15	15		
		16.00	12	12		

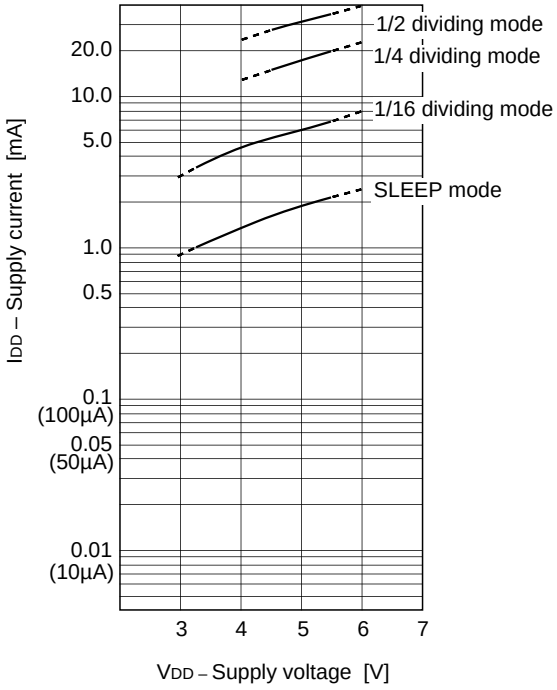
Mask Option Table

Item	Mask product	CXP874P60Q-1-□□□ CXP874P60R-1-	CXP874P60Q-2-□□□ CXP874P60R-2-
Reset pin pull-up resistor	Non-existent/existent	Existent	Existent
Power on reset circuit	Non-existent/existent	Existent	Existent
Genaral purpose prescaler oscillation circuit	Non-existent/existent	Non-existent	Existent
Input circuit format*	CMOS schmitt /TTL schmitt	CMOS schmitt	TTL schmitt

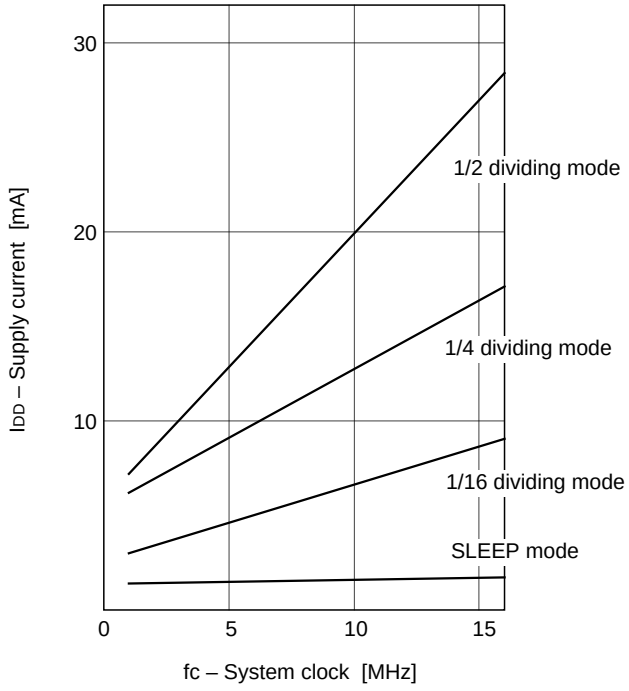
* In PG4/SYNC0/PMI pin and PG5/SYNC1 pin.

Characteristics Curve

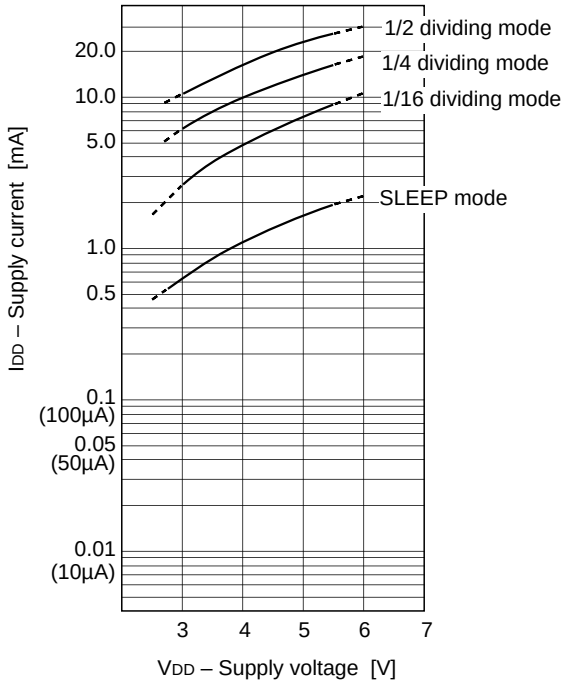
IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)



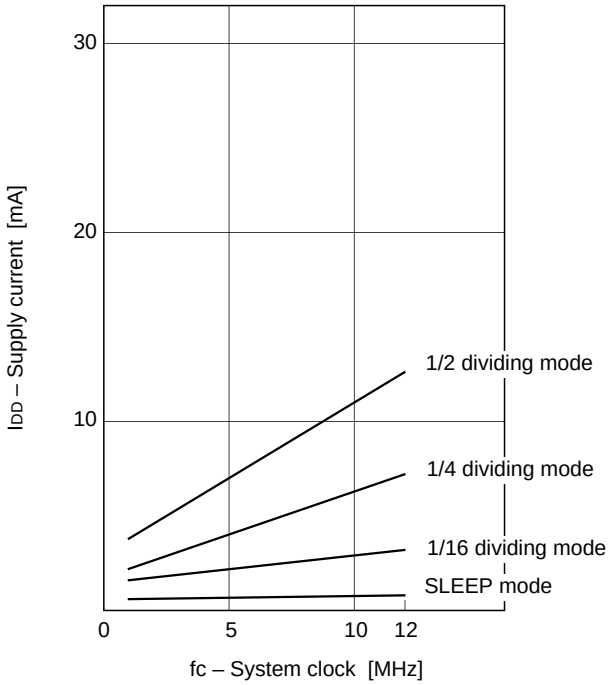
IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)



IDD vs. VDD
(fc = 12MHz, Ta = 25°C, Typical)

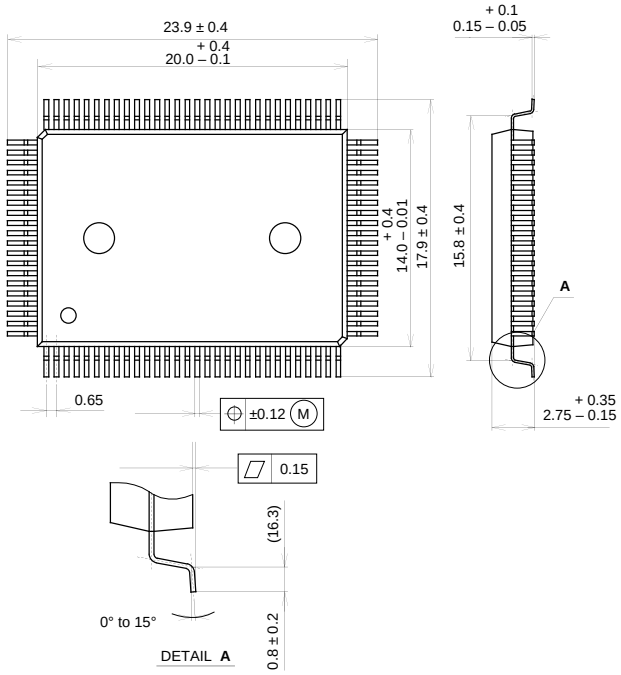


IDD vs. fc
(VDD = 3.3V, Ta = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)

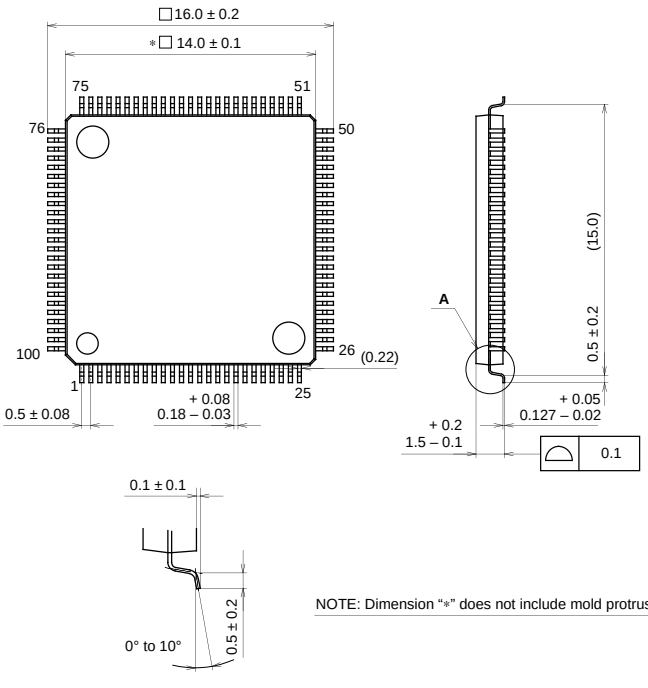


SONY CODE	QFP-100P-L01
EIAJ CODE	*QFP100-P-1420-A
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	*QFP100-P-1414-A
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	