OKI semiconductor

MSM5221

56-DOT STATIC LCD DRIVER

GENERAL DESCRIPTION

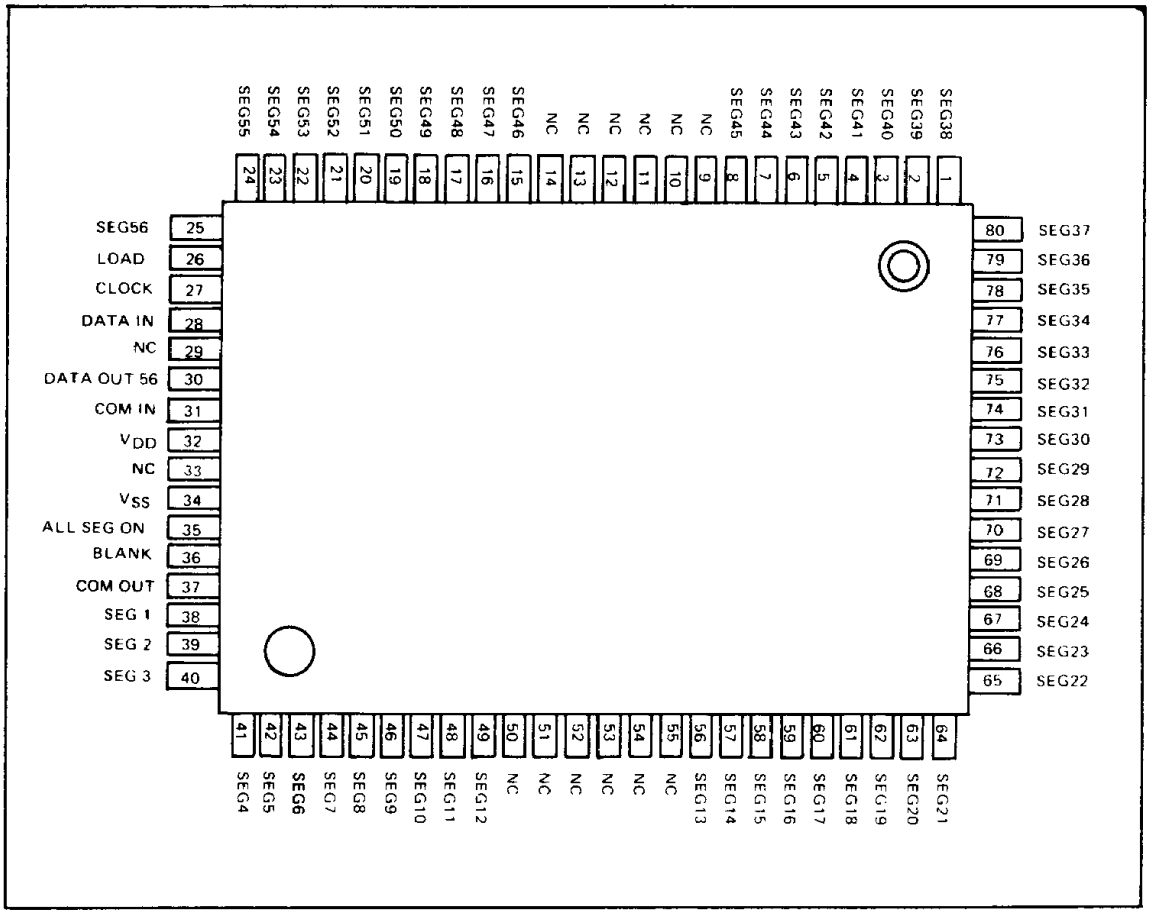
The OKI MSM5221GS is a 56 dot static LCD driver which is fabricated by low power CMOS metal gate technology. This LSI consists of 56-bit shift register, 56-bit latch and 56-bit LCD driver. The display data, which was input to the 56-bit shift register by the DATA IN signal and CLOCK signal, is transferred to the 56-bit latch by the LOAD signal and the data is output to the LCD through the 56-bit LCD driver.

FEATURES

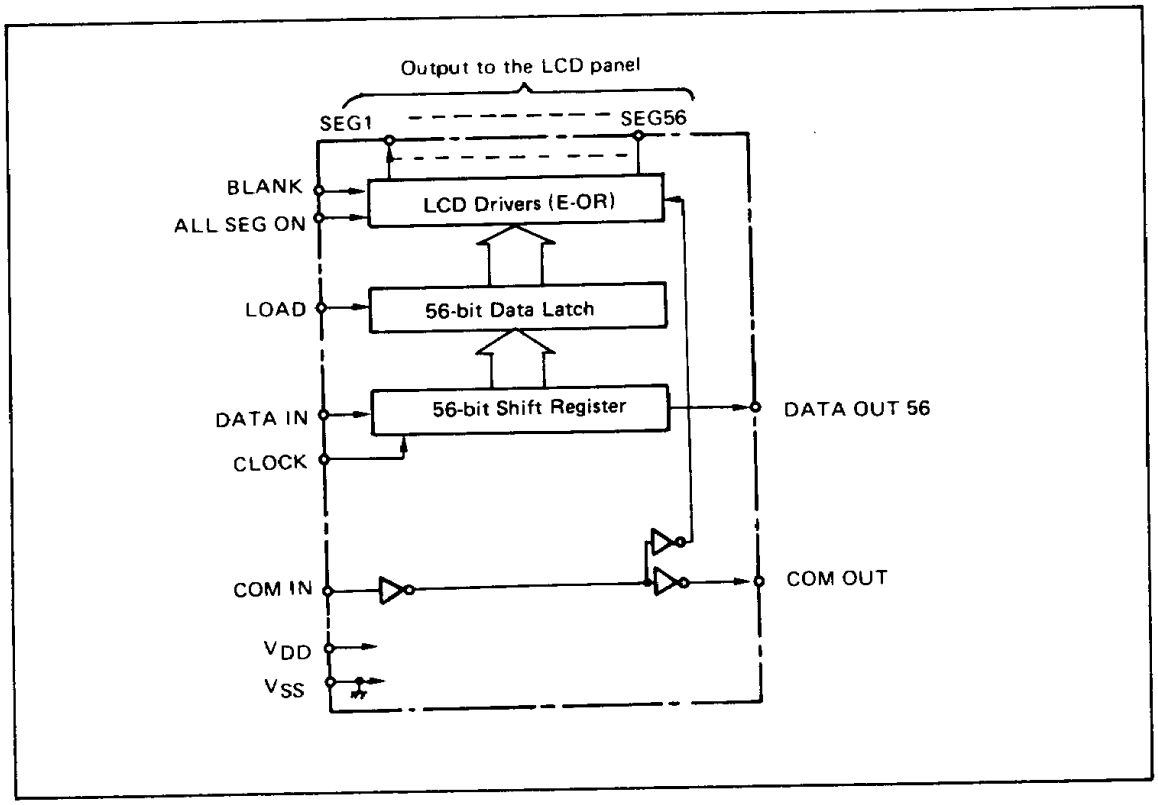
- 56 dots static LCD driving capability
- Simple interface with microcomputer chip (controlled by three input signals)
- Bit-to-bit correspondence between the input and output
- Cascade connection capability
- Fully controlled by the software
- LCD driving AC frequency is directly input externally
- Applicable as an output expander
- Supply voltage: 3 ~ 7V
- 80 pin plastic QFP (QFP80-P-1420-K)
- 80 pin -VI plastic QFP (QFP80-P-1420-VIK)

PIN CONFIGURATION

(Top view) 80 pin plastic QFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	$V_{DD} - V_{SS}$	T_a = 25°C	−0.3 ~ +7	V
Input voltage	V_I	T_a = 25°C	V_{SS} − 0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

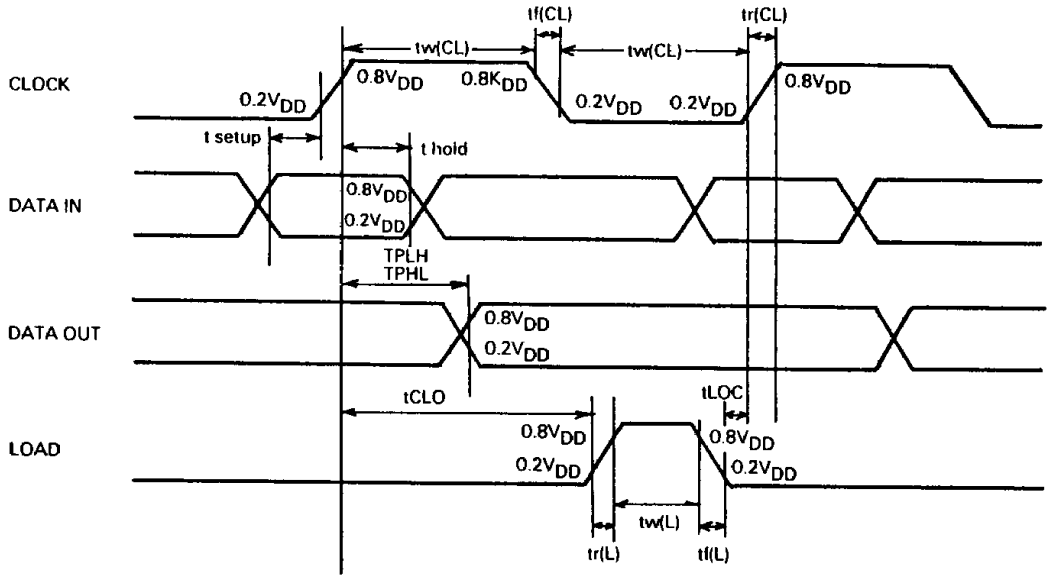
OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply voltage	$V_{DD} - V_{SS}$	—	3 ~ 7	V
Operating temperature	T_{OP}	—	−40 ~ +85	°C

Switching Characteristisc

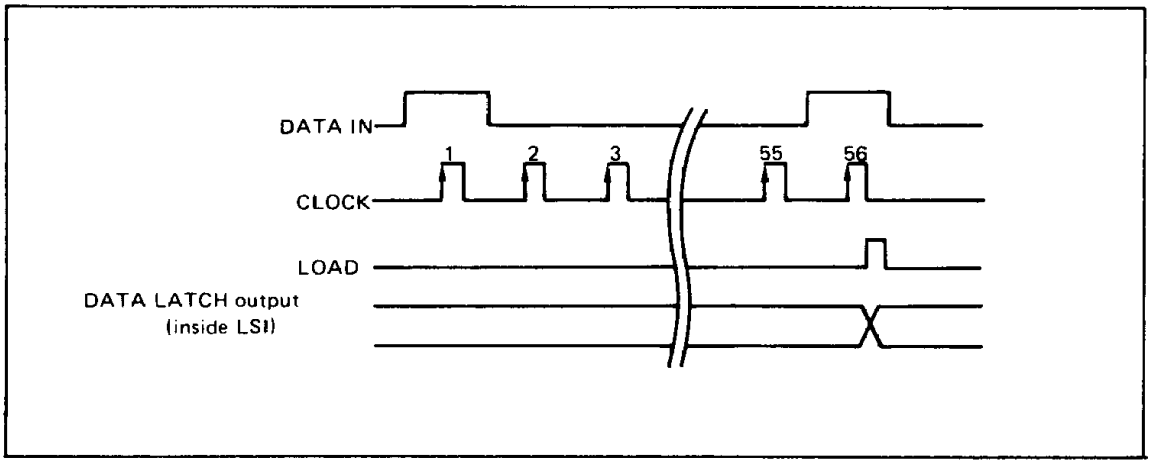
(V_{DD} = 5V ± 10% Ta = 25°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Propagation delay time	tP HL	—	—	—	600	ns
Data out delay time	tP LH	—	—	—	600	ns
Maximum clock frequency	fCL	DUTY = 50%	1	—	—	MHz
Clock width	tw (CL)	—	400	—	—	ns
Load width	tw (L)	—	400	—	—	ns
Data setup time	t setup	—	300	—	—	ns
Data hold time	t hold	—	300	—	—	ns
Clock-to-load time	t CLO	—	500	—	—	ns
Load-to-clock time	t LOC	—	0	—	—	ns
Clock rise/fall time	tr (CL), td (CL)	—	50	—	—	ns
Load rise/fall time	tr (L), tf (L)	—	1	—	—	ns



FUNCTIONAL DESCRIPTION

- **Operation Description**
  The display data is input to the shift register by the DATA IN signal and CLOCK signal. It is transferred to the 56-bit latch by the LOAD signal and it is output to the LCD panel through 56-bit LCD driver.



- **COM IN**
  Input pin to generate the COM OUT signal. The same phase signal as the COM IN pin is output from the COM OUT pin.

- **DATA IN, CLOCK**
  DATA IN is a data input in which enables the LCD to display when DATA IN signal is at high level. The 56-bit shift register is shifted at the rising edge of the CLOCK signal. Initially, the first bit of the shift register contains the current logic level of the DATA IN pin, and the bit N (N = 2 ~ 56) contains the data which was in bit N − 1 (N = 2 ~ 56) before the start of the operation. The data which was in bit 56 before the operation start is considered invalid.

- **LOAD**
  The data in the 56-bit shift register is shifted to the 56-bit latch when the LOAD pin is set at the high level, while the last data which was transferred to the latch when the LOAD pin was set at high level is constantly output when the LOAD is set at low level.

- **ALL SEG ON**
  When this pin is set at high level, all segments display turn on. This pin has the priority to the BLANK pin described as below.

- **BLANK**
  When this pin is set at high level, all segments display turn off. The ALL SEG ON pin has the priority over this pin.

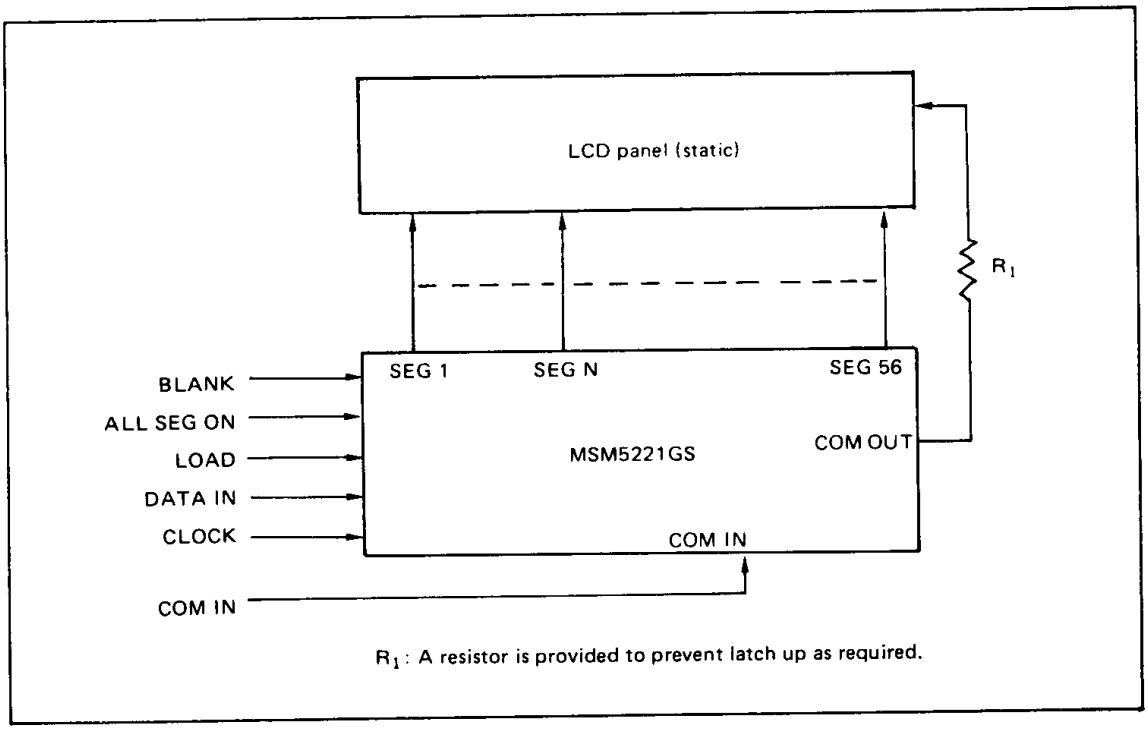
- **SEG1 ~ SEG56**
  LCD driving output pins. The reversed phase of the COM signal, which is used to display the data, is output from these pins when SEG1 ~ SEG56 are set at high level, while there is no display on the LCD when these pins are set at low level.
  The display data which was input from the DATA IN pin is output from these pins to the LCD panel. The SEG N pin corresponds to the bit N of the shift register.

- **COM OUT**
  Output terminal for the LCD. It is connected to the common side of the LCD panel.

- **DATA OUT 56**
  Output pin of the shift register. It is used when the MSM5221GS is connected in a series (cascade connection). MSM5221GS's DATA OUT 56 is connected to the next MSM5221GS's DATA IN terminal.

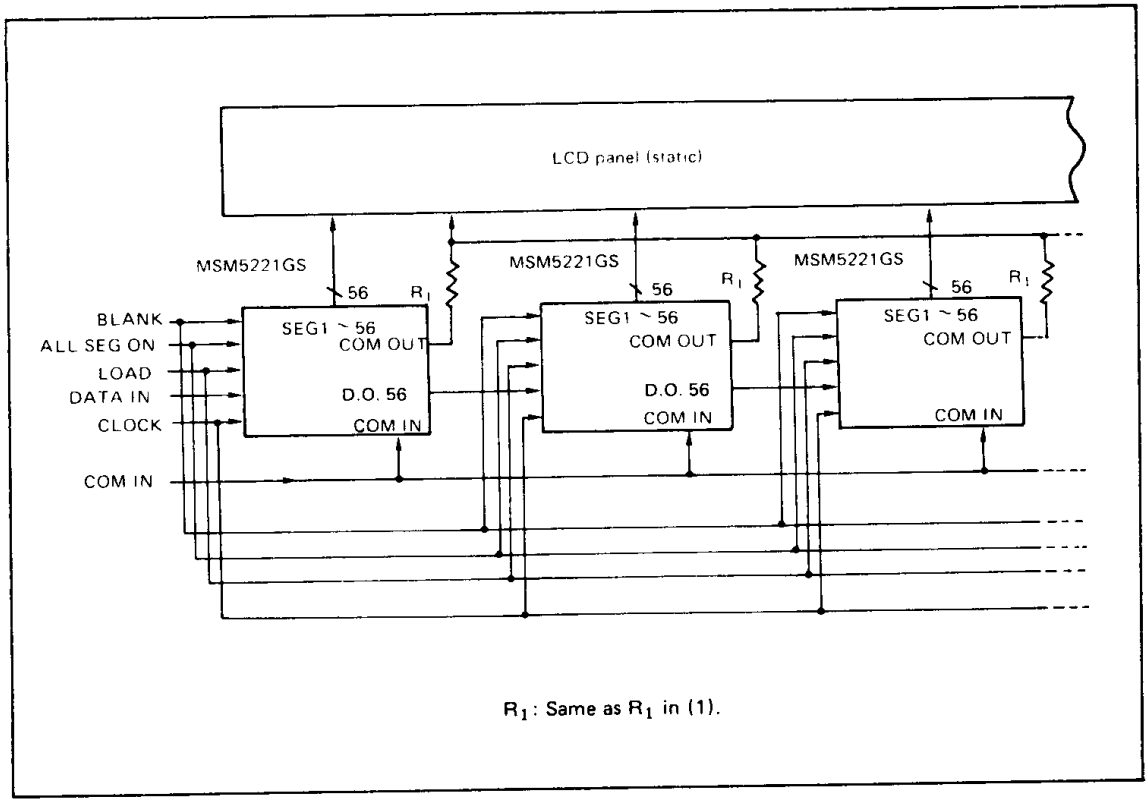
APPLICATION CIRCUIT

- **Single MSM5221GS to the LCD panel**



R_1 : A resistor is provided to prevent latch up as required.

- **Cascade connection**



R_1 : Same as R_1 in (1).