

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT MULTI-CHIP

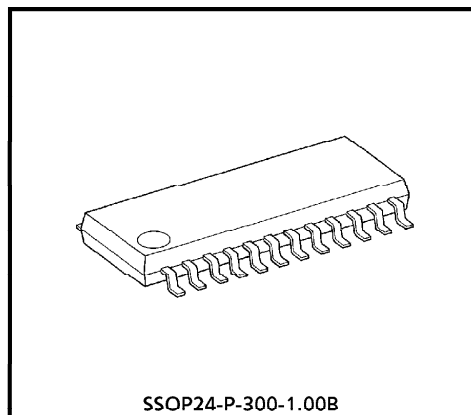
# TA8461F

## DUAL POWER OPERATIONAL AMPLIFIER

The TA8461F is a multiple chip IC consisting of 4 saturated voltage discrete transistors and 1 dual operational amplifier.

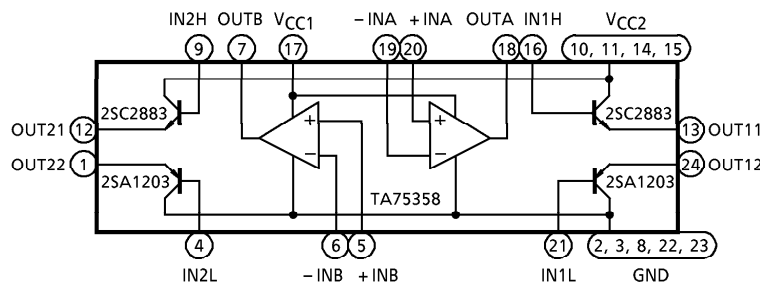
### FEATURES

- Large Output Current :  $I_{OUT} = 1.5A$  (MAX.)
- Sealed in a Small Package : SSOP24

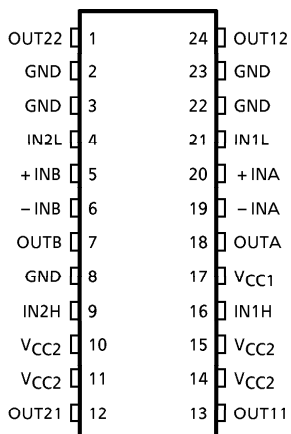


Weight : 0.27g (Typ.)

### BLOCK DIAGRAM



### PIN CONNECTION



961001EBA2

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**PIN FUNCTION**

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	OUT22	PNP (2) Emitter
2	GND	GND
3	GND	GND
4	IN2L	PNP (2) Base
5	+ INB	OP. Amp (B) input (+)
6	- INB	OP. Amp (B) input (-)
7	OUTB	OP. Amp (B) output
8	GND	GND
9	IN2H	NPN (2) Base
10	V <sub>CC2</sub>	Output transistor voltage supply
11	V <sub>CC2</sub>	Output transistor voltage supply
12	OUT21	NPN (2) Emitter
13	OUT11	NPN (1) Emitter
14	V <sub>CC2</sub>	Output transistor voltage supply
15	V <sub>CC2</sub>	Output transistor voltage supply
16	IN1H	NPN (1) Base
17	V <sub>CC1</sub>	OP. Amp. voltage supply
18	OUTA	OP. Amp. (A) output
19	- INA	OP. Amp. (A) input (-)
20	+ INA	OP. Amp. (A) input (+)
21	IN1L	PNP (1) Base
22	GND	GND
23	GND	GND
24	OUT12	PNP (1) Emitter

**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC		SYMBOL	RATING	UNIT	
Supply Voltage		V <sub>CC</sub>	30	V	
Output Transistor	Collector-Base Voltage	V <sub>CBO</sub>	30	V	
	Collector-Emitter Voltage	V <sub>CEO</sub>	30	V	
	Emitter-Base Voltage	V <sub>EBO</sub>	5	V	
	Output Current	I <sub>OUT (AVE.)</sub>	1.5	(Note 1) 3.0	A
		I <sub>OUT (PEAK)</sub>			
	Base Current	I <sub>B</sub>	0.3	A	
OP. Amp.	Amplifier Differential Input Voltage	DV <sub>IN</sub>	30	V	
	Amplifier Input Voltage	V <sub>IN</sub>	30	V	
Power Dissipation		P <sub>D</sub>	(Note 2) 1.0	W	
Junction Temperature		T <sub>j</sub>	125	°C	
Operating Temperature		T <sub>opr</sub>	- 40~85	°C	
Storage Temperature		T <sub>stg</sub>	- 55~125	°C	

(Note 1) Pulse measured : Pulse width = 10ms (MAX.)  
 Repetition cycle = 30% (MAX.)

(Note 2) No heat sink

**ELECTRICAL CHARACTERISTICS**

Output transistor unit (Ta = 25°C)

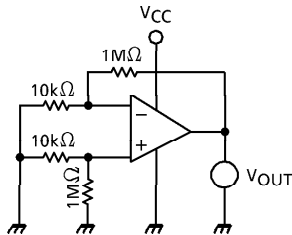
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Current Amplification Factor	h <sub>FE</sub> (1)	—	V <sub>CE</sub> = 2V, I <sub>C</sub> = 0.5A	160	—	600	
	h <sub>FE</sub> (2)	—	V <sub>CE</sub> = 2V, I <sub>C</sub> = 1.5A	50	100	—	
Output Saturation Voltage	V <sub>CE</sub> (sat) (NPN)	—	I <sub>C</sub> = 0.5A, I <sub>B</sub> = 10mA	—	0.2	0.50	V
			I <sub>C</sub> = 1.5A, I <sub>B</sub> = 30mA	—	—	2.0	
	V <sub>CE</sub> (sat) (PNP)	—	I <sub>C</sub> = 0.5A, I <sub>B</sub> = 10mA	—	0.2	0.50	
			I <sub>C</sub> = 1.5A, I <sub>B</sub> = 30mA	—	—	2.0	
Transition Frequency	f <sub>T</sub>	—	V <sub>CE</sub> = 2V, I <sub>C</sub> = 0.5A	—	120	—	MHz
Output Leakage Current	I <sub>OL</sub> (NPN)	—	V <sub>CC</sub> = 30V	—	0	10	μA
	I <sub>OL</sub> (PNP)	—	V <sub>CC</sub> = 30V	—	0	10	
Base-Emitter Voltage	V <sub>BE</sub> (NPN)	—	V <sub>CE</sub> = 2V, I <sub>C</sub> = 0.5A	—	—	1.0	V
	V <sub>BE</sub> (PNP)	—	V <sub>CE</sub> = 2V, I <sub>C</sub> = 0.5A	—	—	1.0	

Operational amplifier unit (V<sub>CC</sub> = 5V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V <sub>IO</sub>	1	R <sub>g</sub> ≤ 10kΩ	—	2	7	mV
Input Offset Current	I <sub>IO</sub>	2	—	—	5	50	nA
Input Bias Current	I <sub>I</sub>	2	—	—	45	250	nA
In-Phase Input Voltage	CMV <sub>IN</sub>	3	V <sub>CC</sub> = 30V	0	—	V <sub>CC</sub> - 1.5	V
Supply Current	I <sub>CC</sub>	4	R <sub>L</sub> = ∞, ALL OP Amps	—	0.7	1.2	mA
Voltage Gain	G <sub>V</sub>	5	R <sub>L</sub> ≥ 2kΩ	86	100	—	dB
Maximum Output Amplitude Voltage	V <sub>Op-p</sub>	6	R <sub>L</sub> = 2kΩ	0	—	V <sub>CC</sub> - 1.5	V
Common Mode Rejection Ratio	CMRR	3	—	60	85	—	dB
Supply Voltage Rejection Ratio	SVRR	1	R <sub>g</sub> ≤ 10kΩ	60	100	—	dB
Source Current	I <sub>source</sub>	6	IN (-) = 0V <sub>DC</sub> , IN (+) = 1V <sub>DC</sub>	20	40	—	mA
Sink Current	I <sub>sink</sub>	6	IN (-) = 0V <sub>DC</sub> , IN (+) = 1V <sub>DC</sub>	10	20	—	mA
Cut-off Frequency	f <sub>T</sub>	—	—	—	1.5	—	MHz
Slew Rate	S <sub>R</sub>	—	—	—	0.8	—	V / μs

TEST CIRCUIT

(1)  $V_{IO}$ , SVRR

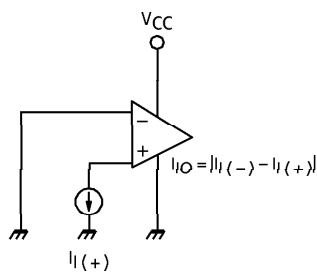
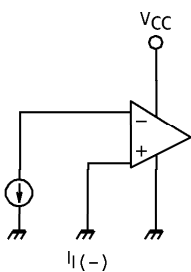


- $V_{IO} = V_{OUT} / 100$
- $SVRR = 20 \log E$  (dB)

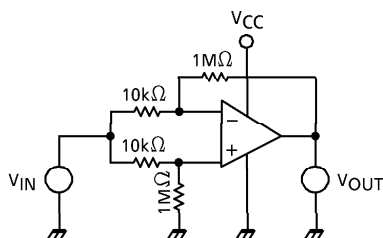
$$E = \left| \frac{V_{OUT1} - V_{OUT2}}{V_{CC1} - V_{CC2}} \right| \times \frac{1}{100}$$

$V_{OUT1}$  :  $V_{OUT}$  ( $V_{CC1} = 5V$ )  
 $V_{OUT2}$  :  $V_{OUT}$  ( $V_{CC2} = 10V$ )

(2)  $I_I$ ,  $I_{IO}$

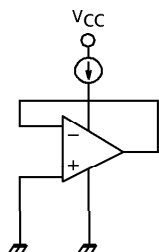


(3)  $CMV_{IN}$ , CMRR



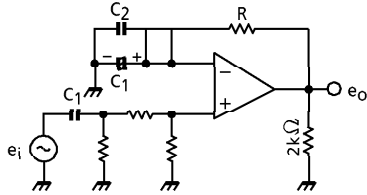
- $CMRR = 20 \log G_D / G_C$  (dB)  
 $G_D$  : Differential Voltage Gain  
 $G_C$  : In-phase Voltage Gain
- $CMV_{IN}$  :  $V_{IN} = 0V$ ,  $V_{CC} = 1.5V$

(4)  $I_{CC}$



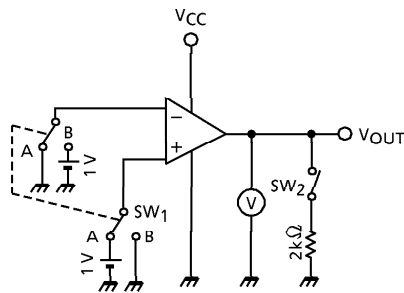
- $I_{CC}$  :  $V_{CC} = 5V$

(5)  $G_V$



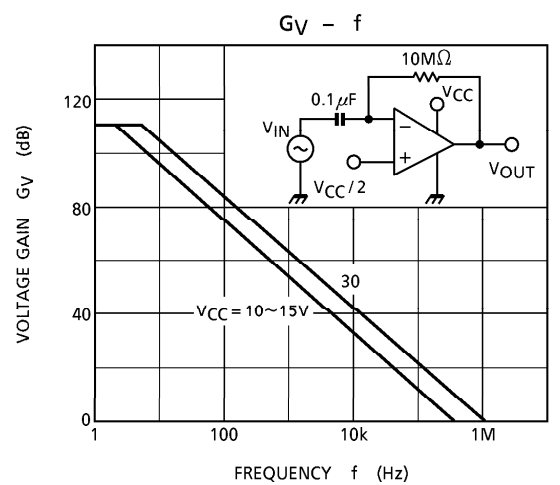
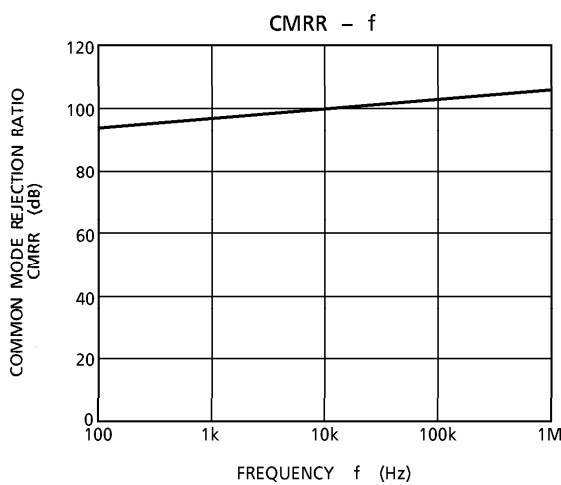
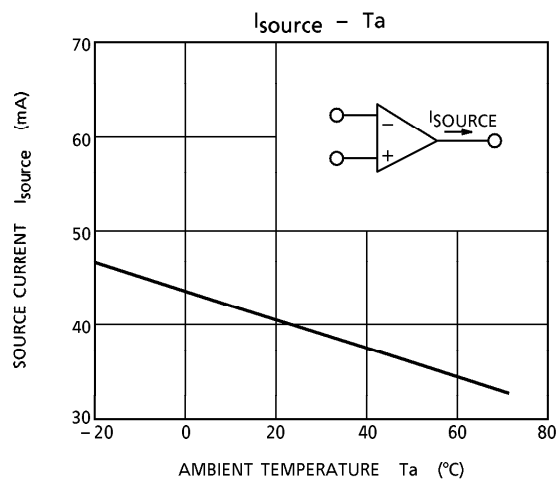
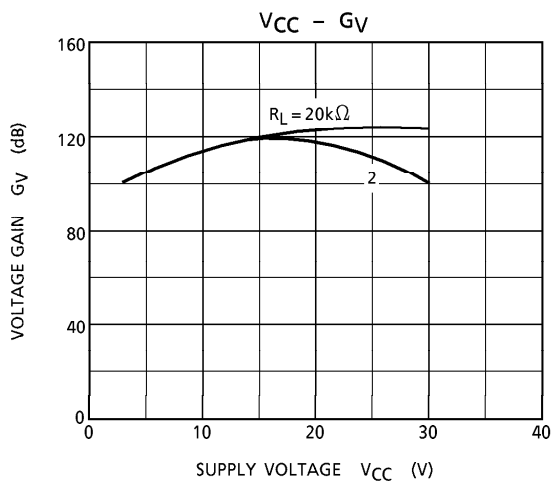
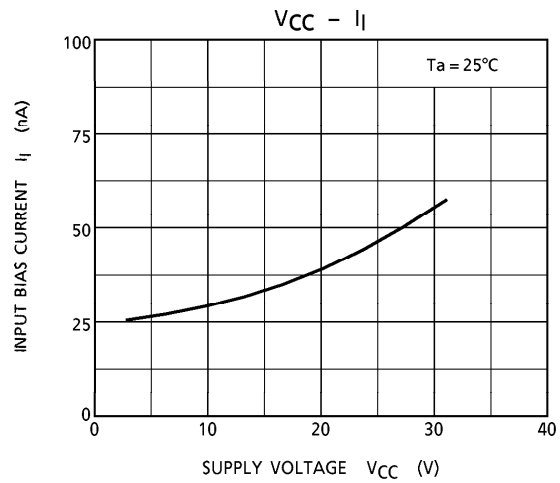
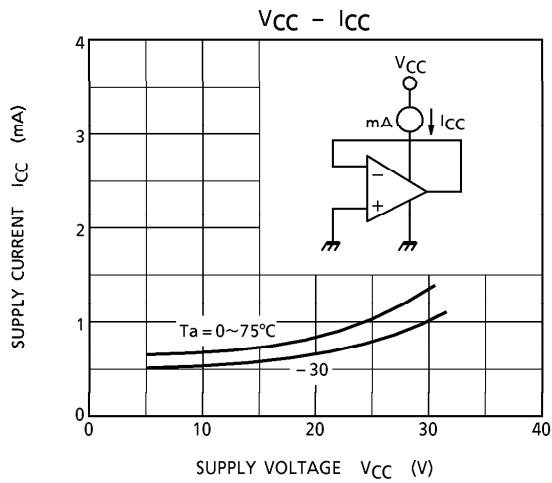
- $G_V = 20 \log e_o / e_i$  (dB)
- $R \gg 1 / \omega C_1$
- $C_1$  : For Preventing DC Short-Circuit.
- $C_2$  : For High Frequency Short-Circuit.
- Use a Mica or Titanium Capacitor.

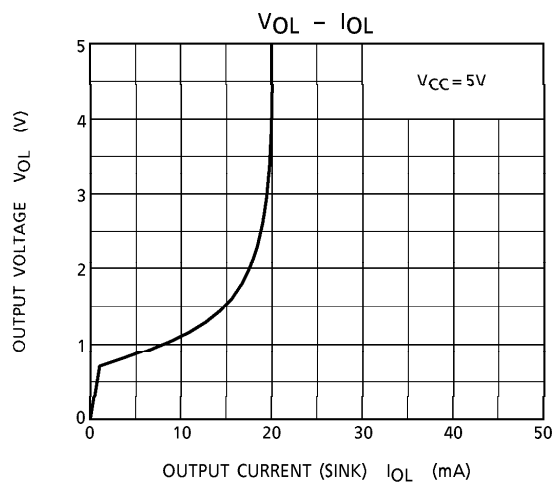
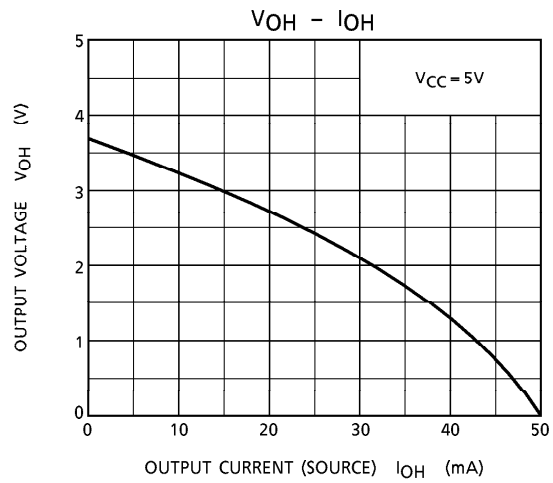
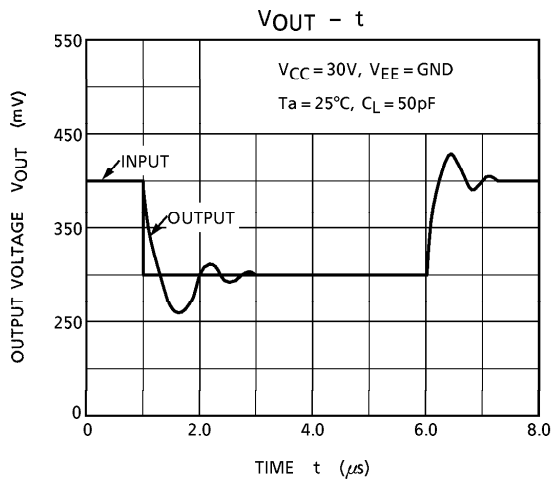
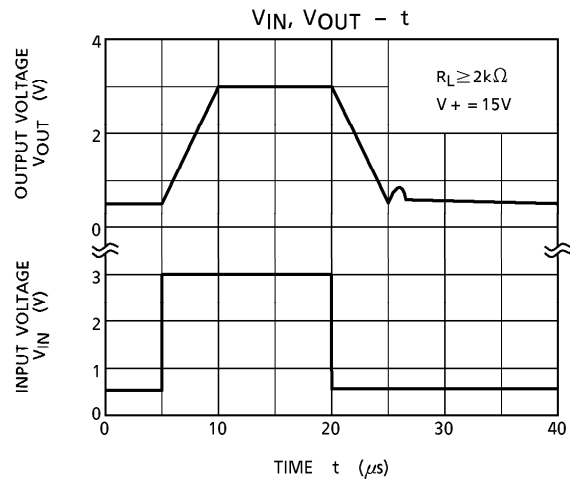
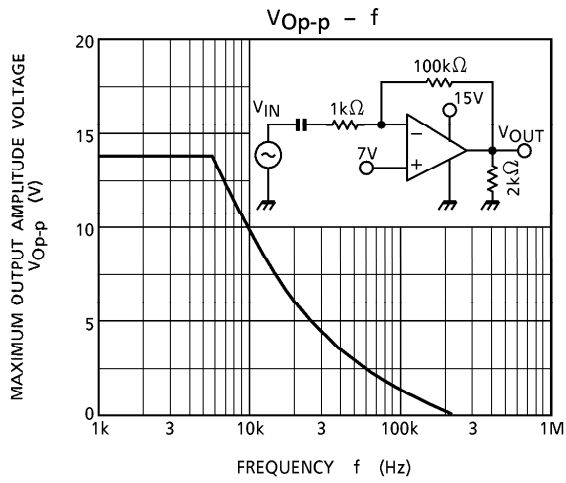
(6)  $V_{Op-p}$ ,  $I_{source}$ ,  $I_{sink}$



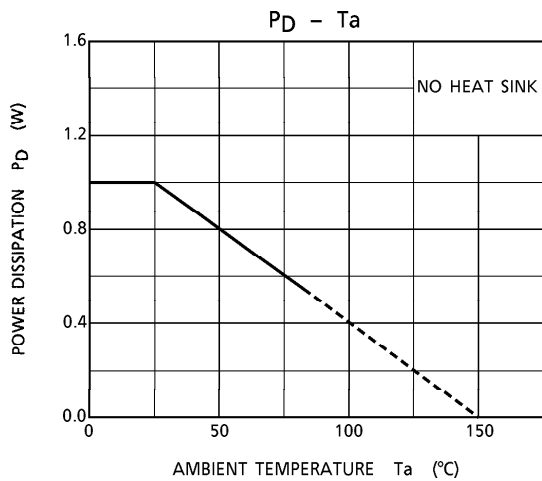
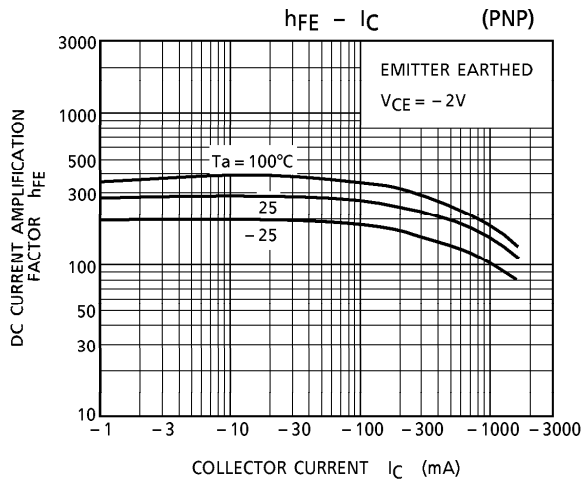
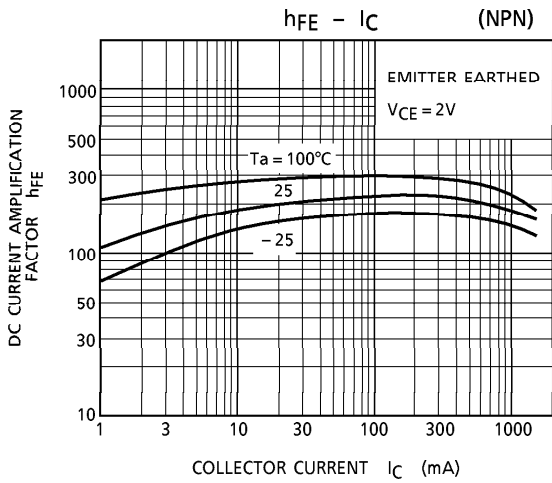
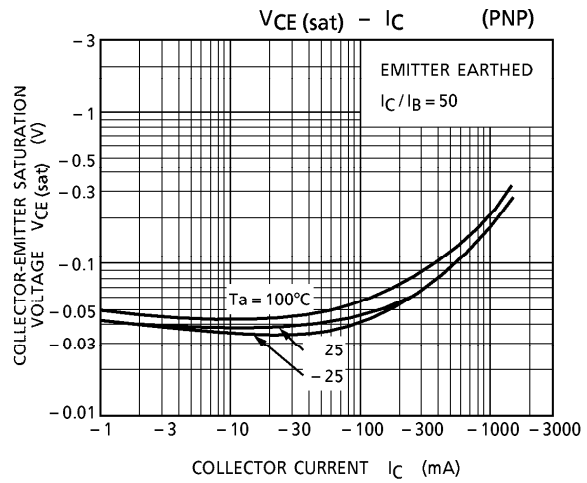
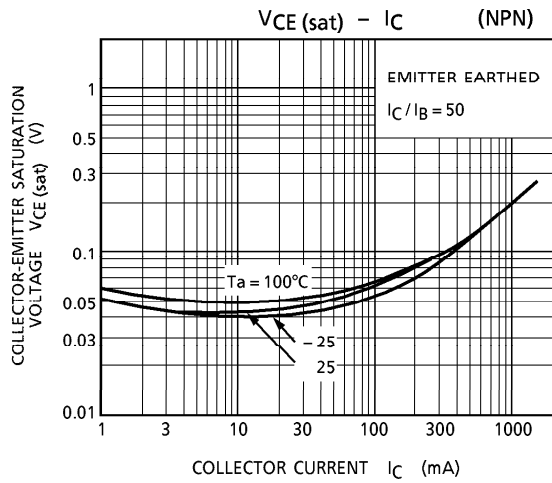
- $V_{Op-p}$ 
  - $V_{OH}$  : SW<sub>1</sub> is to A side.
  - $V_{OL}$  : SW<sub>1</sub> is to B side.
- $I_{source}$ 
  - SW<sub>1</sub> is to A side.
  - $V_{OUT} \rightarrow 0V$  Measurement
- $I_{sink}$ 
  - SW<sub>1</sub> is to B side.
  - $V_{OUT} \rightarrow 5V$  Measurement

**CHARACTERISTIC CURVES** ( $T_a = 25^\circ\text{C}$ )  
 (1) Operational amplifier





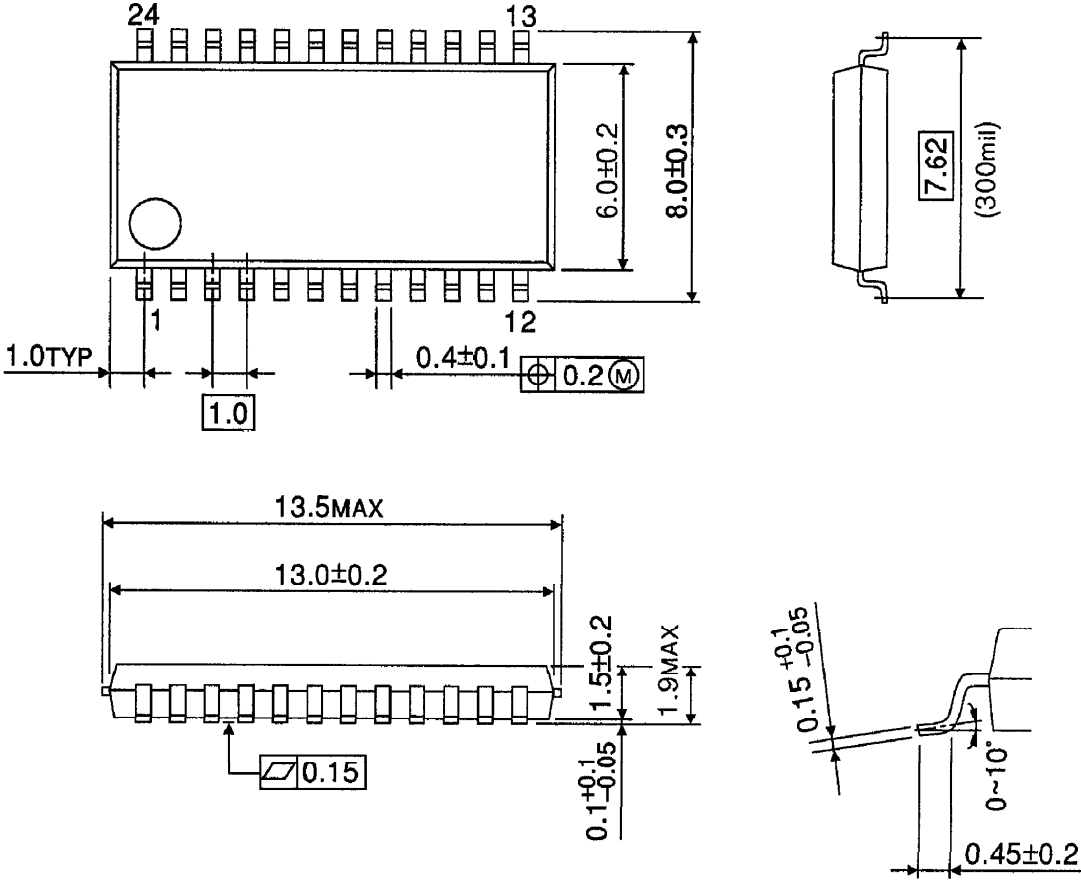
(2) NPN transistor, PNP transistor





OUTLINE DRAWING  
SSOP24-P-300-1.00B

Unit : mm



Weight : 0.27g (Typ.)