Multi-Channel Audio CODEC

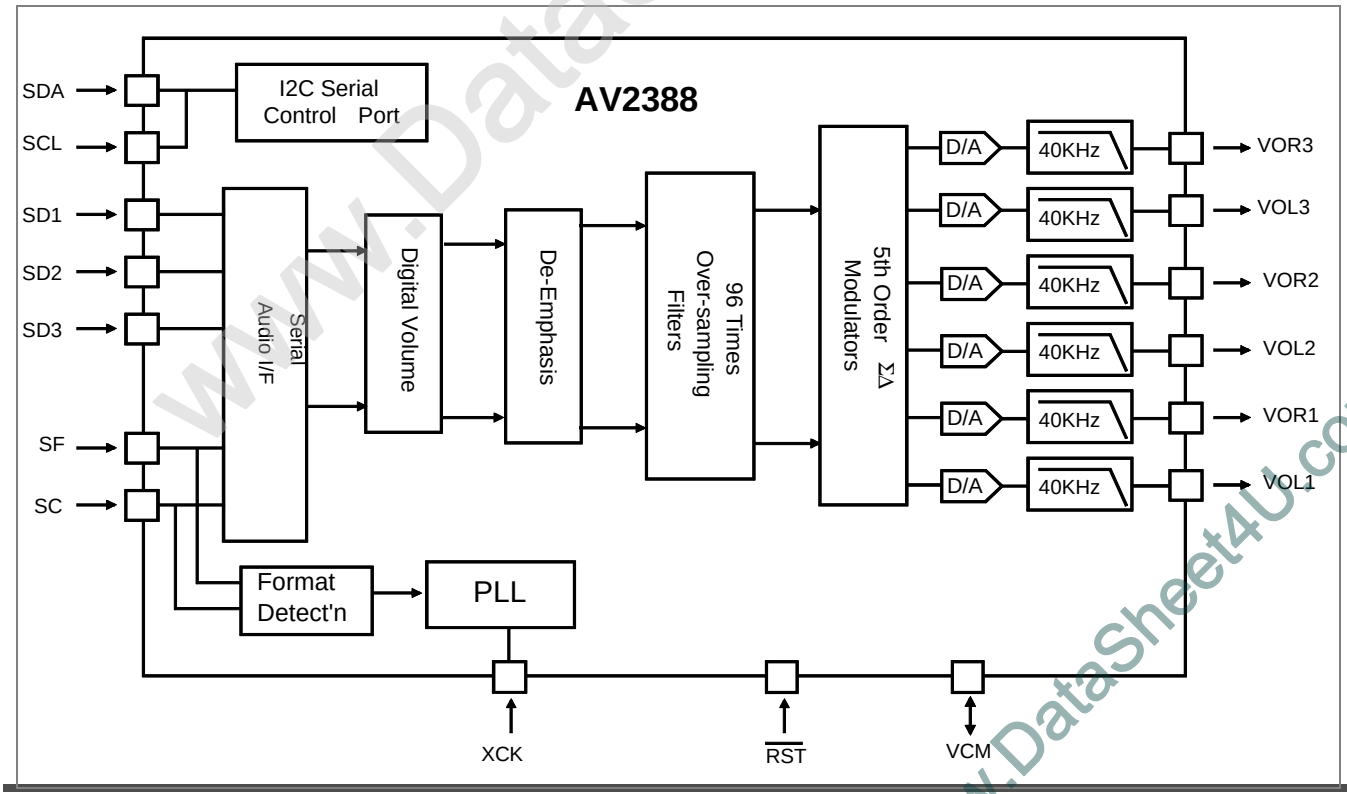
FEATURES

- Six Channel 24/20-bit DACs.
  - 102 dB SNR
  - 104 dB Dynamic Range.
  - -92 dB THD + N Ratio.
  - 32,44.1, 48, 96 and 192KHz. Sampling rates.
  - 24, 20, 18 and 16-bit Digital Inputs.
  - Containing Digital De-emphasis Filters.
  - Independent Digital Volume Control.
  - I^2S, Left and Right Justified Digital Input Formats.
  - Auto-Mute Control.
  - On -chip Reconstruction Filters.
  - -96 dB THD + N Ratio.
  - I^2S and Left Justified Output Formats.
- System clock: 384 fs or 256 fs for 32, 44.1 48, 96 and 192KHz. Sampling Rates, 192 fs or 128 fs for 96 KHz Sampling Rates. and 86 fs or 64 fs for 192 KHz. Sampling Rate.
- Automatic input format detection.
- 5-volt Power Supply.
- 3.3 -volt Digital Interface Friendly.
- I^2C Interface for Mode Setting.

Applications

- Digital Surround Sound For Home Theater
- DVD
- Car Audio.

- 28 pin SOP package



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Item	PERFORMANCE SPECIFICATIONS	Spec.
	Audio DAC	
1	Audio Output Level	1 Vrms
2	Audio Bandwidth 20Hz - 20 KHz	+/- 0.1 dB
3	SNR (A-weight, Muted)	>102 dB
4	SNR (A-weight, Not Muted)	>96 dB
6	THD + N (A-weight, FFS Output)	< -92 dB
7	Dynamic Range	104 dB
8	Channel Separation	< -96 dB
9	Nonlinear Distortion	< 0.25 dB
10	Channel Gain Error	< 0.1 dB

All Measurement were taken with only one channel active.

DESCRIPTION

The AV2388 is a mixed signal CMOS monolithic audio CODEC. It consists of six channels sigma delta DACs The DACs support 24, 20, 18 and 16-bit input data. It also support multiple sampling frequency data. Each DAC has it own individual volume control.

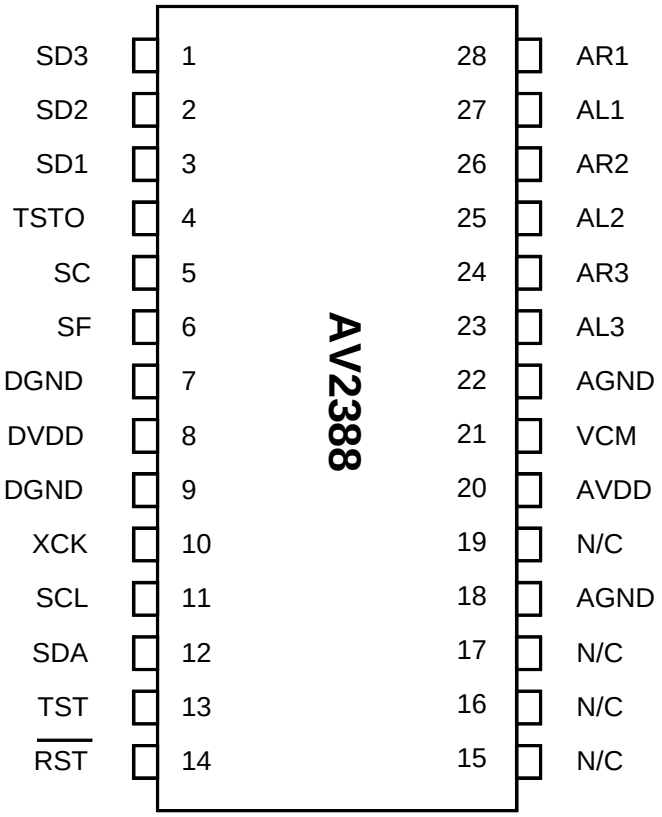
XCK REQUIREMENT

The AV2388 supports 384 and 256 times sampling clock for 32, 44.1, 48, 96 and 192K audio; 192 or 128 times for the 96 K audio.; and 96 and 64 times for the 192K audio.

XCK Requirement

Sampling Rate	XCK Freq.					
	PLLcntl=[0 0]		PLLcntl=[1 0]		PLLcntl=[0 1]	
	Normal XCK		4 times XCK		2 times XCK	
	384*fs	256*fs	4*384*fs	4*256*fs	2*384*fs	2*256*fs
32 K	12.288 MHz	8.192 MHz	49.152 MHz	32.768 MHz	24.576 MHz	16.384 MHz
44.1	16.934 Mhz	11.29 Mhz.	67.738 Mhz	45.158 Mhz.	33.869 Mhz	22.579 Mhz.
48 K	18.432 MHz	12.288 Mhz.	73.728 MHz	49.152 Mhz.	36.864 MHz	24.576 Mhz.
96 K	18.432 MHz	12.288 Mhz.	73.728 MHz	49.152 Mhz.	36.864 MHz	24.576 Mhz.
192 K	18.432 Mhz	12.288 Mhz.	73.728 Mhz	49.152 Mhz.	36.864 Mhz	24.576 Mhz.

PIN ASSIGNMENT



PIN DESCRIPTION

Pin Name	Pin #	Type	Description
DIGITAL			
SD3	1	I	Audio Serial Data Input 3.
SD2	2	I	Audio Serial Data Input 2.
SD1	3	I	Audio Serial Data Input 1,..
TSTO	4	O	Test output pin. This pin should be no be connected.
SC	5	I	Audio Serial Data Clock pin.
SF	6	I	Left/Right Channel Clock pin. For Left justified or Right justified mode, a high in SF indicates Left Channel Data, a low in SF indicates Right Channel Data. For I2S mode, a low in SF indicates Left Channel Data, a high in SF indicates Right Channel Data.
DGND	7	GND	Digital ground
DVDD	8	+5V	Digital power supply.
DGND	9	GND	Digital ground
XCK	10	I	External Master Clock Input.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
SCL	11	I	I2C clock input.
SDA	12	I/O	I2C DATA bus. Open drain output. Externally this pin should tie to a 680 ohm pull up resistor.
TST	13	O	Test fs reference pin. For test vector verification. For normal operation this pin must be tied to '0'.
$\overline{\text{RST}}$	14	I	Active low power down reset. When low, the chip is reset and all programmable registers are reset to default values.

Analog

AR1	28	O	Analog right channel 1 output
AL1	27	O	Analog left channel 1 output
AR2	26	O	Analog right channel 2 output.
AL2	25	O	Analog left channel 2 output.
AR3	24	O	Analog right channel 1 output.
AL3	23	O	Analog left channel 1 output.
AVSS	22	GND	Analog circuits ground
VCM	21		Common voltage output pin for the DAC.
AVDD	20	+5V	Analog circuits power supply
N/C	19		No connection. Can be tied to AVSS
AGND	18	GND	Analog circuits ground
N/C	17	I	No connection. Can be tied to AVSS
N/C	16	I	No connection. Can be tied to AVSS
N/C	15		No connection, Can be tied to AVSS

DIGITAL AUDIO SERIAL INTERFACE

The digital serial interface consists of 3 serial input pins, SD1, SD2, SD3, and one serial clock input pin, SC, and one left/right indicator input pin, SF. The data are 2's complement MSB first numbers. The AV2388 supports four resolution, which are selected either by setting the FMT[1] and FMT[0] pins or by programming the control register CREG0[5:4] via the I^2C serial control port. Table 1 describes these four resolution.

Table (1): Audio Serial Data Input Format,

Format	CREG0[5]	CREG0[4]	SD1, SD2, and SD3
0	0	0	24-bit
1	0	1	20-bit
2	1	0	18-bit
3	1	1	16-bit

The SD3, SD2 and SD1 can be either 24-bit or 32-bit per frame as well as left justified, right justified or I2S. The AV2388 counts the number of BCK per frame to determine whether the input is 24 or 32 bits format.

Table (1): Audio Serial Data Input Modes

Mode	CREG0[7]	0REG0[6]	SD1, SD2, and SD3
0	0	0	Right Justified
1	0	1	I2S
2	1	0	Left Justified
3	1	1	Invalid

Figure 1. Audio Serial Input Data Timing Diagram

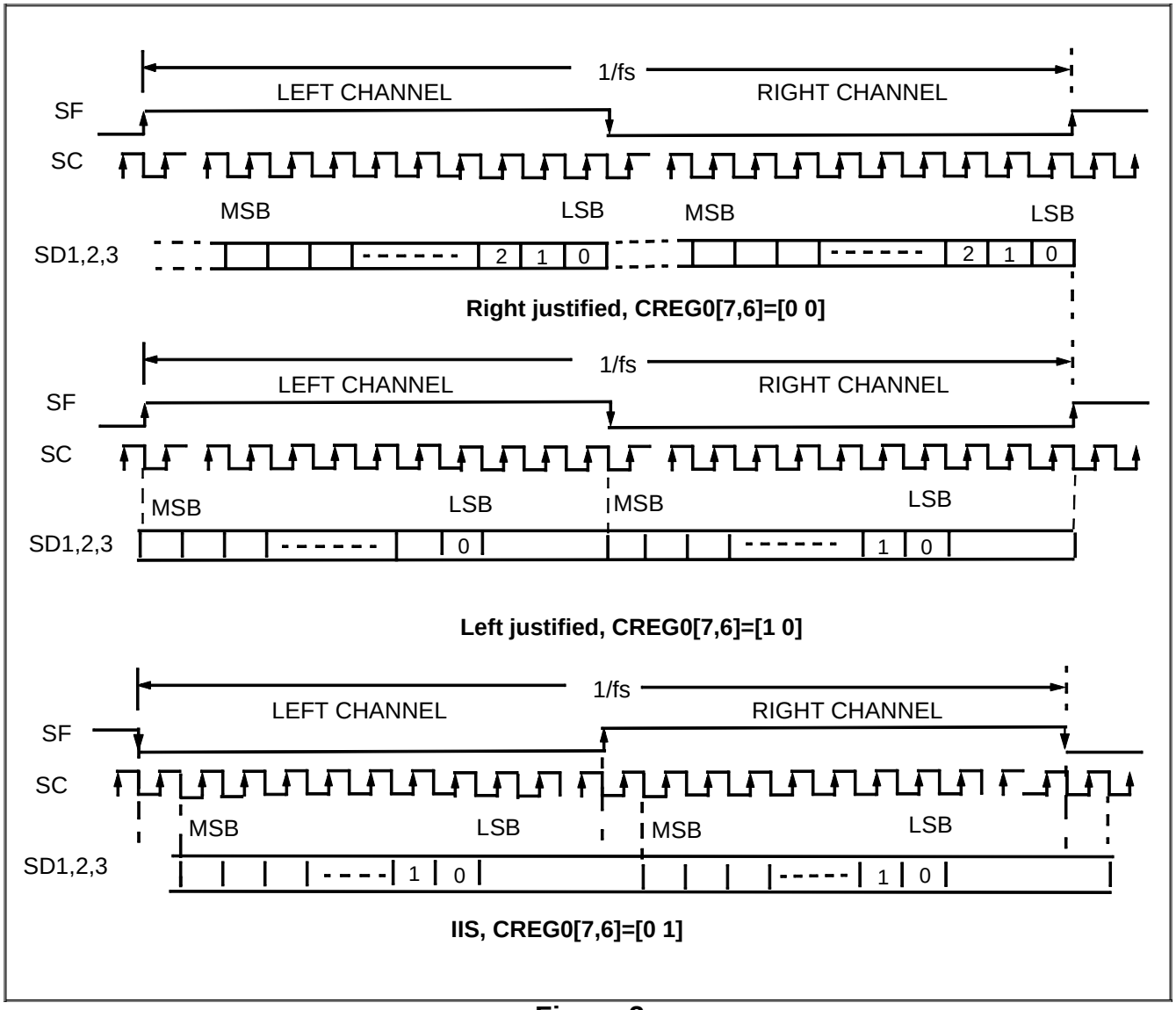
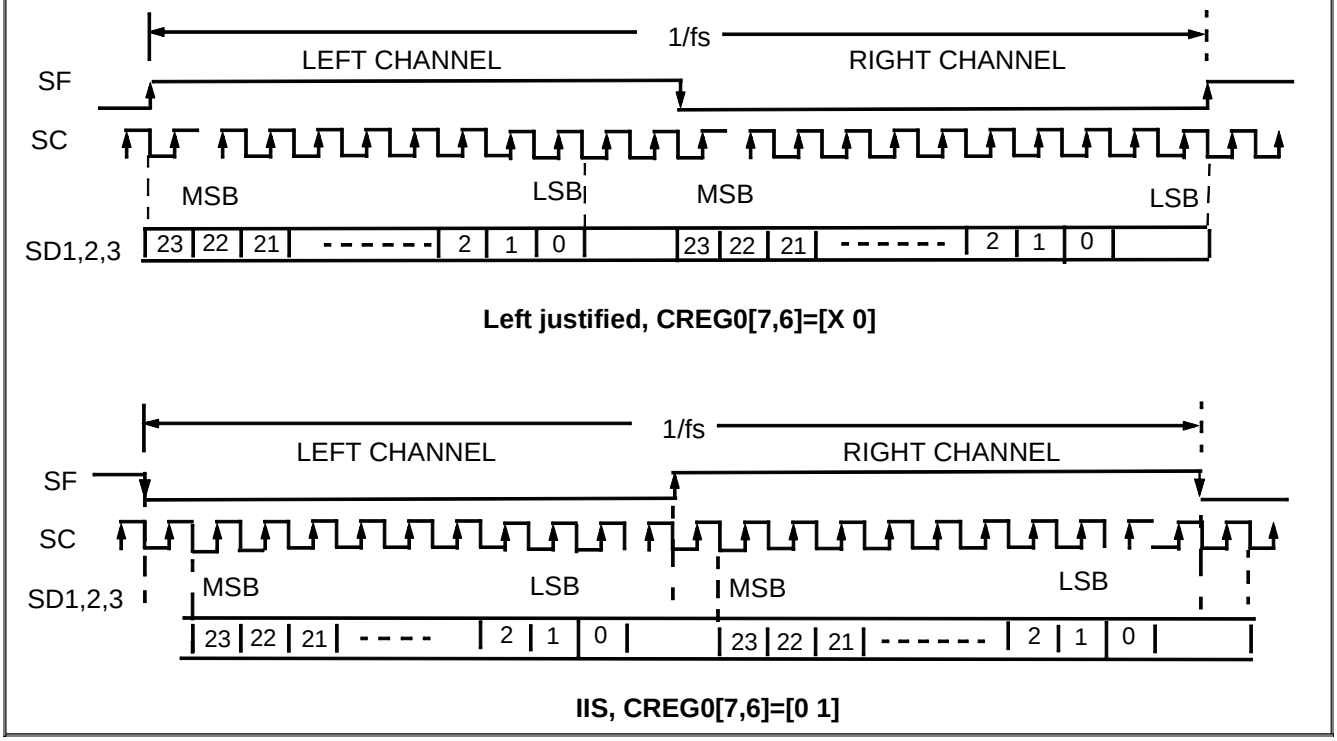


Figure 2.

Figure 3. Audio Serial Output Data Timing Diagram



INFINITE ZERO DETECTION

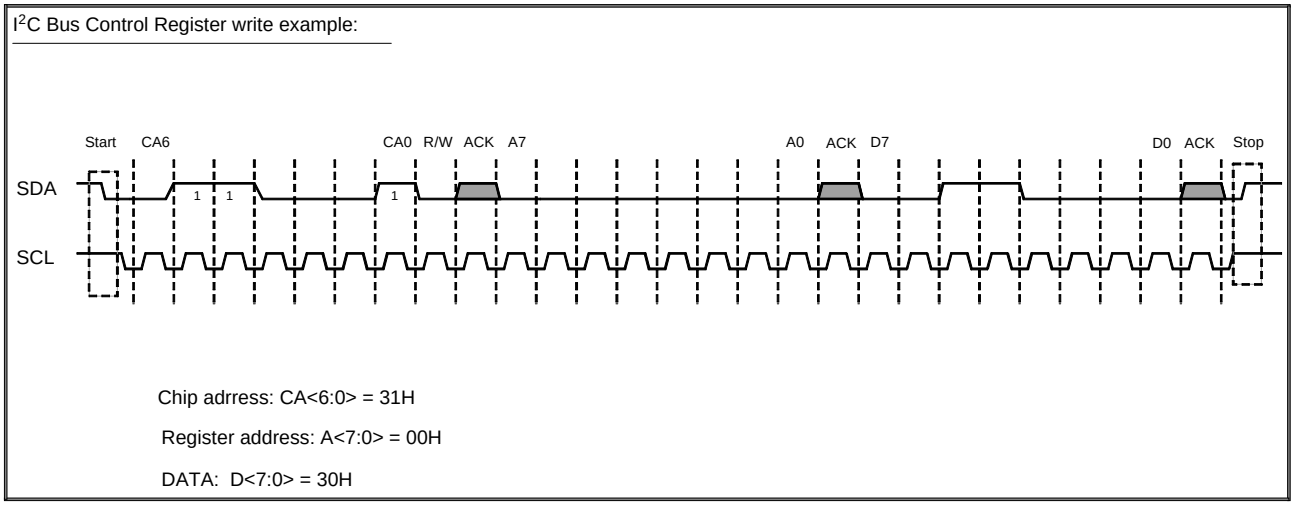
The AV2388 has an Infinite Zero Detection circuit which detects zero in the Audio Serial Port that lasts for approximately 0.5 sec. By default, the zero detection circuit is on.

Serial Command Port

The user can use the pin to select the chip operation or by programming the internal control registers through the 7 bit address I^2C port. The Chip Address for the AV2388 is 31H. The protocol for write operation consists of sending 3 byte data to AV2388, following each byte are the acknowledges generated by AV2388. The first byte is the 7-bit Chip Address followed by the read/write bit (read is high write is low). The second byte is the control register address. The third byte is the control register data.

Upon power up, all programmable registers are set to default values. Figure 4 describes the serial command port timing relationship.

Figure 4. Serial Command Port Timing



SERIAL PORT CONTROL REGISTER ASSIGNMENT

There are 10 registers dedicated to the AV2388 for chip functional programming,. One register for testing. The register addresses assignments are

Address (decimal)	Register	Default Value	Register Function
0	CREG0[7:0]	80	Data input format, de-emphasis filter selection
1	CREG1[7:0]	80	Input format and PLL output frequency selection
2	VOLREG0[7:0]	80	Volume control for channel 1, left
3	VOLREG1[7:0]	80	Volume control for channel 1, right
4	VOLREG2[7:0]	80	Volume control for channel 2, left
5	VOLREG3[7:0]	80	Volume control for channel 2, right
6	VOLREG4[7:0]	80	Volume control for channel 3, left
7	VOLREG5[7:0]	80	Volume control for channel 3, right
8	MUTE[5:0]	00	Mute control register.
9	TREG1[7:0]	00	Test control

CONTROL REGISTERS DESCRIPTION

Control Register 0(ADRS=hex00, default=hex80)

ADDR[4:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 00	LT	IIS	FMT[1:0]		AMUTE	AMPX2	FIRSL[1:0]	
Default Value	1	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[LT, IIS] Digital Serial Bus Format Select
- 00: - Normal or Right Justified Format.
- 01: - I2S Format.
- 10: - Left Justified Format. (default)
- 11: - Not allowed.

FMT[1:0]: - These two bits define the serial audio input resolution
- 00: - 24-bit resolution. (default)
- 01: - 20-bit resolution.
- 10: - 18-bit resolution.
- 11: - 16-bit resolution.

AMUTE: - Active low auto-mute detection enable.
- 0: - Auto-mute enabled. (default)
- 1: - No auto-mute.

AMPX2: - Multiplied the Volume by two.
- 0: - Normal. (default)
- 1: - Volume is doubled. Should be used with Pre-De-emphasis track.

DEML: - De-emphasis Control
- 00: - No De-emphasis. (default)
- 01: - Select 44.1K De-emphasis filter.
- 10:- Select 48 K De-emphasis filter.
- 11: - Select 44.1K and 36K sampling filter: No De-emphasis.

Control Register 1 (ADRS=hex01, default=hex80)

ADDR[4:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 01	Autodet	zero	fs384	px4s	px2s	zero	PLLcntl1	PLLcntl0
Default Value	1	0	0	0		0	0	0
R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W

Autodet: Input format auto detection enable
0 - disable input format detection. The user need to program bit[5:3] in order to select the input format and filters for 96K and 192K sampling.
1 - enable input format detection.

F384: XCK frequency.
0 -XCK is 384 times the bit clock, SCK.
1 - XCK is 256 times the bit clock, SCK.

[Px4s Px2s]: Higher sampling filter selection.
[0 0] - normal sampling.
[0 1] - 2 times over sampling filter enable.
[1 0] - 4 times over sampling filter enable.
[1 1] - invalid.

PLLcntl[1:0]:System clock PLL control.
[0 0] - normal sampling XCK input.
[0 1] - 2 times XCK input.
[1 0] - 4 times XCK input.
[1 1] - invalid

Volume Registers for channel 1 to channel 3, (ADRS=hex02 - hex07, default=hex80)

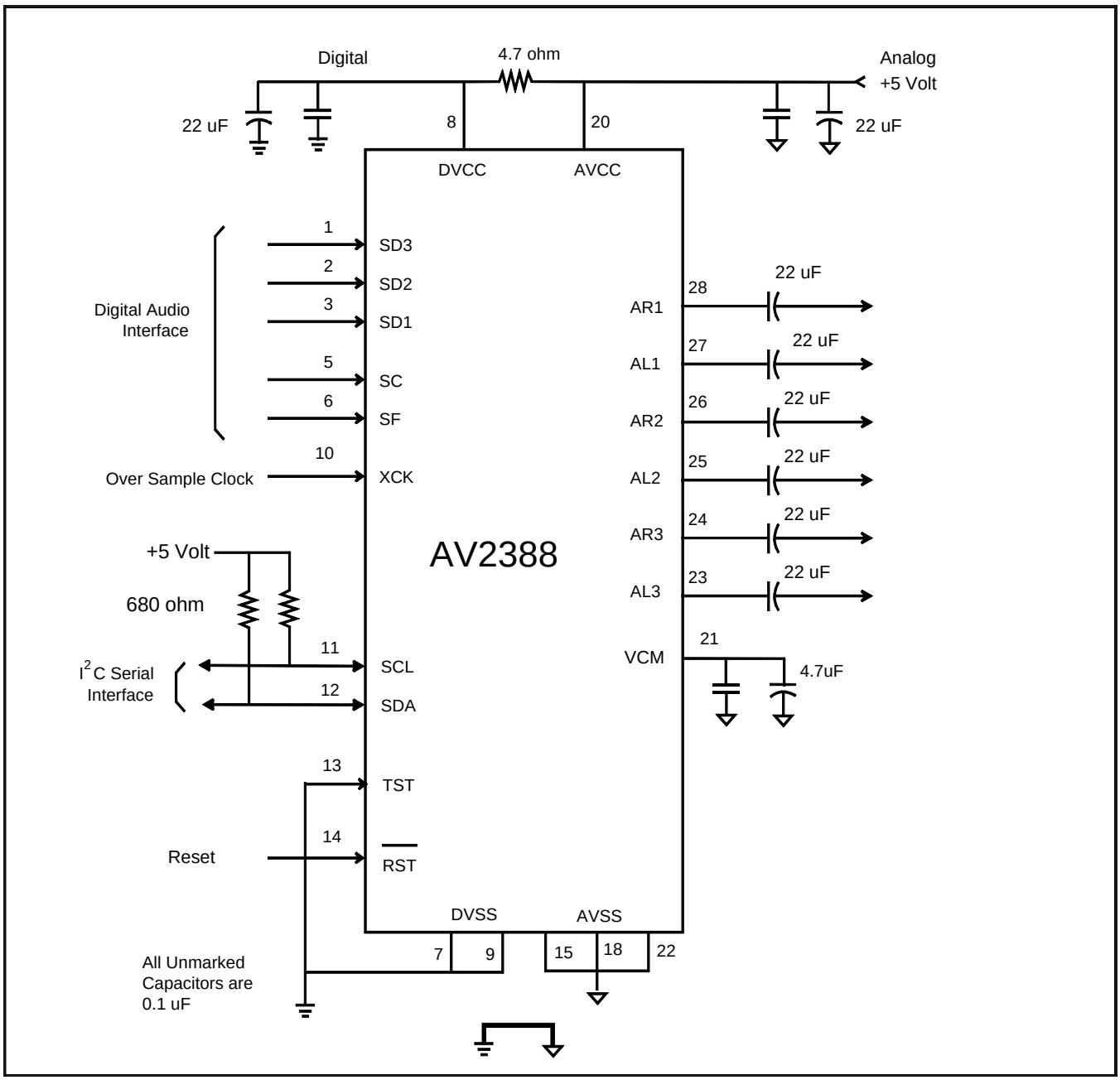
ADDR[4:0]	Volume Registers							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 02	Channel 1 left volume register, VLREG0L[7:0]							
Hex 03	Channel 1 right volume register, VLREG0R[7:0]							
Hex 04	Channel 2 left volume register, VLREG1L[7:0]							
Hex 05	Channel 2 right volume register, VLREG!1R[7:0]							
Hex 06	Channel 3 left volume register, VLREG2L[7:0]							
Hex 07	Channel 3 right volume register, VLREG2RL[7:0]							
Default Value	1	0	0	0	0	0	0	0

VOLREG:- Control the volume of the 6 DAC's
80h- corresponds to 0 dB setting. Value should not be programed greater than 80h.

Mute Reg (ADRS=hex10, default=hex80)

ADDR[4:0]	Mute[5:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 01			Mute3R	Mute3L	Mute2R	Mute2L	Mute1R	Mute1L
Default Value		0	0	0		0	0	0
R/W	R/W		R/W	R/W		R/W	R/W	R/W

Application Connection Example:



TIMING DIAGRAM

Figure 5. Audio Serial Interface Timing Requirement

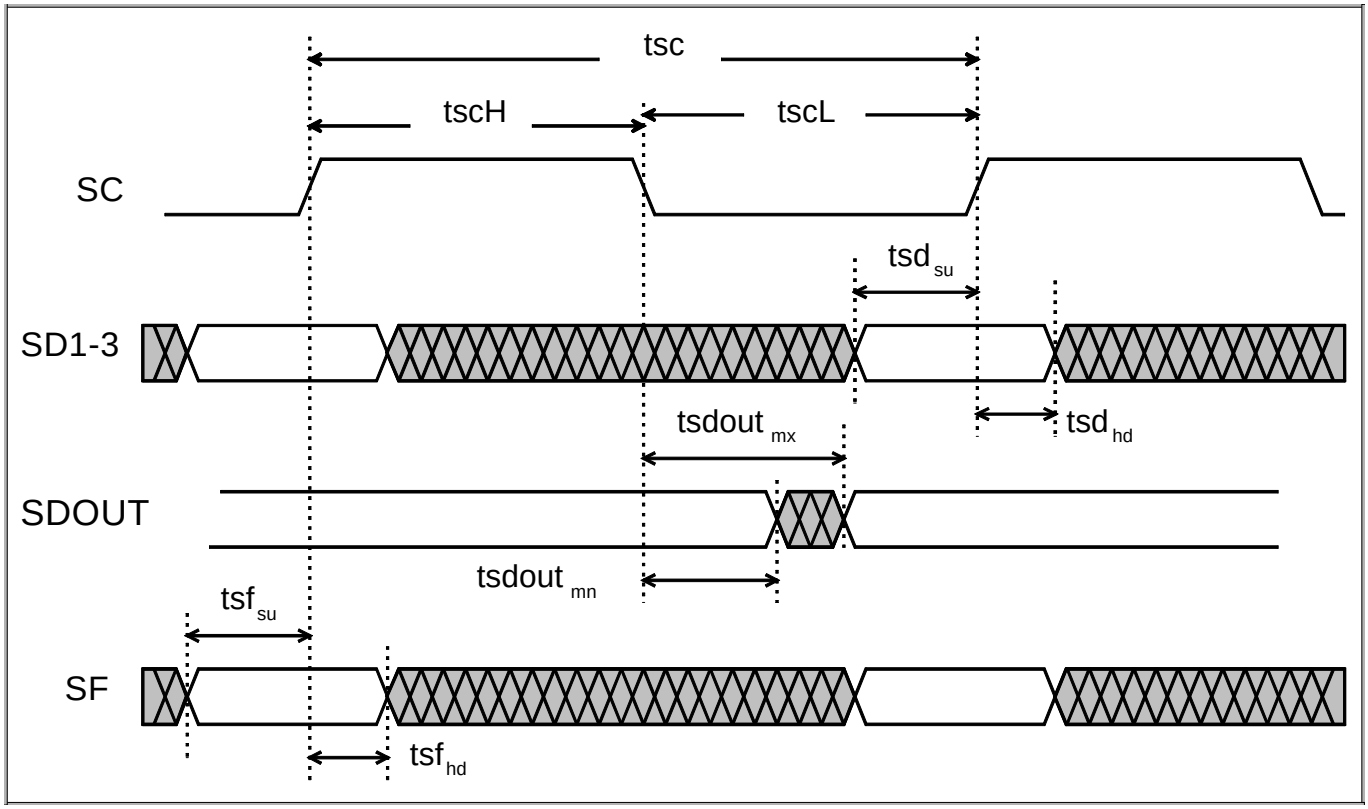


Figure 6. Serial Command Port Write Timing Requirement

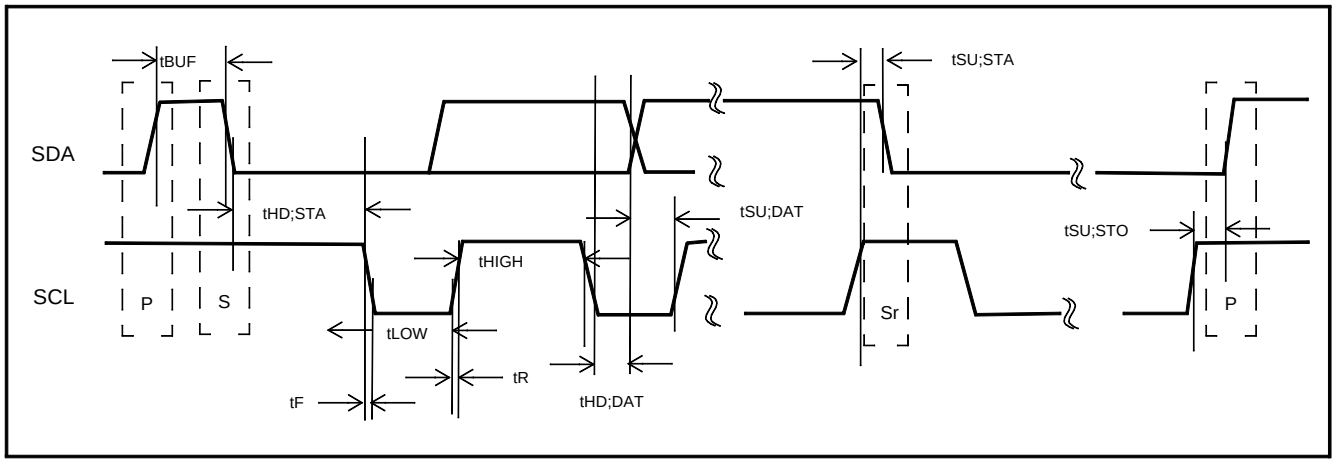
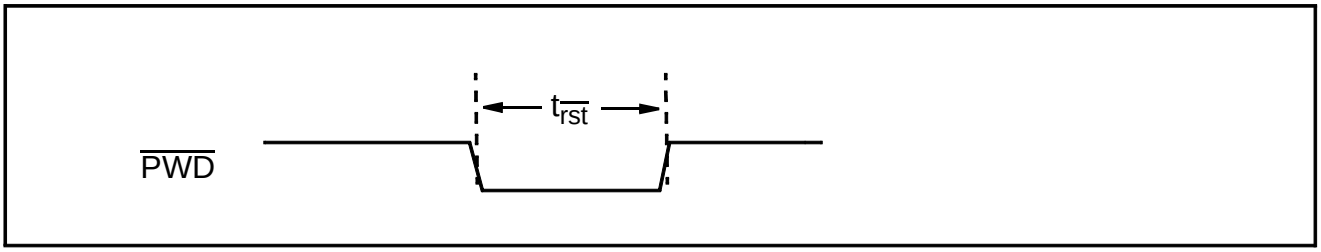


Figure 7. Power Down / Reset Timing



ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Units
V_{DD}	Power Supply Voltage (Measured to GND)	-0.5	+7.0	V
V_i	Digital Input Applied Voltage[2]	GND-0.5		V
A_i	Digital Input Forced Current[3,4]	-100	100	mA
V_o	Digital Output Applied Voltage[2]	GND-0.5	V_{DD}+0.5	V
A_o	Digital Output Forced Current[3,4]	-100	100	mA
TDsc	Digital Short Circuit Duration (single output high state to Vss)		1	Sec
TA_{SC}	Analog Short Circuit Duration (single output to VSS1)		infinite	Sec
T_a	Ambient Operating Temperature Range	-25	+125	^oC
Tstg	Storage Temperature Range	-65	+150	^oC
T_j	Junction Temperature (Plastic Package)	-65	+150	^oC
Tsol	Lead Soldering Temperature (10 sec., 1/4” from pin)		300	^oC
Tvsol	Vapor Phase Soldering (1 minute)		220	^oC
T_{stor}	Storage Temperature	-65	+150	^oC

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.

2. Applied voltage must be current limited to specified range, and measured with respect to VSS.

3. Forcing voltage must be limited to specified range.

4. Current is specified as conventional current, flowing into the device.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Typical	Max	Units
V_{DD}	Power supply voltage	4.5	5	5.5	V
V_{VCM}	Reference voltage		2.25	2.41	V
R_L	Analog output load		37.5	70	Ω
T_a	Ambient operating temperature range	0		70	°C

ELECTRICAL CHRACTERISTICS

Parameter	Characteristics	Min	Typ	Max	Units
Supply					
I_{DD}	Total Power Supply Current, Analog + Digital		135	145	mA
Digital Characteristics					
V_{IH}	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V_{DD}	V
V_{IL}	Digital Input Voltage, Logic LOW, TTL Compatible Inputs	V_{SS}		0.8	V
I_{IH}	Digital Input Current, Logic HIGH, (V_{IN}=4.0V)			10	µA
I_{IL}	Digital Input Current, Logic LOW, (V_{IN}=0.4V)			-10	µA
C_{IN}	Digital Input Capacitance (f=1Mhz, V_{IN}=2.4V)			7	pF
V_{OH}	Digital Output Voltage, Logic HIGH, (I_{OH}= -1mA)	3.2	3.4	3.5	V
V_{OL}	Digital Output Voltage, Logic LOW, (I_{OL}=4.0 mA)	V_{SS}		0.4	V
I_{OZH}	Hi-Z Leakage Current, HIGH, V_{DD}=Max, V_{IN}=$V_{DD)}$			10	µA
I_{OZL}	Hi-Z Leakage Current, LOW, V_{DD}=Max, V_{IN}=$V_{SS)}$			-10	µA
C_I	Digital Input Capacitance (T^A=25°C, f=1Mhz)			8	pF
C_O	Digital Output Capacitance (T^A=25°C, f=1Mhz)			10	pF

Parameter	Characteristics	Min	Typ	Max	Units
Audio Serial Interface Timing					
tsc	SC Cycle Time	80			ns
tsc_H	SC Pulse Width, HIGH	30			ns
tsc_L	SC Pulse Width, LOW	30			ns
tsd_{su}	Audio Data Setup Time With Respect To Rising Edge of SC	10			ns
tsd_{hd}	Audio Data Hold Time With Respect to Rising Edge of SC	15			ns
tsf_{su}	Audio SFSetup Time With Respect To Rising Edge of SC	10			ns
tsf_{hd}	Audio SF Hold Time With Respect To Rising Edge of SC	15			ns
$tsdout_{mx}$	SC falling edge to SDOUT Valid			25	ns
$tsdout_{mn}$	SC falling edge to SDOUT Valid	5			ns
Reset Signal					
$t_{\overline{rst}}$	Active low reset time		1		µs
Serial Command Port					
fsc	SCL Clock Frequency			100	kHz
tsu;sta	Start condition set up time	4.7			us
thd;sta	Start condition hold time	4.0			us
tsu;sto	Stop condition set up time	4.0			us
tLOW	SCL Low time	4.7			us
tHIGH	SCL High time	4.0			us
tr	SCL & SDA rise time			1.0	us
tf	SCL & SDA fall time			0.3	us
tsu;DAT	Data set-up time	250			ns
thd;DAT	Data hold time	0			ns
tvd;DAT	SCL LOW to data out valid			3.4	us
tBUF	Bus Free time	4.7			us

Parameter	Characteristics	Min	Typ	Max	Units
Audio DAC Characteristics					
SNR	Signal To Noise Ratio	99	102		dB
THD+N	Total Harmonic Distortion + Noise	94			dB
	Dynamic Range	102	104		dB
	Channel Separation	84	97		dB
	Full Scale Output Voltage	.96	1	1.02	Vrms
	Center Voltage	2.18	2.20	2.25	V
	Inter-channel Gain Mismatch		0.1		dB
	Analog Output Load Resistance	5			KΩ
	Analog Output Load Capacitance			100	pF

PACKAGING INFORMATION

Dimensions

	Mils				Mils		
	min	norm	max		min	norm	max
A	93	100	104	E1	291	295	299
A1	4	8	12	E2	394	406	419
b	14	16	19	e		50	
C	9	10	12	L	20	30	40
D	691	702	713				

28-Pin (SOP)