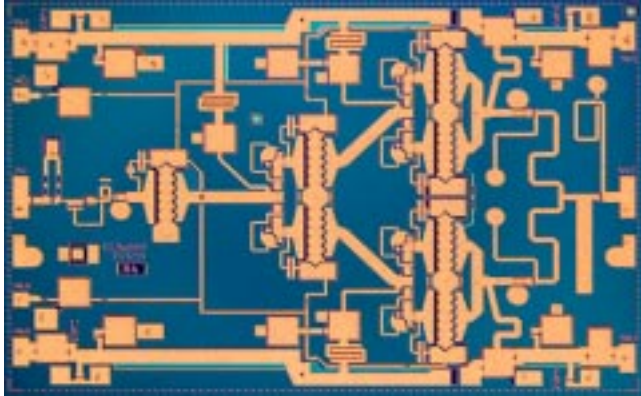


**6 - 18 GHz 2.8 Watt, 24 dB Power Amplifier**

**TGA2501**

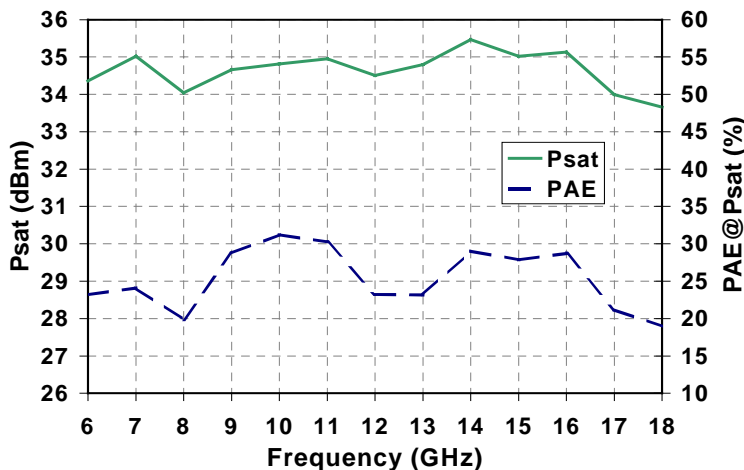
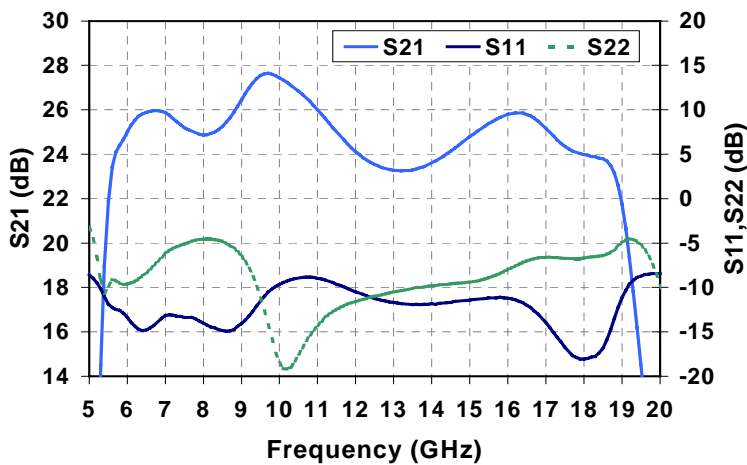


**Key Features and Performance**

- 34.5 dBm Midband Pout
- 24 dB Nominal Gain
- 10 dB Typical Input Return Loss
- 5 dB Typical Output Return Loss
- Bias Conditions: 8V @ 1.2A
- 0.25 μm Ku pHEMT 2MI
- Chip dimensions: 4.3 x 2.9 x 0.1 mm (170 x 115 x 4 mils)

**Preliminary Measured Performance**

Bias Conditions:  $V_D = 8V$   $I_D = 1.2A$

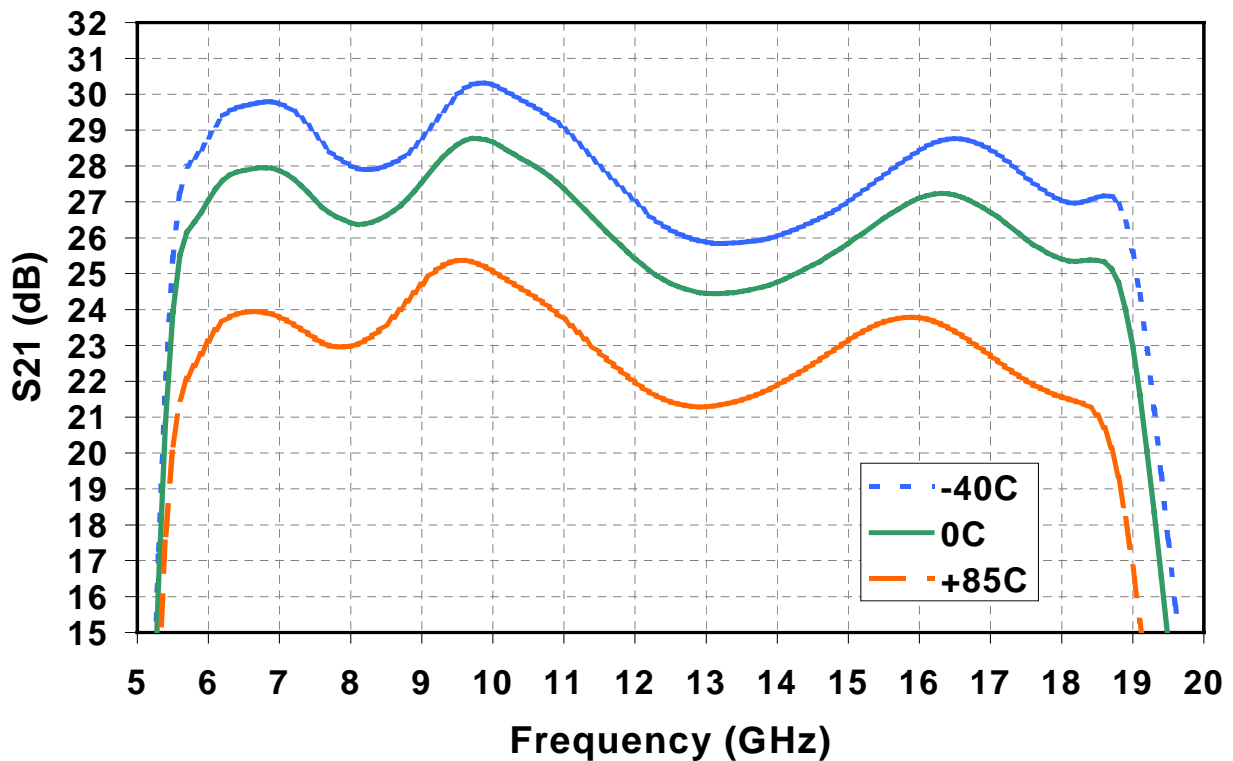
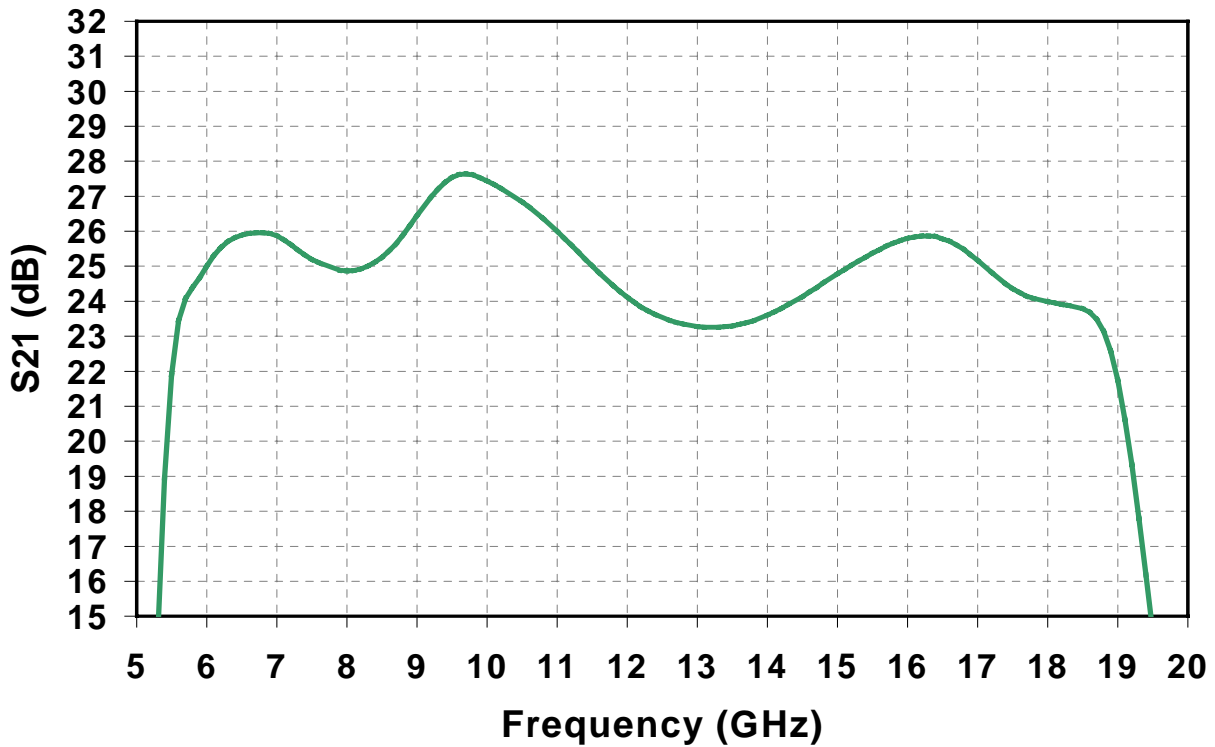


**Primary Applications**

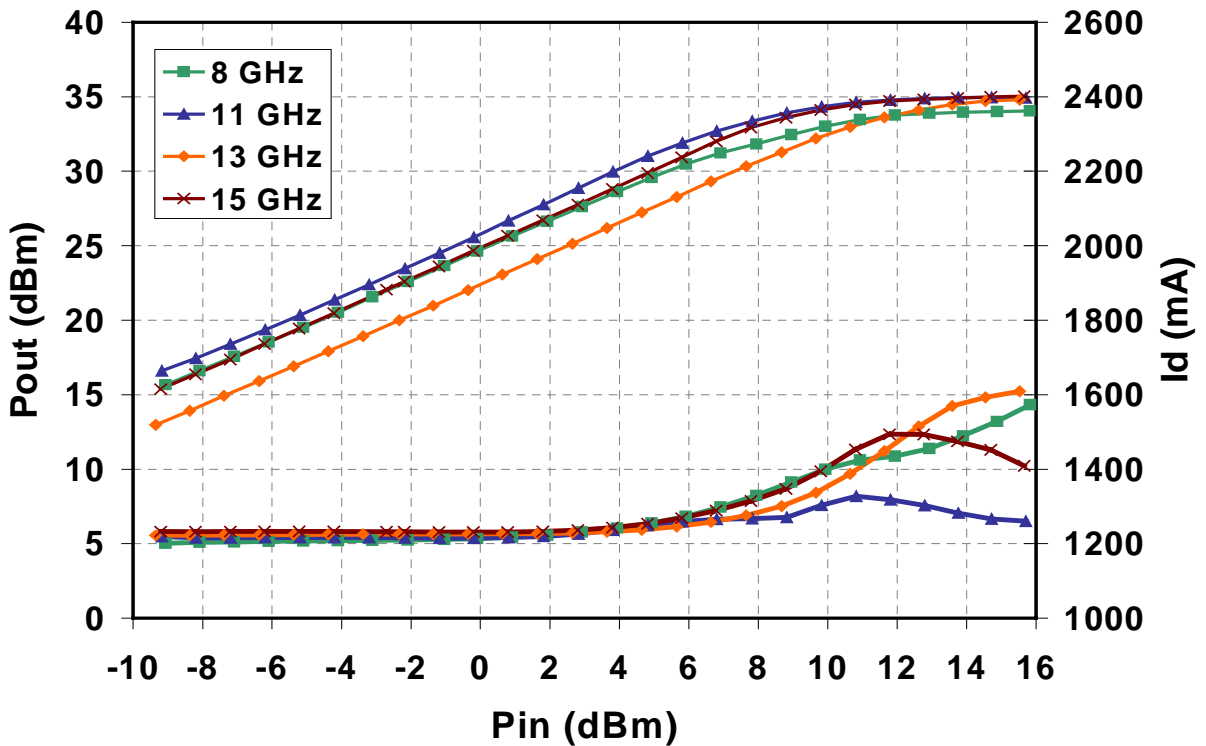
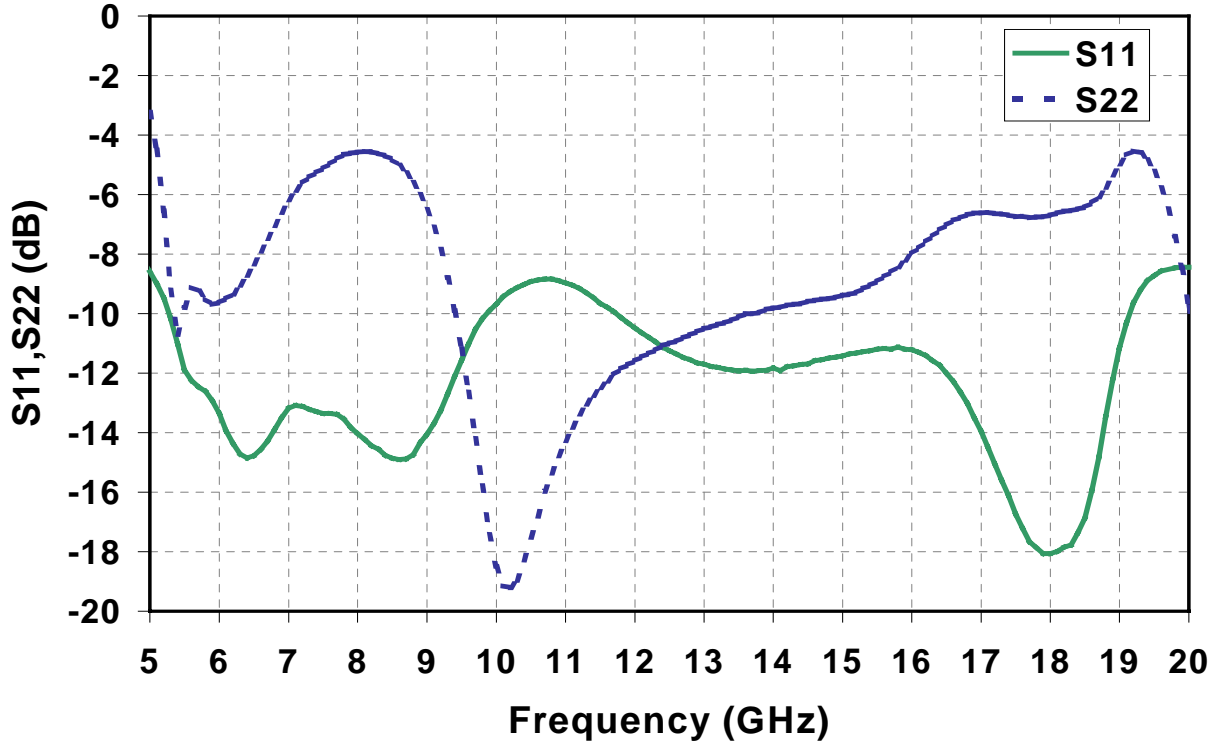
- X-Ku Point-to-Point
- ECCM

Note: This device is early in the characterization process prior to finalizing all electrical specifications. Specifications are subject to change without notice.

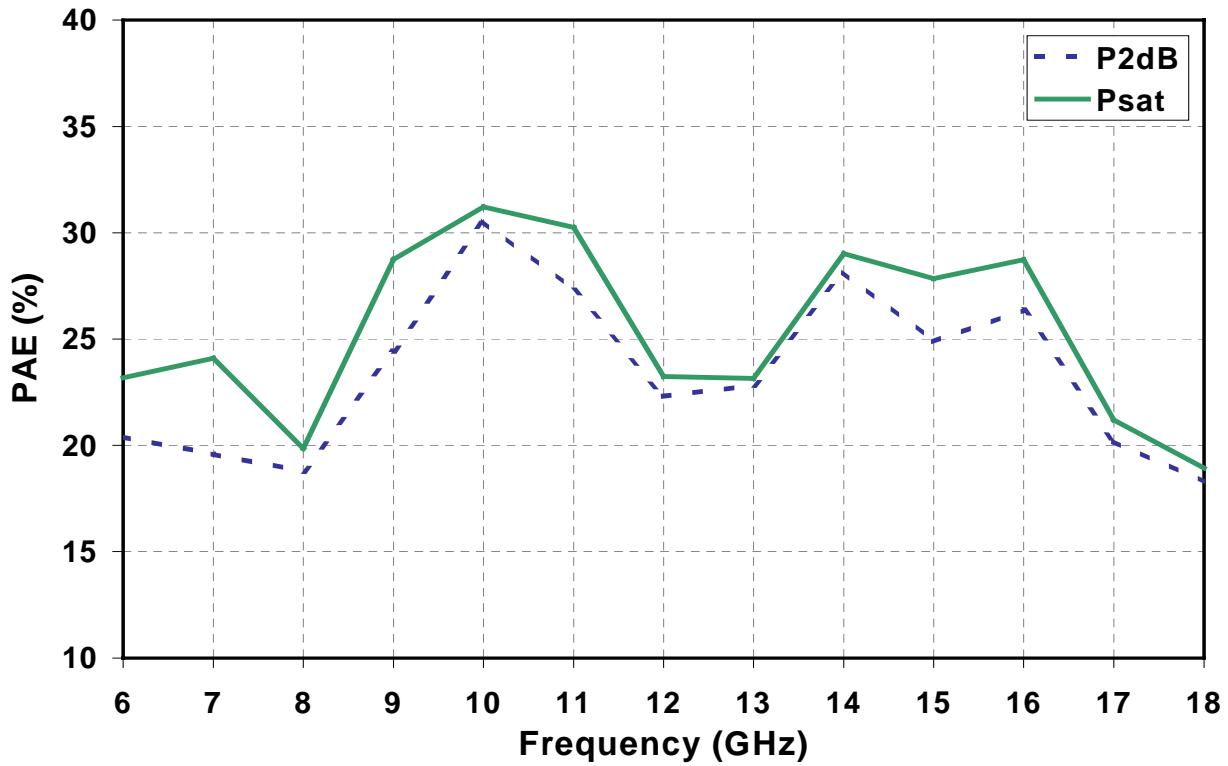
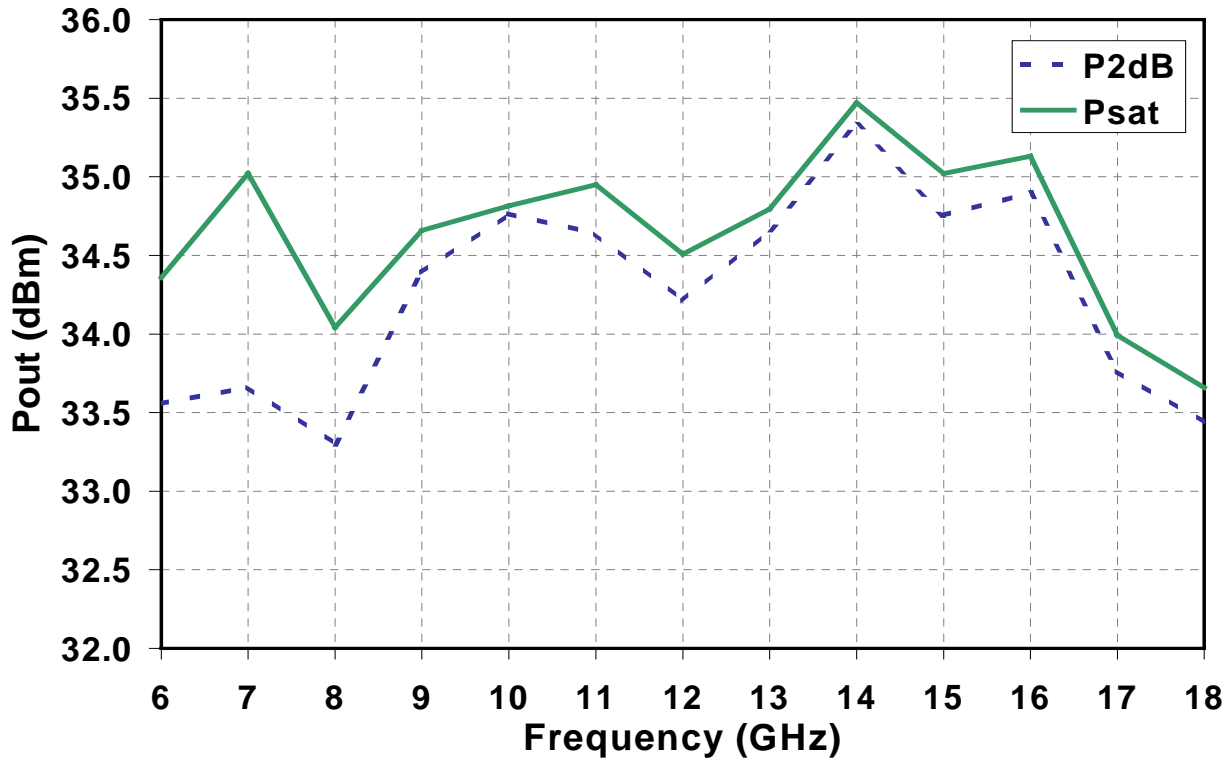
**Fixture Performance**



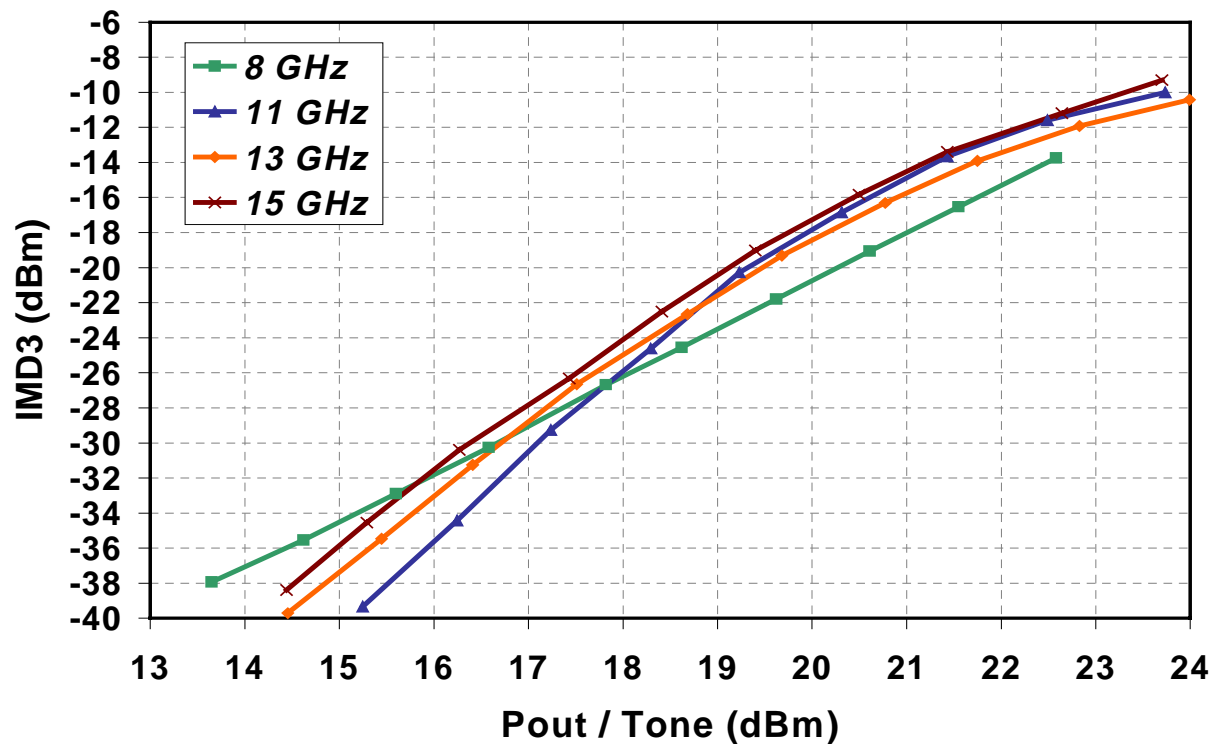
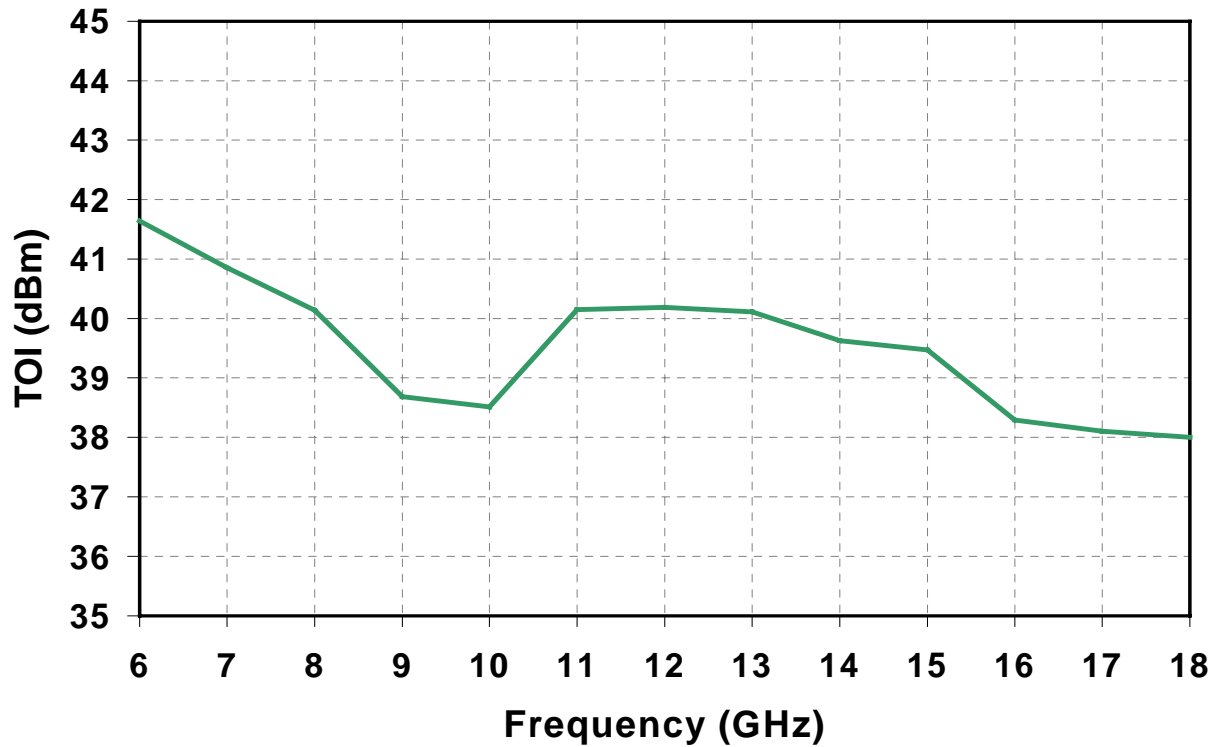
**Fixtured Performance**



**Fixture Performance**



**Fixture Performance**



**TABLE I**  
**MAXIMUM RATINGS**

Symbol	Parameter <u>5/</u>	Value	Notes
V <sup>+</sup>	Positive Supply Voltage	9 V	<u>4/</u>
V <sup>-</sup>	Negative Supply Voltage Range	-5 V to 0 V	
I <sup>+</sup>	Positive Supply Current (Quiescent)	2.0 A	<u>4/</u>
I <sub>G</sub>	Gate Supply Current	52 mA	<u>6/</u>
P <sub>IN</sub>	Input Continuous Wave Power	26 dBm	<u>4/</u>
P <sub>D</sub>	Power Dissipation	14.4 W	<u>3/ 4/</u>
T <sub>CH</sub>	Operating Channel Temperature	150 °C	<u>1/ 2/</u>
T <sub>M</sub>	Mounting Temperature (30 Seconds)	320 °C	
T <sub>STG</sub>	Storage Temperature	-65 to 150 °C	

- 1/ These ratings apply to each individual FET.
- 2/ Junction operating temperature will directly affect the device median time to failure (T<sub>M</sub>). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 3/ When operated at this bias condition with a base plate temperature of 70 °C, the median life is reduced from 1.6E+6 to 5.4E+4 hours.
- 4/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub>.
- 5/ These ratings represent the maximum operable values for this device.
- 6/ This current can be doubled by applying gate bias to both gate pads.

**TABLE II**  
**THERMAL INFORMATION**

PARAMETER	TEST CONDITION	T <sub>CH</sub> (°C)	R <sub>θjc</sub> (°C/W)	MTTF (HRS)
R <sub>θjc</sub> Thermal Resistance (Channel to Backside)	V <sub>D</sub> = 8 V I <sub>D</sub> = 1.2 A P <sub>DIS</sub> = 9.6 W	144.56	7.77	1.6E+6

Note: Assumes eutectic attach using 1.5mil 80/20 AuSn mounted to a 20mil CuMo carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

**TABLE III**  
**DC PROBE TEST**  
(TA = 25 °C, nominal)

NOTES	SYMBOL	LIMITS		UNITS
		MIN	MAX	
<u>1/</u>	$I_{DSS(Q1)}$	120	564	mA
<u>1/</u>	$G_{M(Q1)}$	264	636	mS
<u>1/</u> , <u>2/</u>	$ V_P $	0.5	1.5	V
<u>1/</u> , <u>2/</u>	$ V_{BVGs} $	13	30	V
<u>1/</u> , <u>2/</u>	$ V_{BVGD} $	13	30	V

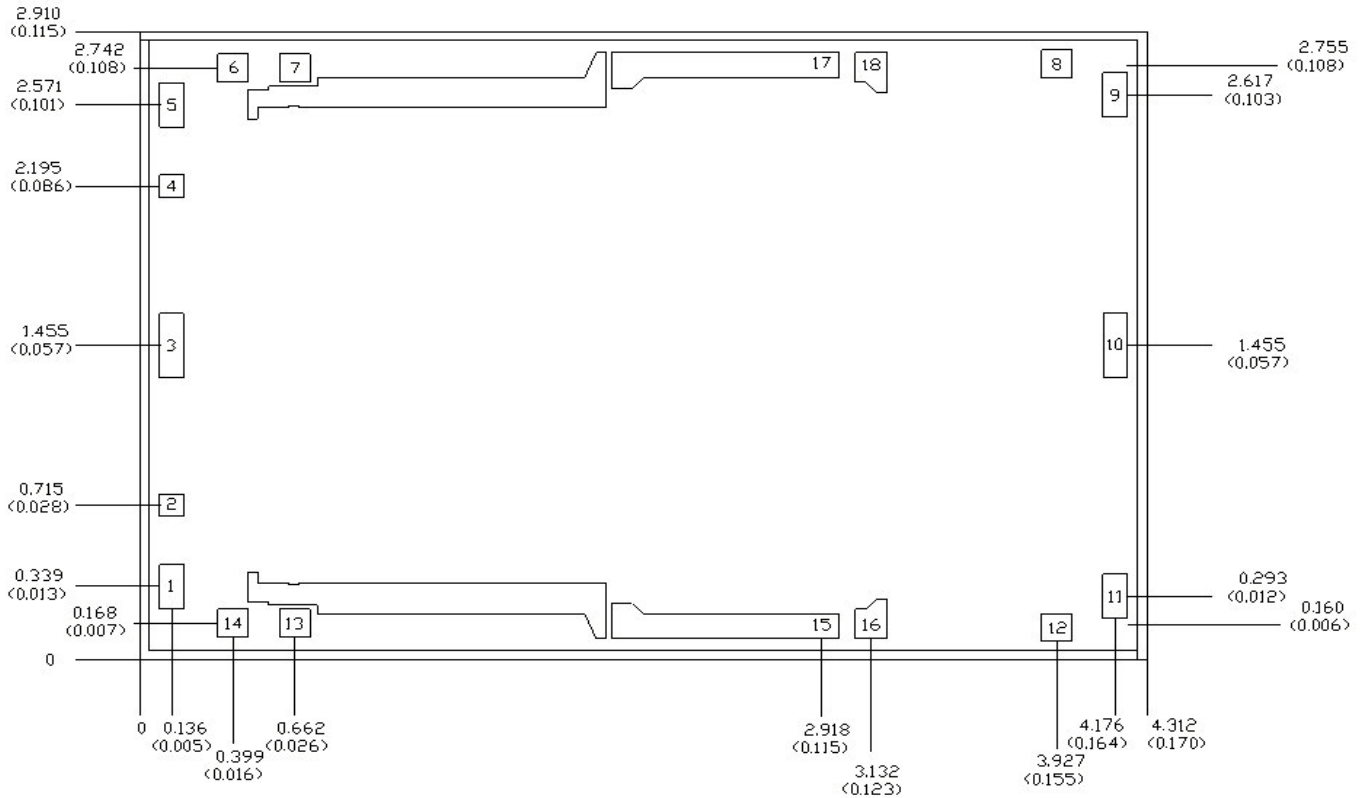
1/ Q1 is a 1200  $\mu\text{m}$  FET  
2/  $V_P$ ,  $V_{BVGD}$ , and  $V_{BVGs}$  are negative.

**TABLE IV**  
**RF CHARACTERIZATION TABLE**  
(TA = 25°C, nominal)  
(Vd = 8V, Id = 1.2A  $\pm$ 5%)

SYMBOL	PARAMETER	TEST CONDITION	TYPICAL	UNITS
Gain	Small Signal Gain	F = 6-18 GHz	24	dB
IRL	Input Return Loss	F = 6-18 GHz	10	dB
ORL	Output Return Loss	F = 6-18 GHz	5	dB
PWR	Output Power @ Pin=+15dBm	F = 6-18 GHz	34.5	dBm

Note: Table IV Lists the RF Characteristics of typical devices as determined by fixtured measurements.

**Mechanical Drawing**



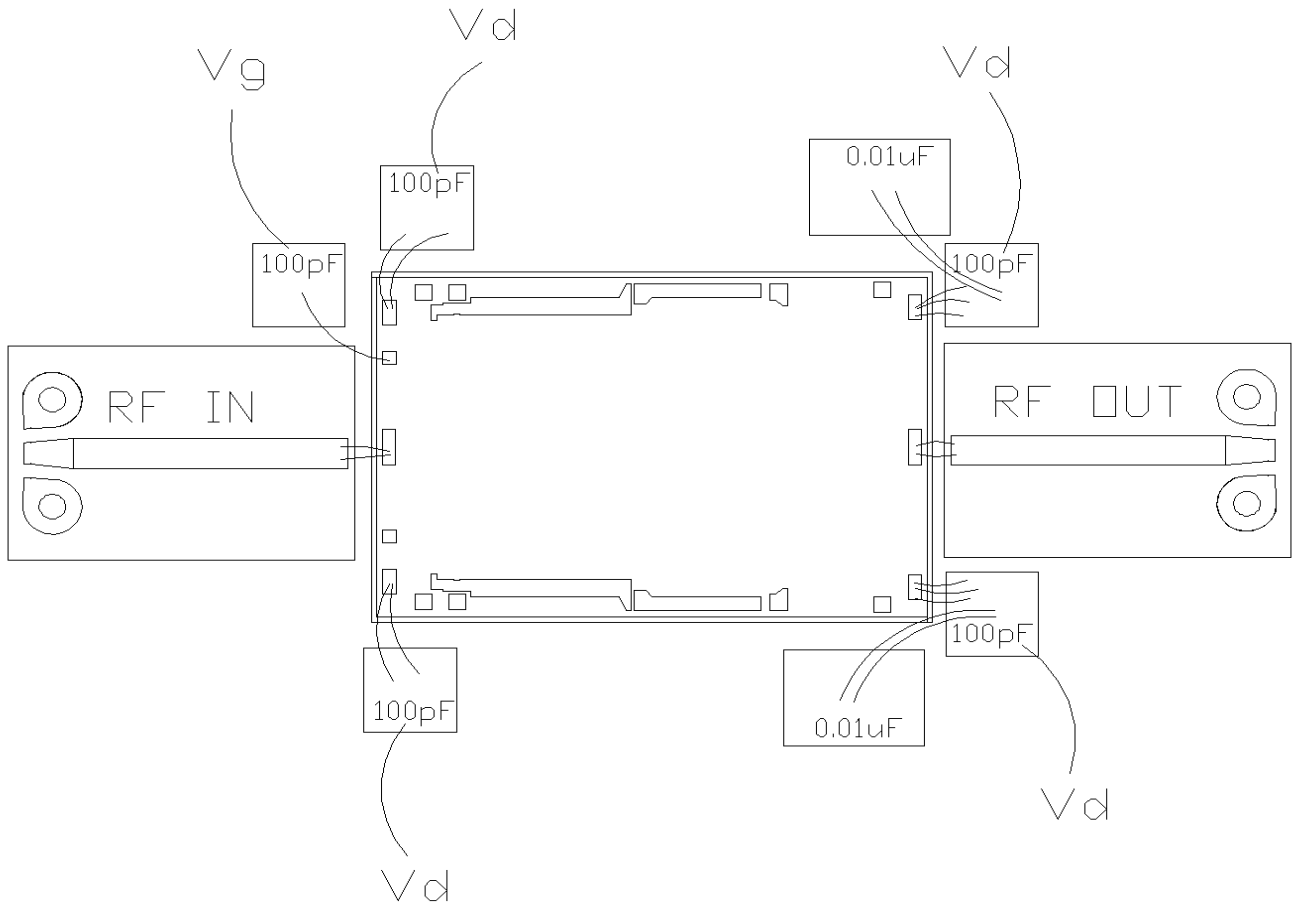
Units: millimeters (inches)  
 Thickness: 0.1016 (0.004) (reference only)  
 Chip edge to bond pad dimensions are shown to center of Bond pads.  
 Chip size tolerance: +/- 0.0508 (0.002)  
 RF Ground on backside of MMIC

Bond Pad #1,5 (Vd1&Vd2)	0.100 x 0.200	<0.004 x 0.008>
Bond Pad #9,11 (Vd3)	0.100 x 0.200	<0.004 x 0.008>
Bond Pad #2,4 (Vg)	0.100 x 0.100	<0.004 x 0.004>
Bond Pad #3 (RF Input)	0.100 x 0.300	<0.004 x 0.012>
Bond Pad #10 (RF Output)	0.100 x 0.300	<0.004 x 0.012>
Bond Pad #6,7,13,14 (DQ)	0.125 x 0.125	<0.005 x 0.005>
Bond Pad #15,16,17,18 (Vd)	0.100 x 0.100	<0.004 x 0.004>

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**



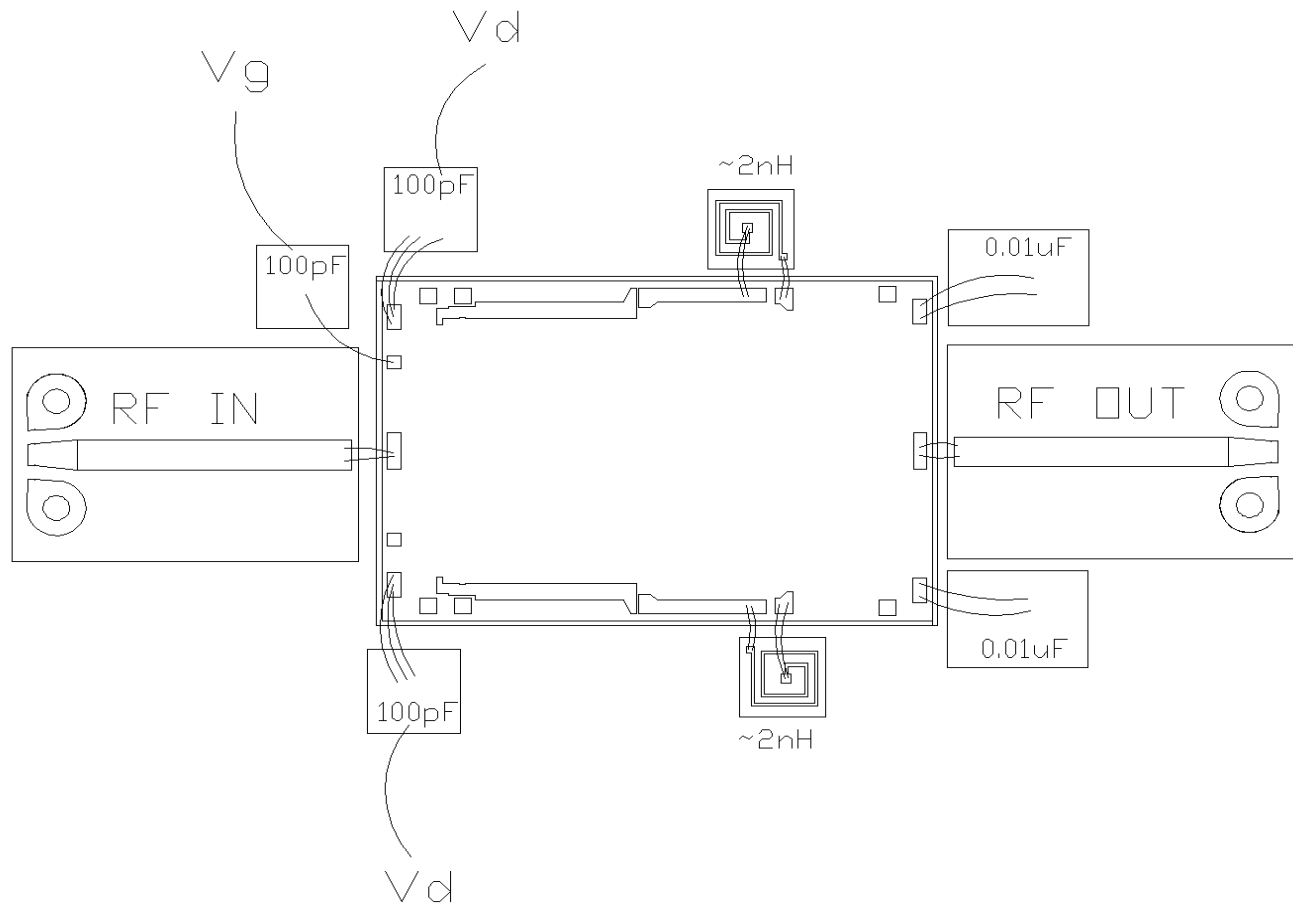
**Chip Assembly & Bonding Diagram**



1uF or larger capacitors (not shown) should be on the gate and drain line.

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***

**Alternative Chip Assembly & Bonding Diagram**



1uF or larger capacitors (not shown) should be on the gate and drain line.

*GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.*

## **Assembly Process Notes**

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C. (30 seconds maximum)
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***