ADC-574Z, -674Z
12-Bit, μP-Compatible A/D Converter with S/H

PRODUCT DATA

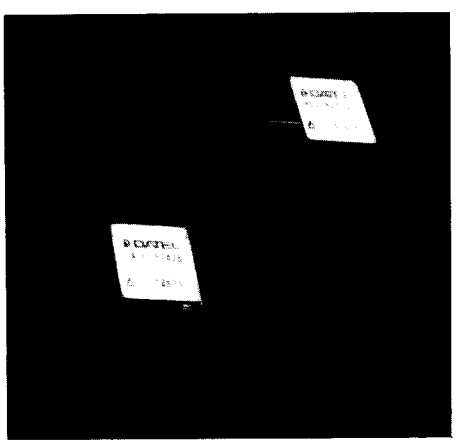
FEATURES

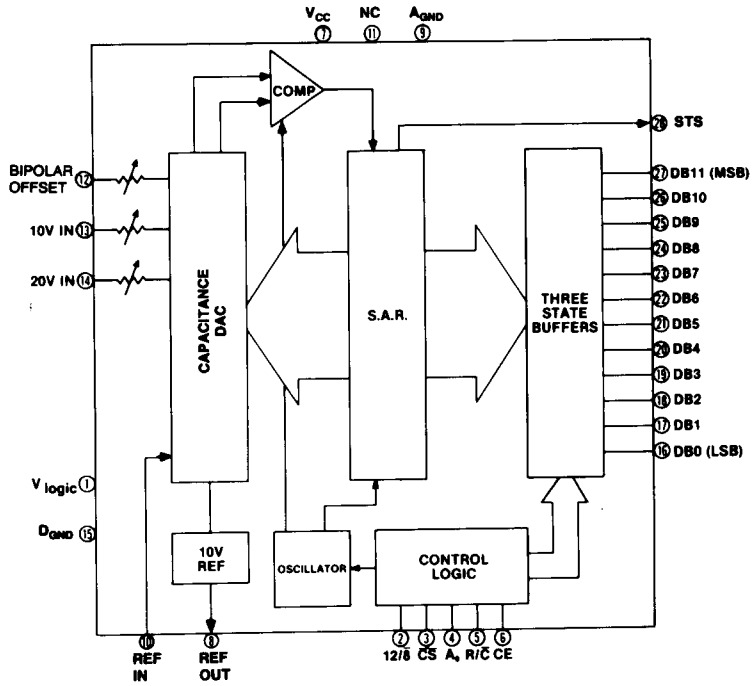
- **Complete 12-Bit A/D converters with sample-hold, reference, and clock**
- **Pin-to-pin compatible with industry standard HI574A/674A**
- **No missing codes over temperature**
- **15 μSec. Conversion time (ADC-674Z)**
- **150 mW maximum power dissipation**

GENERAL DESCRIPTION

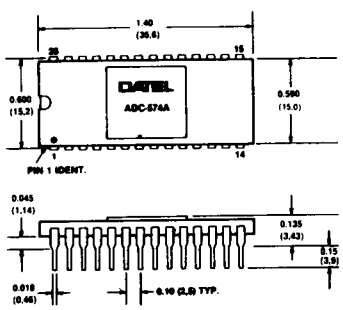
DATEL's ADC-574Z/674Z family of A/D converters are single chip monolithic CMOS versions of the industry standard devices. The sample-hold feature of this device allows conversion of input frequencies of up to 5 KHz without requiring an external circuit.

These units include a reference, clock, three-state outputs, and digital interface circuit which allows direct connection to the microprocessor address bus and control lines. The ADC-574Z completes a 12-bit conversion in microseconds, while the ADC-674Z converts in 15 microseconds. Four user selectable input ranges are provided: 0 to +10V, 0 to +20V, ±5V, and ±10V dc. Laser trimming ensures specified linearity, gain, and offset accuracy.





MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	V_{logic}, +5V	15	D_{GND}
2	12/$\overline{8}$, DATA MODE SELECT	16	DB0 (LSB)
3	$\overline{CS}$, CHIP SELECT	17	DB1
4	A_0, BYTE ADDRESS/SHORT CYCLE	18	DB2
5	R/$\overline{C}$, READ/CONVERT	19	DB3
6	CE, CHIP ENABLE	20	DB4
7	V_{CC}	21	DB5
8	REFERENCE OUT	22	DB6
9	A_{GND}	23	DB7
10	REFERENCE IN	24	DB8
11	NC	25	DB9
12	BIPOLAR OFFSET	26	DB10
13	10V IN	27	DB11 (MSB)
14	20V IN	28	STS

ABSOLUTE MAXIMUM RATINGS	
Analog Supply Voltage (V_{CC} to D_{GND})	0 to +16.5
Logic Supply Voltage (Pin 1)	0V to +7V
Analog Common (Pin 9) to Digital Common (Pin 15)	±1V
Digital Control Inputs (Pins 2–6) to Digital Common	−0.5V to V_{logic} +0.5V
Analog Inputs (Pins 10, 12, 13) to Analog Common	±16.5V
20V Input (Pin 14) to Analog Common	±24V
Ref. Out (Pin 8) Short Circuit Duration	Indefinite to common momentary to V_S
Chip Temperature	100°C
Package Dissipation	1000 mW
Lead Temperature, soldering	300°C, 10 Sec.
Thermal Resistance, Junction-to-Ambient	48°C/W

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, +15V dc (or +12V dc) and +5V dc supply voltage, unless otherwise noted.

ANALOG INPUTS	
Input Voltage Range, unipolar	0 to +10V, 0 to +20V
bipolar	±5V, ±10V
Input Impedance, 10V range	5 KΩ ±25%
20V range	10 KΩ ±25%
ANALOG OUTPUTS[1]	
Internal Reference, voltage	+10.00V ±0.1 max.
current	2.0 mA max.
DIGITAL INPUTS[2]	
Logic Levels: logic "1"	+2.4V min. to +5.5V max.
logic "0"	−0.5V min. to +0.8V max.
Loading: logic current, min.	−5 μA
max.	+5 μA
Capacitance	5 pF
DIGITAL OUTPUTS[3]	
Logic Levels: logic "0" (I sink, 1.6 mA)	+0.4V max.
logic "1" (I source, 500 μA)	+2.4V min.
Leakage (high impedance state)	−5 μA min. to +5 μA max.
Capacitance	5 pF
POWER REQUIREMENTS	
Analog Supply Voltage Range	+11.4V to +16.5V
Logic Supply Voltage Range	+4.5V to +5.5V
Supply Current max., Analog Supply	+7 mA
Logic Supply	+1 mA
Power Consumption (+V_S = +15V), max.	150 mW
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Type	28 pin side brazed ceramic DIP
SAMPLE/HOLD PERFORMANCE	
Acquisition Time 574Z	2.4 ± 0.6 μ Sec.
674Z	1.4 ± 0.4 μ Sec.
Aperture Jitter	8 n Sec.

PERFORMANCE	574ZA	674ZA	574ZB	674ZB	574ZC	674ZC
Resolution	12 Bits		12 Bits		12 Bits	
Unipolar Offset, max.[5]	±2 LSB		+2 LSB		±2 LSB	
Conversion Time, max.	25 μSec.	15 μSec.	25 μSec.	15 μSec.	25 μSec.	15 μSec.
Full Scale Calibration Error, max.[6]						
at 25°C	0.5% of F.S.		0.3% of F.S.		0.3% of F.S.	
over temp.[7]	0.5%		0.4%		0.35%	
over temp.[8]	0.22%		0.12%		0.05%	
Linearity Error, max. (over temp)	±1 LSB		±½ LSB		±½ LSB	
Differential Linearity Error[4]	±1 LSB		±½ LSB		±½ LSB	
Bipolar Offset, max.[5]	±10 LSB		±4 LSB		±4 LSB	
Tempco:[9]						
Unipolar Offset	10 ppm/°C		5 ppm/°C		5 ppm/°C	
Bipolar Offset	10 ppm/°C		5 ppm/°C		5 ppm/°C	
Full Scale Calibration	45 ppm/°C		25 ppm/°C		10 ppm/°C	
Power Supply Rejection:[10]						
+V_S = 13.5V to 16.5V or +11.4V to +12.6V	±2 LSB		±1 LSB		±1 LSB	
±V_{logic} = +4.5V to +5.5V	±½ LSB		±½ LSB		±½ LSB	

SPECIFICATION FOOTNOTES:

1. Available for external loads. External load should not change during conversion. When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the reference output.
2. Logic Inputs — CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$.
3. Logic Outputs — DB11-DBO, STS.
4. Over temperature.
5. Adjustable to zero.
6. With 50 Ω fixed resistor from REF OUT to REF IN. Adjustable to zero.
7. No adjustment at 25°C.
8. With adjustment at 25°C.
9. Guaranteed maximum change, Tmin to Tmax (using internal reference).
10. Maximum change in full scale calibration.

TECHNICAL NOTES

1. The ADC-574Z, -674Z may interface directly to a microprocessor which can take full control of each conversion, or the device can be operated in the "stand alone" mode (controlled only by the R/$\overline{C}$ input). Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion and reading the output data when ready. The data may be read 12 bits at once or 8 followed by 4 in a left-justified format. There are five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE) and all are TTL/CMOS compatible. (See Control Input Truth Table.)

2. A conversion is initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$. One, two, or all three may be dynamically controlled. The nominal delay for each of the three inputs is the same and if necessary, all three may change states simultaneously. If it is required that a particular input controls the start of conversion, the other two should be set up at least 50 nanoseconds earlier. (See Start Convert Timing.)

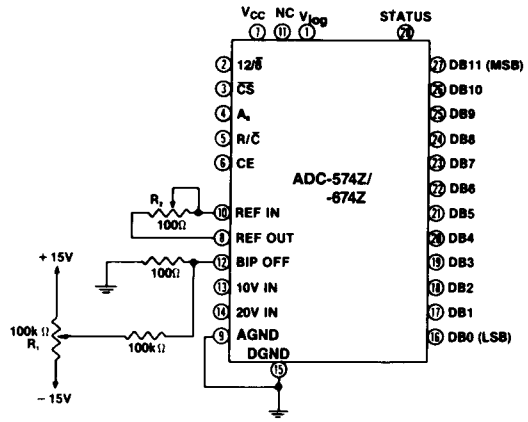
3. To read the output data, four conditions must be met (or the output buffers will remain in high impedance state): R/$\overline{C}$ taken high, STS low, CE high and $\overline{CS}$ low. When this is accomplished, the data lines are activated according to the state of the 12/$\overline{8}$ and A_0 inputs. (See START CONVERT, READ CYCLE TIMING and APPLICATION.)

4. The analog signal source driving the ADC-574Z, -674Z's input will see a nominal load of 5 KΩ (10V range) or 10 KΩ (20V range). However, the other end of these input resistors may change 400 mV with each bit decision, causing sudden changes in current at the analog input. Therefore, the signal source must maintain its output voltage while supplying these step changes in load current which occur at 1.6 microsecond intervals. This requires low output impedance and fast settling by the signal source. If a sample/hold is required to precede the converter, DATEL's SHM-20 is recommended.

5. The power supply used should be low noise and well regulated. Voltage spikes can affect accuracy. If a switching supply is used, the outputs should be carefully filtered to assure "noise free" dc voltage to the converter. Decoupling capacitors should be used on all power supply pins; the +5V dc supply decoupling capacitor should be connected directly from $+V_{logic}$ (Pin 1) to digital common (Pin 15). V_{CC} (Pin 7) should be decoupled directly to A_{GND} (Pin 9). It is recommended that a 10 μF tantalum type in parallel with a 0.1 μF ceramic type be used for decoupling.

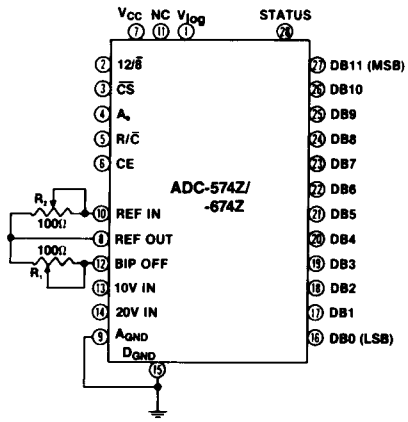
6. The use of good circuit board layout techniques is required for rated performance. It is recommended that a double sided printed circuit board with a ground plane on the component side is used. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard will have an unpredictable effect on accuracy. Sensitive analog signals should be routed between ground traces and kept away from digital lines. If analog and digital lines must cross, they should do so at right angles.

TYPICAL CONNECTIONS



UNIPOLAR CONFIGURATION

NOTES: The trimpots shown are for calibration of offset and gain. If adjustment is not required in unipolar; replace R_2 with a 50Ω, 1% metal film resistor, omit the network on Pin 12 and connect Pin 12 to Pin 9. In bipolar; either R_1, or R_2 or both can be replaced by 50Ω, 1% metal film resistors.



BIPOLAR CONFIGURATION

CODING TABLES

INPUT RANGE		OUTPUT CODING		
0 to + 10V	0 to + 20V	MSB		LSB
+10.000	+20.0000	1111	1111	1111
+9.9963	+19.9927	1111	1111	111Ø*
+5.0012	+10.0024	1000	0000	000Ø*
+4.9988	+9.9976	Ø000	0000	000Ø*
+4.9963	+9.9927	0111	1111	111Ø*
+0.0012	+0.0024	0000	0000	000Ø*
0.0000	+0.0000	0000	0000	0000

INPUT RANGE		OUTPUT CODING		
±5V	±10V	MSB		LSB
+5.0000	+10.0000	1111	1111	1111
+4.9963	+9.9927	1111	1111	111Ø*
+0.0012	+0.0024	1000	0000	000Ø*
-0.0012	-0.0024	Ø000	0000	000Ø*
-0.0037	-0.0073	0111	1111	111Ø*
-4.9988	-9.9976	0000	0000	000Ø*
-5.0000	-10.0000	0000	0000	0000

*Voltages shown are theoretical values for the transitions indicated. Ideally, in the continuous conversion mode, the output bits indicated as Ø will change from "1" to "0" or "0" to "1" as the input voltage passes through the level indicated.

Output coding is straight binary for unipolar and offset binary for bipolar.

CALIBRATION

UNIPOLAR CALIBRATION

Offset Adjust

Apply an input of + ½ LSB (+1.22 mV for the 10V range; +2.44 mV for the 20V range). Adjust the offset trimpot (R_1) until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Gain Adjust

Apply 1½ LSB's below the nominal full-scale (+9.9963V for the l0V range; +19.9927V for the 20V range). Adjust the gain trimpot (R_2) so that the output flickers between 1111 1111 1110 and 1111 1111 1111.

BIPOLAR CALIBRATION

Offset Adjust

Apply ½ LSB above negative full-scale (−4.9988V for the ±5V range; −9.9976V for the ±10V range.) Adjust the offset trimpot (R_1) so that the output flickers between 0000 0000 0000 and 0000 0000 0001.

Gain Adjust

Apply 1½ LSB's below positive full scale (+4.9963V for the ±5V range; +9.9927V for the ±10V range). Adjust the gain trimpot (R_2) so that the output flickers between 1111 1111 1110 and 1111 1111 1111.

TIMING CONTROL

The variety of the ADC-574Z, -674Z's control modes (as shown in the "CONTROL INPUTS TRUTH TABLE") allow for simple interface in most system applications.

The output signal STS indicates the status of the device; high during a conversion, and low at the completion of a conversion. During a conversion (STS output high), the output buffers remain in the high impedance state and data cannot be read. A start convert during conversion will not reset the converter or reinitiate a conversion. However, if A_0, changes state after a conversion begins, an additional start convert pulse will latch the new state of A_0, causing a wrong cycle length for that conversion.

Control Inputs Truth Table

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
0-1	0	0	X	0	Initiate 12-bit conversion
0-1	0	0	X	1	Initiate 8-bit conversion
1	1-0	0	X	0	Initiate 12-bit conversion
1	1-0	0	X	1	Initiate 8-bit conversion
1	0	1-0	X	0	Initiate 12-bit conversion
1	0	1-0	X	1	Initiate 8-bit conversion
1	0	1	1	X	Initiate 12-bit conversion
1	0	1	0	0	Enable's 8 MSB's only
1	0	1	0	1	Enable's 4 LSB's plus 4 trailing zeroes

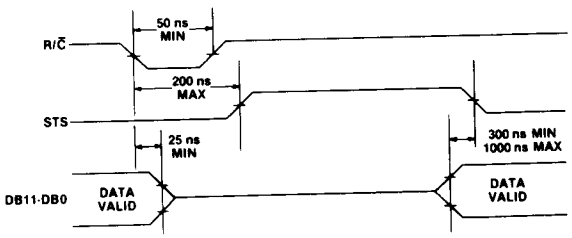
TIMING AND OPERATION

Stand-Alone Mode Timing

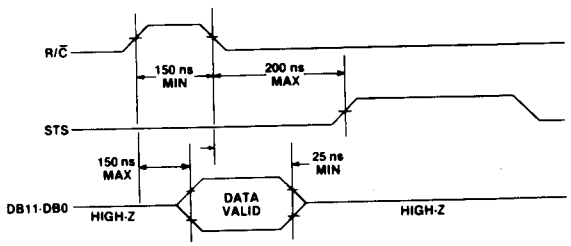
For stand-alone operation, all that is required is a single control line to R/$\overline{C}$. CE and 12/$\overline{8}$ are tied high, $\overline{CS}$ and A_0 are tied low, and the output appears in words of 12 bits.

The R/$\overline{C}$ signal may have any duty cycle within the limits shown in the diagrams below.

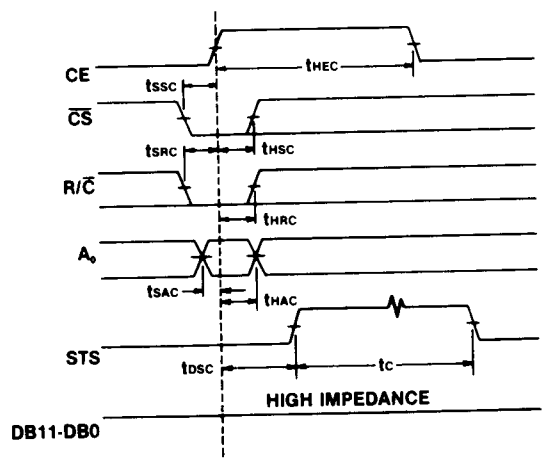
The data may be read when R/$\overline{C}$ is high unless STS is also high indicating a conversion is in progress.



Outputs Enabled After Conversion

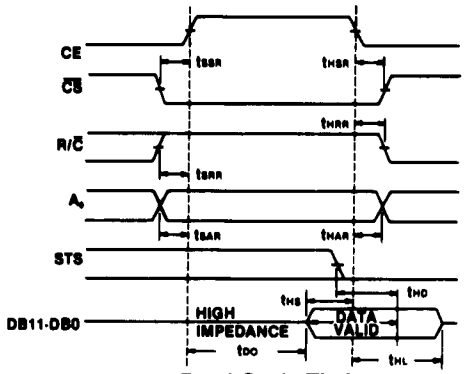


Outputs Enabled With R/$\overline{C}$ High



Start Convert Timing

A read operation in most applications begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. (See Technical Note 3.)



Read Cycle Timing

Read Mode

Symbol	Parameter	Min.	Typ.	Max.
t_{DD}	Access Time from CE	—	75 nS	150 nS
t_{HD}	Data Valid after CE low	25 nS	35 nS	—
t_{HL}	Output Float Delay	—	100 nS	150 nS
t_{SSR}	$\overline{CS}$ to CE Setup	50 nS	0	—
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0	—
t_{SAR}	A_0 to CE Setup	50 nS	25 nS	—
t_{HSR}	$\overline{CS}$ Valid after CE Low	0	0	0
t_{HRR}	R/$\overline{C}$ High after CE Low	0	0	0
t_{HAR}	A_0 Valid after CE Low	50 nS	25 nS	—
t_{HS}	STS Delay after Data Valid			
	-574Z	300 nS	—	1000 nS
	-674Z	100 mS	—	600 mS

ADC-574Z, 674Z Convert Mode Timing

Symbol	Parameter	Min.	Typ.	Max.
t_{DSC}	STS Delay From CE	—	100 nS	200 nS
t_{HEC}	CE Pulse Width	50 nS	30 nS	—
t_{SSC}	$\overline{CS}$ to CE Setup	50 nS	20 nS	—
t_{HSC}	$\overline{CS}$ Low during CE High	50 nS	20 nS	—
t_{SRC}	R/$\overline{C}$ to CE Setup	50 nS	0	—
t_{HRC}	R/$\overline{C}$ Low during CE High	50 nS	20 nS	—
t_{SAC}	A_0 to CE Setup	0	0	0
t_{HAC}	A_0 Valid during CD High	50 nS	20 nS	—
t_C	Conversion Time, -574Z			
	12-bit cycle	15 μS	18 μS	25 μS
	8-bit cycle	10 μS	13 μS	17 μS
	Conversion Time, -674Z			
	12-bit cycle	9 μS	—	15 μS
	8-bit cycle	6 μS	—	10 μS

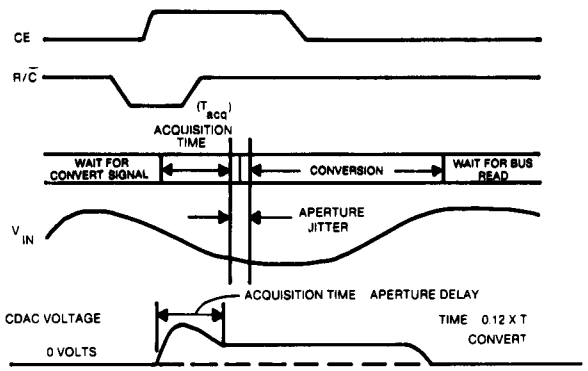
Built-in Sample/Hold

Both the ADC-574Z and the ADC-674Z contain internal sample-and-hold (S/H) capable of sampling inputs up to 5 KHz.

The R/$\overline{C}$ line controls the internal S/H. The 574Z/674Z sampling and conversion sequence begins when the R/$\overline{C}$ line makes a negative transition.

After the first two clock cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

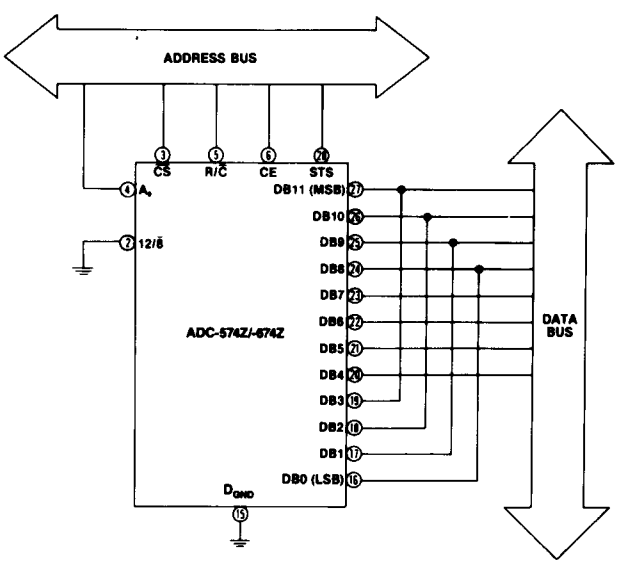
Since the sample is taken relative to the R/$\overline{C}$ transition, Tacq is also the "aperture delay" of the S/H. The duration of Tacq is measured in clock cycles and is specified as 2.4 μS ± 0.6 μS for the 574Z and 1.4 μS ± 0.4 μS for the 674Z. The "aperture jitter" nominally allows converting signals of up to 5 KHz without an external sample-hold. Above 5 KHz, the internal S/H will be transparent.



Sample and Hold Function

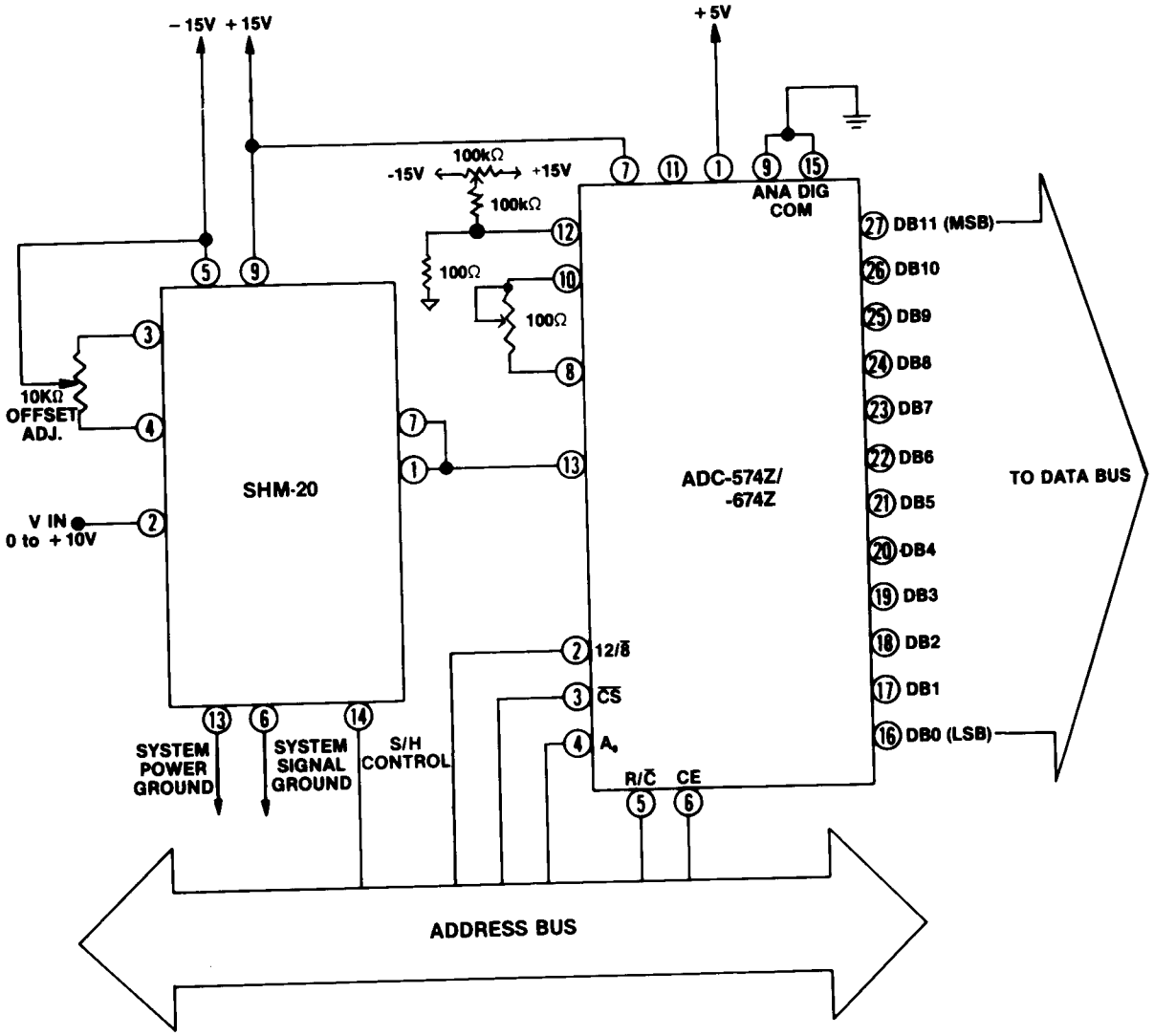
Interface To An 8-Bit Data Bus

The 12/$\overline{8}$ input will be tied either high or low in most applications. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously for interface to a 12- or 16-bit data bus. A_0 is ignored. Taking 12/$\overline{8}$ low organizes the output in two 8-bit bytes, which are selected one at a time by A_0. This allows an 8-bit data bus to be connected as shown above. A_0 is normally tied to the LSB of the address bus for storing the converter's output in two consecutive memory locations. This two byte format is called "left justified data" for which a decimal point is assumed to the left of byte 1. In addition, A_0 may be toggled at any time without damage to the converter. Break-before-make switching is guaranteed between two data bytes, which assures that the outputs strapped together as shown are never enabled at the same time.



DATEL

FAST A/D WITH SAMPLE HOLD



The above diagram shows the ADC-574Z, -674Z configured for unipolar (0 to + 10V) operation. Preceding the ADC-574Z, -674Z is DATEL's SHM-20, a 1 microsecond precision sample/hold. All sample/hold amplifiers are compatible with the ADC-574Z, -674Z; however, many will require an additional wide-band buffer amplifier to reduce their output impedance.

ORDERING INFORMATION

MODEL NO.	TEMPCO
ADC-574ZC	45 ppm/°C
ADC-574ZB	25 ppm/°C
ADC-574ZA	10 ppm/°C
ADC-674ZC	45 ppm/°C
ADC-674ZB	25 ppm/°C
ADC-674ZA	10 ppm/°C

ACCESSORIES Part Number	Description
TP100 or TP100K	Trimming Potentiometers

DS-0036B

DATEL

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