

# DATA SHEET

## **TDA1575T** FM front end circuit for CENELEC EN 55020 applications

Preliminary specification  
Supersedes data of October 1990  
File under Integrated Circuits, IC01

April 1993

## FM front end circuit for CENELEC EN 55020 applications

## TDA1575T

### FEATURES

- Bipolar integrated FM front end circuit, designed for use in car radios and home receivers
- Fulfils CENELEC EN 55020 requirements
- Radio frequency range of 76 to 90 MHz (Japan) or 87.5 to 108 MHz (Europe, USA)
- Low noise oscillator, buffered oscillator output
- Double balanced mixer
- Internal buffered mixer driving
- Linear IF amplifier, suitable for ceramic IF filters
- Regulated reference voltage.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_P$	supply voltage	7	8.5	10	V
$I_P$	supply current, without mixer	–	23	–	mA
$V_{REF}$	reference voltage output	–	4.2	–	V
$Z_I$	mixer input impedance	–	14	–	$\Omega$
NF	noise figure of mixer	–	9	–	dB
EMF1	3rd order intermodulation	–	115	–	$\text{dB}\mu\text{V}$
$V_{OSC}$	oscillator buffer output signal (RMS value)	75	–	–	mV
THD	total harmonic distortion	–	–15	–	dB
$G_v$	IF gain	–	30	–	dB
NF	IF noise figure	–	6.5	–	dB
$Z_I$	IF input impedance	–	300	–	$\Omega$
$Z_O$	IF output impedance	–	300	–	$\Omega$
EMF2	AGC wideband threshold (RMS value)	–	17	–	mV

### ORDERING INFORMATION

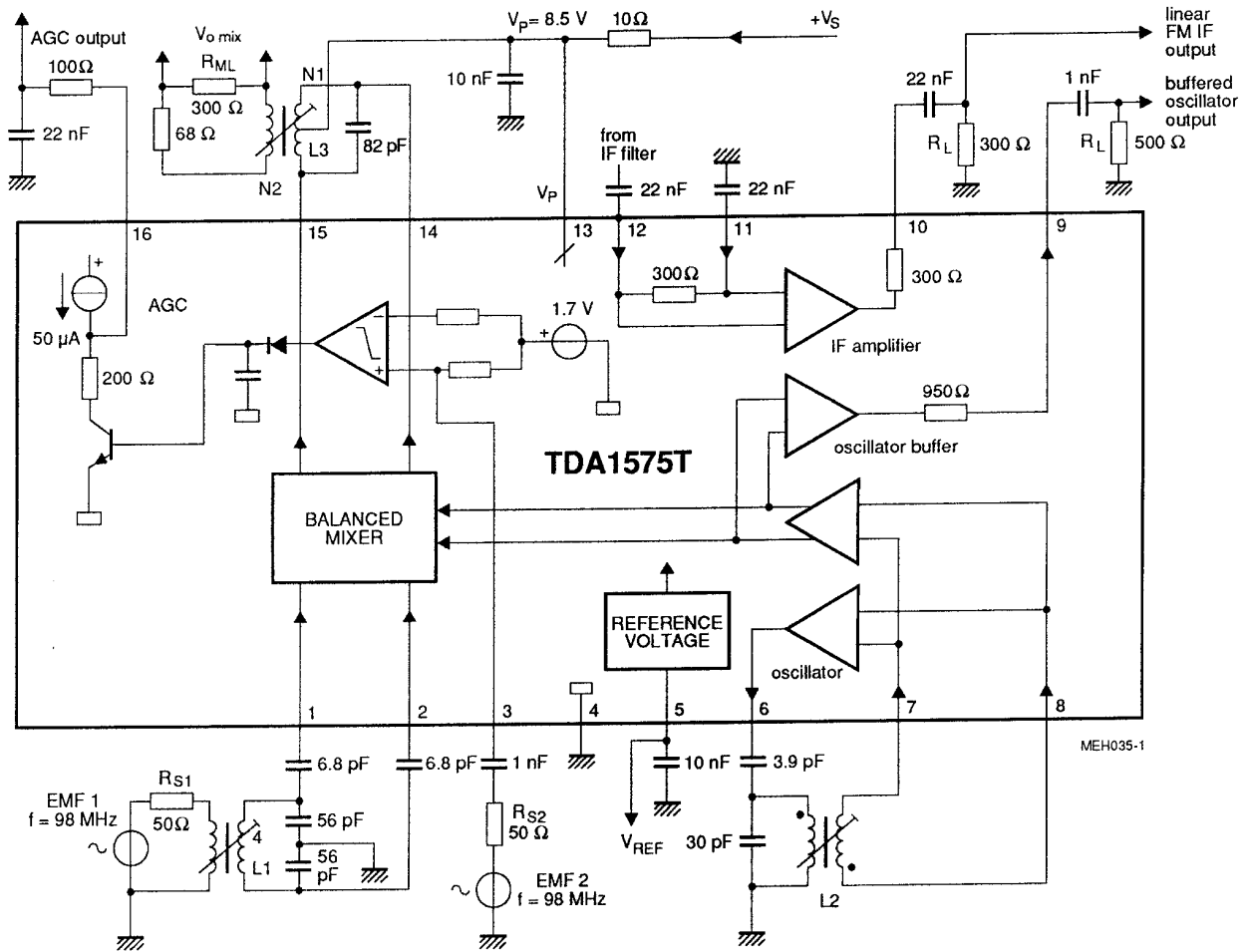
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1575T	16	mini-pack	plastic	SOT109A <sup>(1)</sup>

#### Note

1. SOT109-1; 1996 August 29.

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Coils TOKO

L1: MC-108 514 HNE-150023S14; L = 78 nH, N = 4 turns

L2: MC-111 E516 HNS-200057; L = 80 nH

L3: A119 ACS-17114 FTT

Fig.1 Block diagram and test circuit.

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**PINNING**

SYMBOL	PIN	DESCRIPTION
MIXI1	1	RF input 1 to mixer
MIXI2	2	RF input 2 to mixer
AGCI	3	HF input to automatic gain control
GND	4	ground (0 V)
V <sub>REF</sub>	5	reference voltage output
OSCO	6	oscillator output
OSCI1	7	oscillator input 1
OSCI2	8	oscillator input 2
LO	9	buffered oscillator output
IFO	10	linear FM IF output
IFI1	11	FM IF input 1
IFI2	12	FM IF input 2
V <sub>P</sub>	13	supply voltage (+8.5 V)
MIXO1	14	mixer output 1
MIXO2	15	mixer output 2
AGCO	16	automatic gain control output

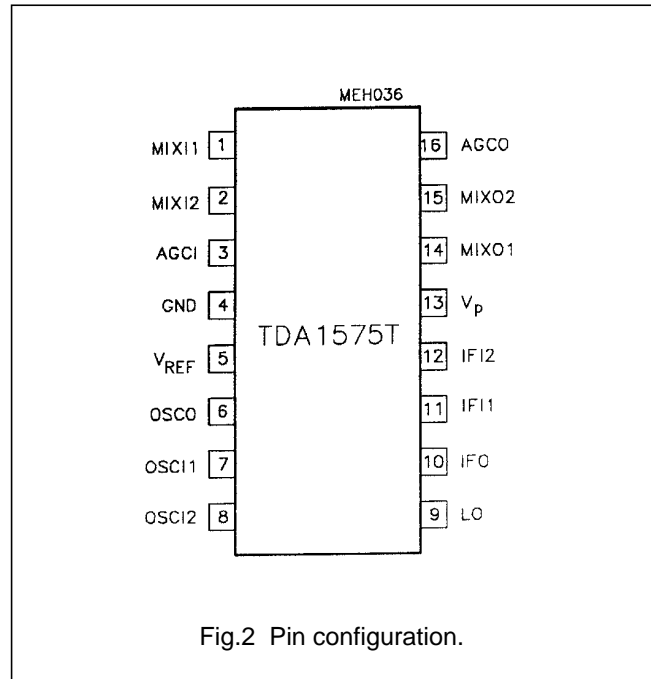


Fig.2 Pin configuration.

**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>P</sub>	supply voltage (pin 13)	0	12	V
V <sub>14, 15</sub>	voltage at mixer output	0	V <sub>P</sub>	V
P <sub>tot</sub>	total power dissipation	0	380	mW
T <sub>stg</sub>	storage temperature range	-55	+150	°C
T <sub>amb</sub>	operating ambient temperature range	-40	+85	°C
V <sub>ESD</sub>	electrostatic handling (see note 1)			
	all pins except 3 and 10	-	±2000	V
	pin 3	-	+2000	V
		-	-1000	V
	pin 10	-	+1500	V
		-	-2000	V

**Note to the limiting values**

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

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**CHARACTERISTICS**

$V_P = 8.5$  V and  $T_{amb} = +25^\circ\text{C}$ , measurements taken in Fig.1 with  $f_0 = 98$  MHz (EMF1) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P$	supply voltage (pin 13)		7	8.5	10	V
$I_P$	supply current	without mixer	16	23	30	mA
$V_{REF}$	reference voltage (pin 5)	$I_5 \leq 3$ mA	3.9	4.2	4.4	V
<b>Mixer</b>						
$I_{14+15}$	mixer supply current (pins 14 and 15)		–	4	–	mA
$V_{1,2}$	DC voltage input (pins 1 and 2)		–	1	–	V
$Z_{1,2}$	input impedance		–	14	–	$\Omega$
$V_{14,15}$	DC output voltage (pins 14 and 15)		4	–	10	V
$C_{14,15}$	output capacitance		–	13	–	pF
$G_P$	conversion power gain	note 1	–	14	–	dB
EMF1 <sub>IP3</sub>	3rd order intercept point		–	115	–	dB $\mu$ V
NF	noise figure		–	9	–	dB
	total noise figure	including transforming network	–	11	–	dB
<b>Oscillator</b>						
$V_{7,8}$	DC input voltage (pins 7 and 8)		–	1.3	–	V
$V_6$	DC output voltage (pin 6)		–	2.0	–	V
$\Delta f$	residual FM at pin 6	$f = 300$ to $15000$ Hz; de-emphasis $50 \mu\text{s}$	–	2.2	–	Hz
<b>Oscillator buffered output (pin 9)</b>						
$V_O$	output signal (RMS value)	$R_L = 500 \Omega$ ; $C_L = 2$ pF	75	–	–	mV
$V_9$	DC output voltage		–	6	–	V
$R_9$	DC output resistor		–	950	–	$\Omega$
THD	total harmonic distortion		–	–15	–	dBc
$f_S$	spurious frequencies	EMF1 = 2 V; $R_S = 50 \Omega$ ; $f_{OSC} = 108.7$ MHz	–	–37	–	dBc
<b>Automatic gain control (AGC)</b>						
$R_3$	input resistance (pin 3)		–	4	–	k $\Omega$
$C_3$	input capacitance		–	3	–	pF
$V_{16}$	AGC output swing (DC)	Figs 3 and 4	0.5	–	$V_P - 0.3$	V
$I_{16}$	output current at $I_3 = 0$	$V_{16} = \frac{1}{2}V_P$	–25	–50	–150	$\mu$ A
	output current at $U_3 = 2$ V	$V_{16} = 7$ to $10$ V	2	–	5	mA
EMF2	threshold (RMS value)	$I_{16} = 0$ ; $V_{16} = \frac{1}{2}V_P$ ; Figs 4 and 5	–	17	–	mV

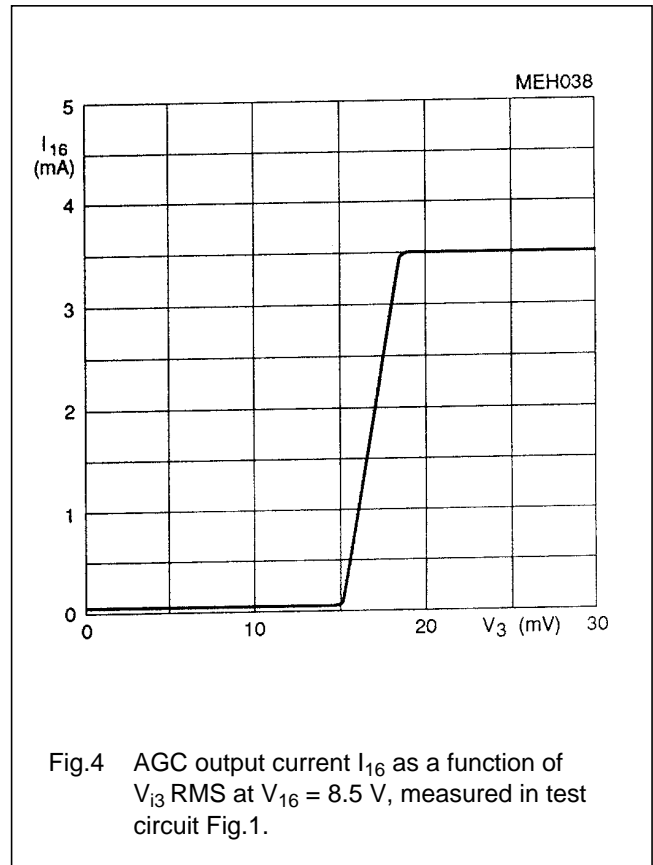
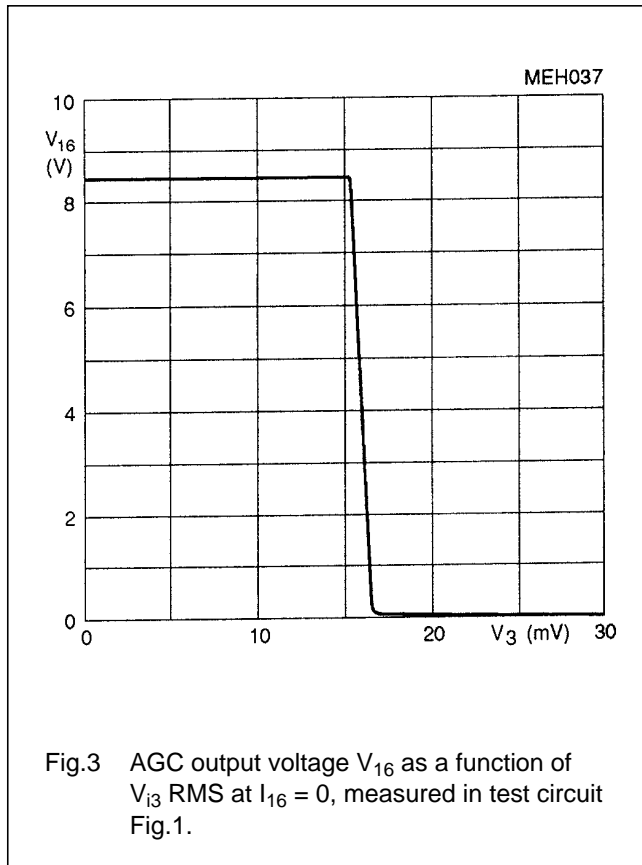
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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Linear IF amplifier</b>		IF = 10.7 MHz				
V <sub>11,12</sub>	DC input voltage (pins 11 and 12)		–	1.25	–	V
Z <sub>12-11</sub>	input impedance		240	300	360	Ω
C <sub>12-11</sub>	input capacitance		–	13	–	pF
V <sub>10</sub>	DC output voltage (pin 10)		–	4.4	–	V
Z <sub>10</sub>	output impedance		240	300	360	Ω
C <sub>10</sub>	output capacitance		–	3	–	pF
V <sub>O</sub>	output signal (RMS value)	–1 dB compression	–	–	650	mV
G <sub>V</sub>	IF voltage gain (20 log (V <sub>10-4</sub> / V <sub>12-11</sub> ))		27	30	–	dB
ΔG <sub>V</sub>	IF voltage gain deviation	T <sub>amb</sub> = –40 to +85 °C	–	0	–	dB
NF	noise figure	R <sub>S</sub> = 300 Ω	–	6.5	–	dB

**Note**

1.  $G_p = 10 \log (4V_{o\text{ mix}} \times 10.7 \text{ MHz}) / (\text{EMF2} \times 98 \text{ MHz})^2 \times (R_{S1} / R_{ML})$ .



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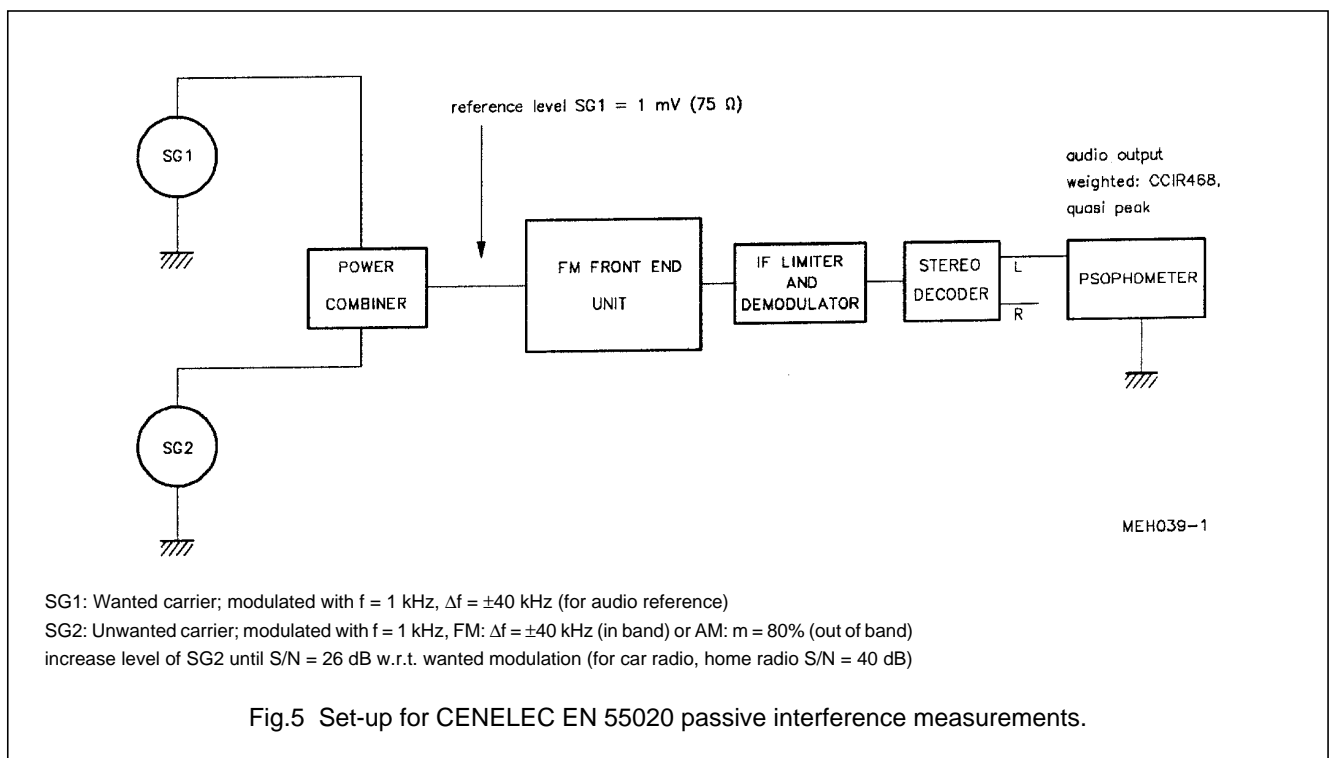
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## APPLICATION INFORMATION

### Operating characteristics

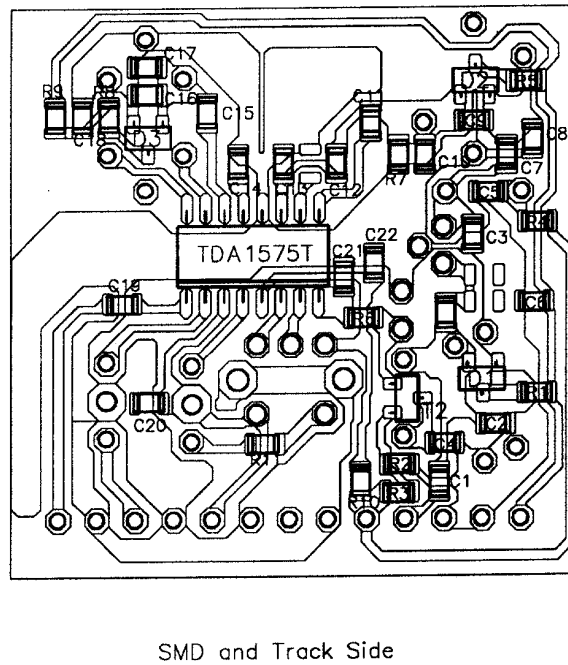
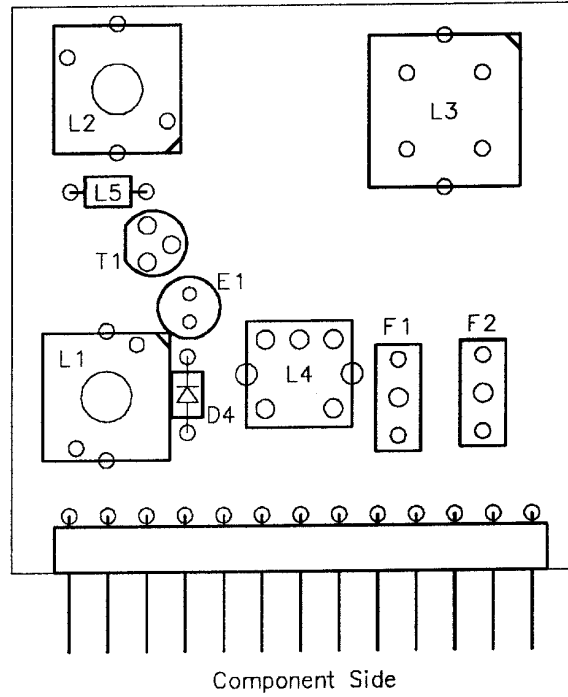
Measured in application circuit Fig.7, according to "CENELEC EN 55020, Chapter 4.1 (passive interference suppression)". Measurements are shown in Figs. 8 and 9.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>S</sub>	supply voltage		7	8.5	10	V
I <sub>S</sub>	total supply current		–	37	–	mA
f <sub>RF</sub>	tuning range of RF input		87.5	–	108	MHz
V <sub>tune</sub>	tuning voltage of RF input		1	–	7	V
G	gain (20 log V <sub>O IF</sub> / V <sub>ant</sub> )		–	43	–	dB
V <sub>i ant</sub>	input sensitivity	S/N = 26 dB; R <sub>ant</sub> = 150 Ω	–	2	–	μV
IR	image rejection	f = 98 MHz	–	64	–	dB
RSS	repeat spot suppression	f = 98 MHz; V <sub>i ant</sub> = 10 μV	–	89	–	dB
DBS	double beat suppression	f1 = 93 MHz; f2 = 98 MHz				
	DBS1	f <sub>tune</sub> = 88 MHz	–	81	–	dB
	DBS2	f <sub>tune</sub> = 103 MHz	–	80	–	dB
	DBS3	f <sub>tune</sub> = 90.15 MHz	–	85	–	dB
CBS	continuous beat suppression	f1 = 90 MHz; f2 = 100.7 MHz f <sub>tune</sub> = 95 MHz	–	90	–	dB



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MEH040

Fig.6 PCB layout of FM front end unit.





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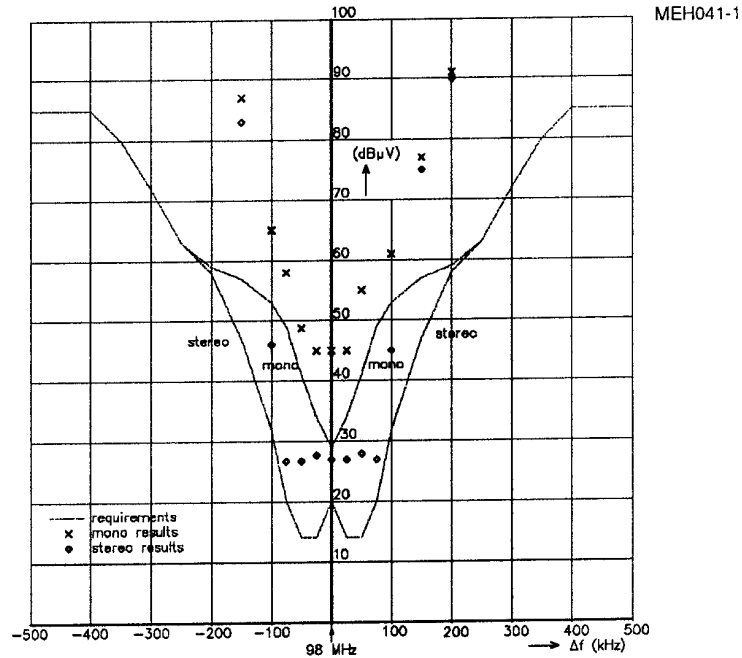


Fig.8 Interference level as a function of detuning for S/N = 26 dB;  
IN-BAND passive interference (CENELEC EN 55020).

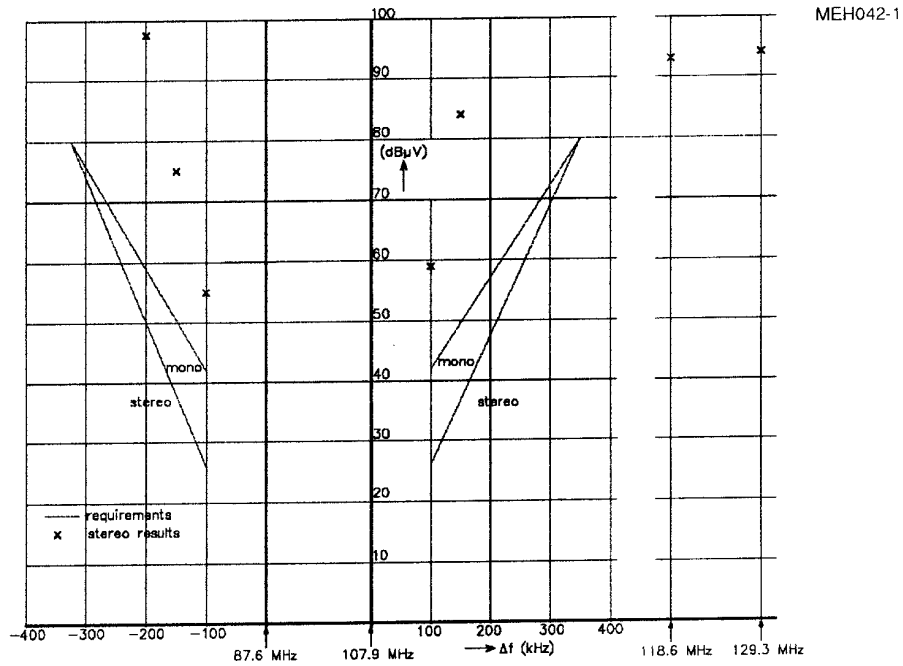


Fig.9 Interference level as a function of detuning for S/N = 26 dB;  
OUT-OF-BAND passive interference (CENELEC EN 55020).

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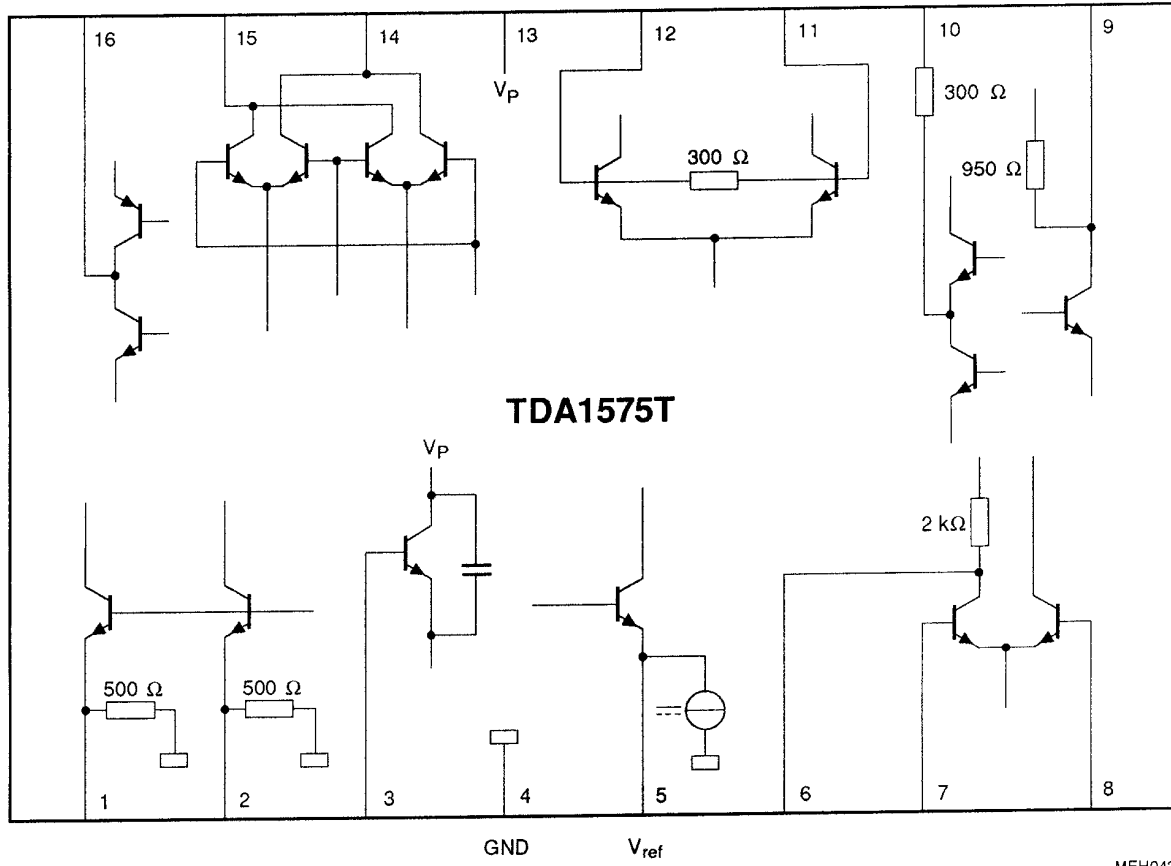


Fig.10 Internal circuits.

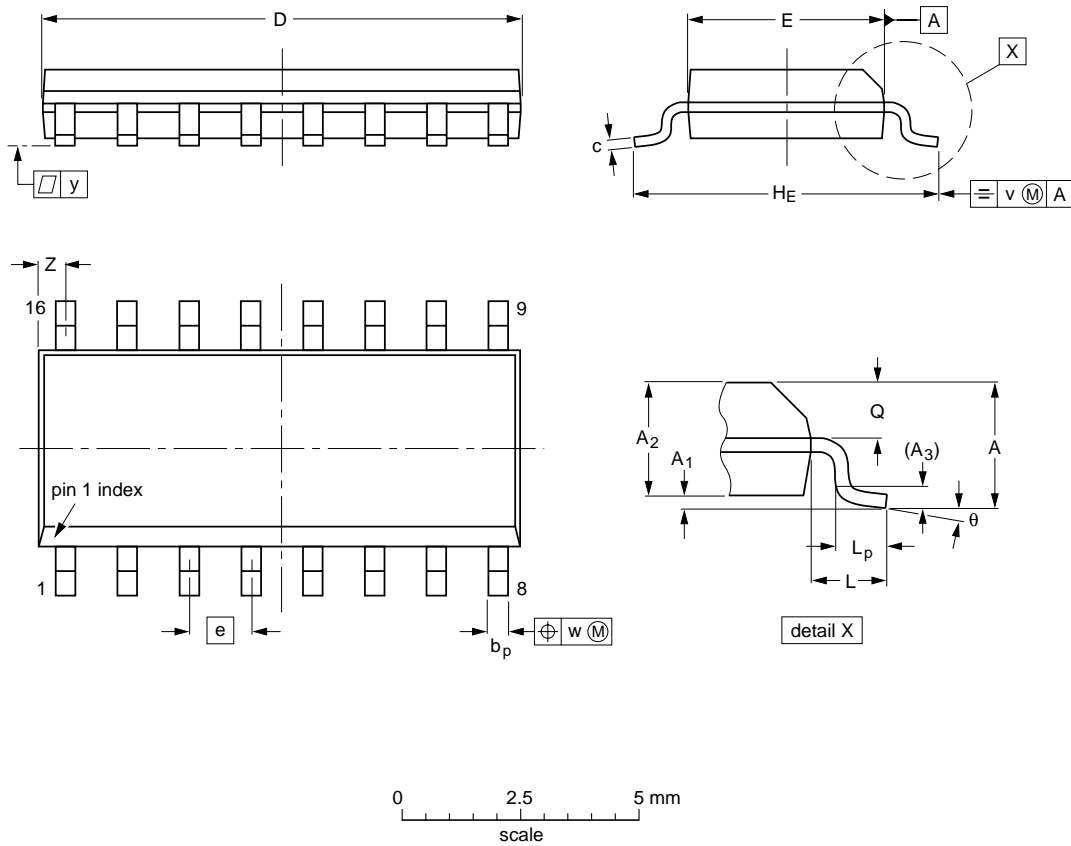
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PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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## FM front end circuit for CENELEC EN 55020 applications

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "*IC Package Databook*" (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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**TDA1575T****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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