

## MOS INTEGRATED CIRCUIT

 $\mu$ PD27C4000

## 4 M BIT CMOS PROM

**DESCRIPTION**

The  $\mu$ PD27C4000 is a 4 194 304-bit electrically programmable read-only memory. The word organization is selectable (word mode: 256K words by 16 bits, byte mode: 512K words by 8 bits). The device is fabricated using an advanced CMOS process which substantially saves power in operating and standby modes and is of use for a low power supply system.

The  $\mu$ PD27C4000DZ is available in a standard 40-pin cerdip package with a quartz window as an ultraviolet (UV) erasable PROM. The  $\mu$ PD27C4000CZ and  $\mu$ PD27C4000GW are available in plastic packages as ONE TIME PROMs.

**FEATURES**

- Word organization: 256K words by 16 bits (word mode)  
512K words by 8 bits (byte mode)
- Electrically programmable
- Fast access time: (See ORDERING INFORMATION)
- Low power dissipation: 50 mA MAX. active current  
100  $\mu$ A MAX. standby current
- High speed programming mode
- Input/Output TTL-compatible
- Single +5 V power supply
- Three state outputs
- Pinout compatibility with 40-pin mask ROM,  $\mu$ PD23C4000s

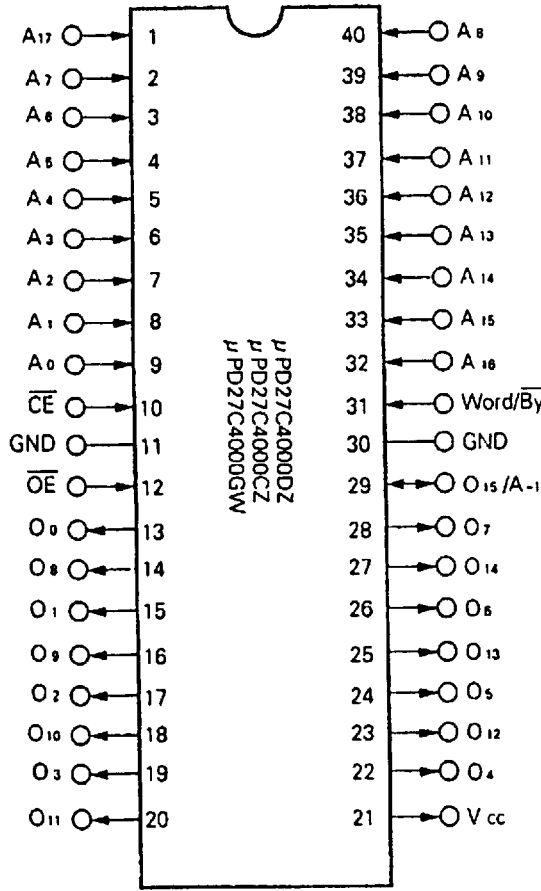
## ORDERING INFORMATION

PART NUMBER	ACCESS TIME (MAX.)	PACKAGE TYPE	FUNCTION	QUALITY GRADE
$\mu$ PD27C4000DZ-15	150 ns	40-pin Ceramic DIP with a quartz window (600 mil) (Mask programmable ROM compatible)	UV EPROM	STANDARD
$\mu$ PD27C4000DZ-17	170 ns			
$\mu$ PD27C4000DZ-20	200 ns			
$\mu$ PD27C4000CZ-15	150 ns	40-pin Plastic DIP (600 mil) (Mask programmable ROM compatible)	ONE TIME PROM	
$\mu$ PD27C4000CZ-17	170 ns			
$\mu$ PD27C4000CZ-20	200 ns			
$\mu$ PD27C4000GW-15	150 ns	40-pin Plastic SOP (525 mil) (Mask programmable ROM compatible)		
$\mu$ PD27C4000GW-17	170 ns			
$\mu$ PD27C4000GW-20	200 ns			

**Note**  $\mu$ PD27C4000 is compatible with the  $\mu$ PD23C4000.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

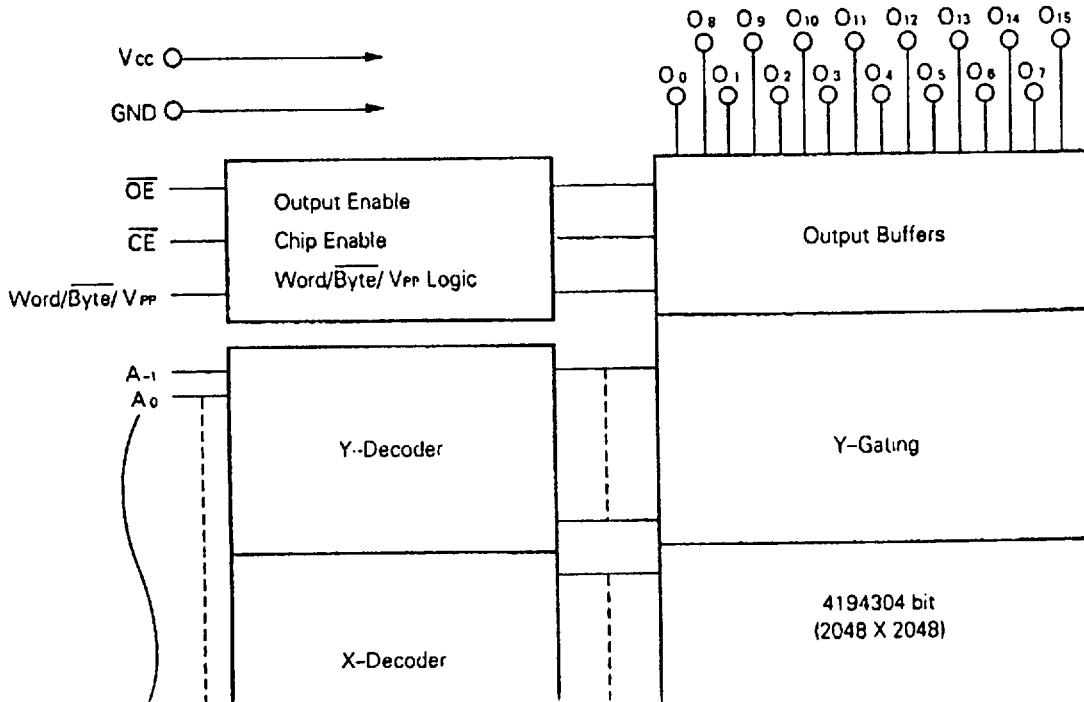
**PIN CONFIGURATION (Top View)**



**PIN NAMES**

- A<sub>0</sub> to A<sub>17</sub> : Address Inputs
- O<sub>0</sub> to O<sub>7</sub>, O<sub>8</sub> to O<sub>14</sub> : Data Outputs
- O<sub>15</sub>/A<sub>-1</sub> : Data 15 Output (word mode)/  
LSB Address Input (byte mode)
- Word/  $\overline{\text{Byte}}$ / V<sub>PP</sub> : Mode Selects/Program Voltage
- $\overline{\text{CE}}$  : Chip Enable
- $\overline{\text{OE}}$  : Output Enable
- V<sub>CC</sub> : Supply Voltage
- GND : Ground

**BLOCK DIAGRAM**



1.  $\mu$ PD27C4000 Operating Mode

## MODE SELECTION

Mode \ Symbol	$\overline{CE}$	$\overline{OE}$	Word/Byte /V <sub>PP</sub>	V <sub>CC</sub>	O <sub>0</sub> to O <sub>7</sub>	O <sub>8</sub> to O <sub>14</sub>	O <sub>15</sub> /A-1
Read (Word mode)	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	+5 V	Dout	Dout	Dout
Read (Byte mode)	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	+5 V	Dout	High-Z	LSB
Output Disable	V <sub>IL</sub>	V <sub>IH</sub>	X	+5 V	High-Z	High-Z	High-Z
Standby	V <sub>IH</sub>	X	X	+5 V	High-Z	High-Z	High-Z
Program	V <sub>IL</sub>	V <sub>IH</sub>	+12.5 V	+6.5 V	Din	Din	Din
Program Verify	X	V <sub>IL</sub>	+12.5 V	+6.5 V	Dout	Dout	Dout
Program Inhibit	V <sub>IH</sub>	V <sub>IH</sub>	+12.5 V	+6.5 V	High-Z	High-Z	High-Z

X can be either V<sub>IL</sub> or V<sub>IH</sub>

## (1) Read Mode (Word Mode)

Setting Word/Byte/V<sub>PP</sub> to "1",  $\overline{CE}$  to "0" and  $\overline{OE}$  to "0" puts the device into the read mode (Word Mode), and the data is valid at the output pins O<sub>0</sub> to O<sub>15</sub> after t<sub>acc</sub> from stabilizing all addresses, after t<sub>ce</sub> from the falling edge of  $\overline{CE}$  or after t<sub>oe</sub> from the falling edge of  $\overline{OE}$ .

## (2) Read Mode (Byte Mode)

Setting Word/Byte/V<sub>PP</sub> to "0",  $\overline{CE}$  to "0" and  $\overline{OE}$  to "0" puts the device into the read mode (Byte Mode), and the data is valid at the output pins O<sub>0</sub> to O<sub>7</sub> after t<sub>acc</sub> from stabilizing all addresses, after t<sub>ce</sub> from the falling edge of  $\overline{CE}$  or after t<sub>oe</sub> from the falling edge of  $\overline{OE}$ . In this case of byte mode, O<sub>8</sub> to O<sub>14</sub> are high-impedance, O<sub>15</sub>/A-1 is LSB address input.

## (3) Output Disable

Setting  $\overline{OE}$  to "1" puts pins O<sub>0</sub> to O<sub>15</sub> into the high-impedance state to disable data to be output. Therefore, when multiple  $\mu$ PD27C4000s are connected to the data bus, data can be read from any one of them by controlling  $\overline{OE}$ .

## (4) Standby Mode

Setting  $\overline{CE}$  to "1" puts the device into the standby mode, and the current at pin V<sub>CC</sub> drops from 50 mA to 1 mA. The standby current varies depending on the level of  $\overline{CE}$ : 1 mA max. (I<sub>CCS1</sub>) with  $\overline{CE} = V_{IH}$  min. or 100  $\mu$ A max. (I<sub>CCS2</sub>) with  $\overline{CE} \geq V_{CC} - 0.2$  V. In this mode, pins O<sub>0</sub> to O<sub>15</sub> are in the high-impedance state regardless of the state of  $\overline{OE}$ .

#### (5) Program Mode

The programming flowchart is shown in Fig. 1.

The  $\mu$ PD27C4000 is shipped with bits being set to all "1". Programming causes relevant bits to change to "0". Programming starts by setting  $V_{CC}$  to +6.5 V and  $\overline{Word/Byte}/V_{PP}$  to +12.5 V and initial address.

Data to be programmed can be directly input in the 16-bit format through the data bus.

The 0.1 ms program pulse (active low) is applied to pin  $\overline{CE}$  with  $\overline{OE} = "1"$  for the initial address, and immediately  $\overline{OE}$  is set to "0" to verify the data. If programming is not performed by applying the program pulse once, the program and program verification are executed X times ( $X \leq 10$ ) repeatedly to verify the 1-word, and then the programming is complete. On completion of 1-word programming, the address is incremented. The same sequence is repeated up to the last address.

**Note:** Byte Program Mode is not supported.

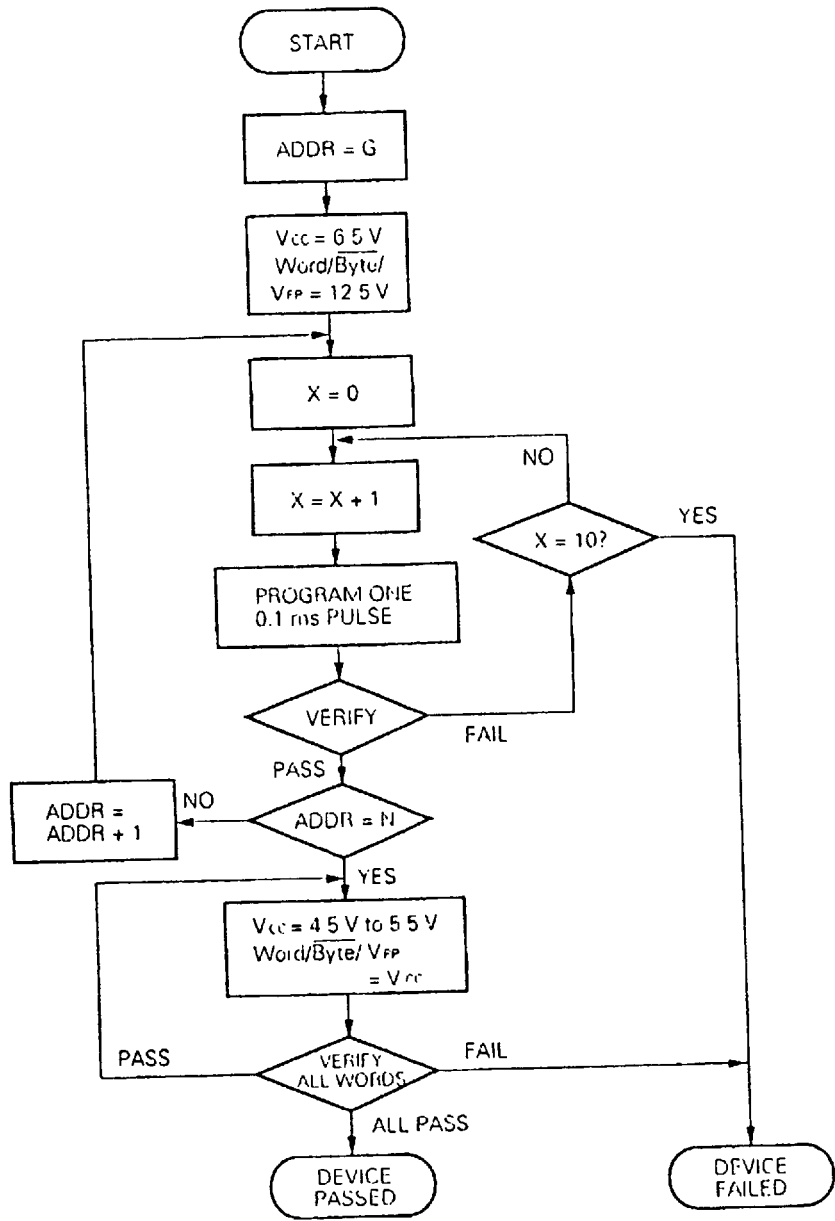
#### (6) Program Verify Mode

This mode is used to verify that the device is correctly programmed. After programming, check for the correct programming to each bit position in this mode. The programmed data can be verified with  $\overline{OE} = "0"$ .

#### (7) Program Inhibit Mode

This mode is used to program one of multiple  $\mu$ PD27C4000s whose pins  $\overline{OE}$ ,  $\overline{Word/Byte}/V_{PP}$  and  $O_0$  to  $O_{15}$  are connected in parallel. Programming is performed in the program mode described above. Other  $\mu$ PD27C4000s can be inhibited from being programmed by setting their  $\overline{CE}$  pins to "1" while the one device is programmed.

Fig. 1 Programming Flowchart



G = FIRST ADDR  
N = LAST ADDR

## 2. Electrical Specifications

### ABSOLUTE MAXIMUM RATINGS\*

Operating Temperature	-10 to +80	°C
Storage Temperature: ONE TIME PROM	-55 to +125	°C
Storage Temperature: UV EPROM	-65 to +125	°C
Output Voltage	-0.6 to +7	V
Input Voltage	-0.6 to +7	V
Input Voltage: A <sub>9</sub>	-0.6 to +13.5	V
Supply Voltage: V <sub>cc</sub>	-0.6 to +7	V
Program Voltage: Word/Byte/V <sub>pp</sub>	-0.6 to +13.5	V

\*COMMENT: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### READ OPERATION

### RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage V <sub>cc</sub>	V <sub>cc</sub>	4.5	5.0	5.5	V
Input High Voltage	V <sub>IH</sub>	2.0		V <sub>cc</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3		0.8	V
Operating Temperature	T <sub>a</sub>	0		70	°C

### DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Output High Voltage	V <sub>OHI</sub>	2.4			V	I <sub>OH</sub> = -400 μA
	V <sub>OHz</sub>	V <sub>cc</sub> - 0.7			V	I <sub>OH</sub> = -100 μA
Output Low Voltage	V <sub>OL</sub>			0.45	V	I <sub>OL</sub> = 2.1 mA
Output Leakage Current	I <sub>LO</sub>	-10		10	μA	V <sub>OUT</sub> = 0 to V <sub>cc</sub> , $\overline{OE}$ = V <sub>IH</sub>
Input Leakage Current	I <sub>LI</sub>	-10		10	μA	V <sub>IN</sub> = 0 to V <sub>cc</sub>
Word/Byte/V <sub>pp</sub> Current	I <sub>PP</sub>		1	100	μA	Word/Byte/V <sub>pp</sub> = 0 to V <sub>cc</sub>
V <sub>cc</sub> Current (active)	I <sub>CCA1</sub>			50	mA	$\overline{CE}$ = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub>
	I <sub>CCA2</sub>			50	mA	f = 6.7 MHz, I <sub>OUT</sub> = 0 mA
V <sub>cc</sub> Current (standby)	I <sub>CCS1</sub>			1	mA	$\overline{CE}$ = V <sub>IH</sub> MIN.
	I <sub>CCS2</sub>		1	100	μA	$\overline{CE} \geq V_{cc} - 0.2$ V, V <sub>IN</sub> = 0 to V <sub>cc</sub>

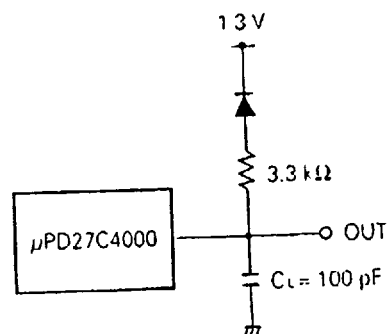
AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

PARAMETER	SYMBOL	$\mu$ PD27C4000-15		$\mu$ PD27C4000-17		$\mu$ PD27C4000-20		UNIT	TEST CONDITION
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Address to Output Delay	$t_{ACC}$		150		170		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	$t_{CE}$		150		170		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	$t_{OE}$		70		70		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ or $\overline{CE}$ High to Output Float	$t_{OF}$	0	55	0	55	0	60	ns	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$
Address to Output Hold	$t_{OH}$	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
Word/Byte Access Time	$t_{WB}$		150		170		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$

TEST CONDITIONS

- Output Load: See Fig. 2
- Input Rise and Fall Time  $\leq 20$  ns
- Input Pulse Levels: 0.45 V and 2.4 V
- Timing Measurement Reference Level  
 Input : 0.8 V and 2.0 V  
 Output: 0.8 V and 2.0 V

Fig. 2 Output Load

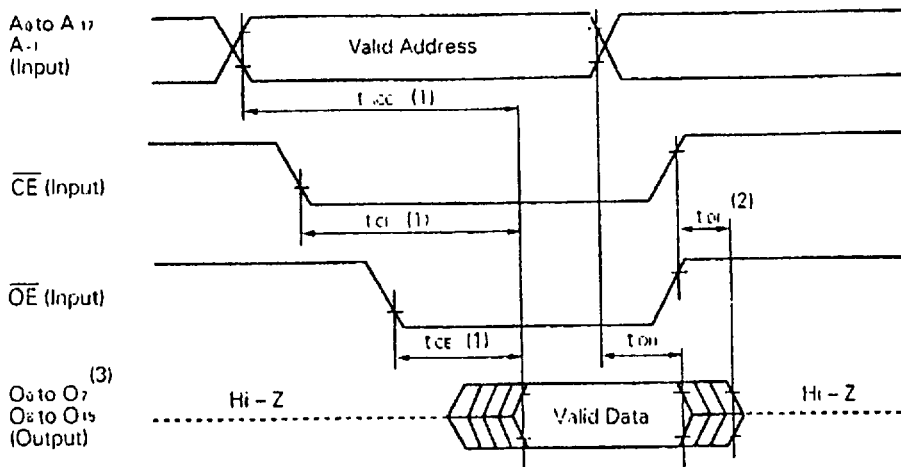


CAPACITANCE ( $T_a = 25$  °C,  $f = 1$  MHz)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input Capacitance	$C_{IN}$			14	pF	$V_{IN} = 0$ V
Output Capacitance	$C_{OUT}$			16	pF	$V_{OUT} = 0$ V



### Read Mode Timing



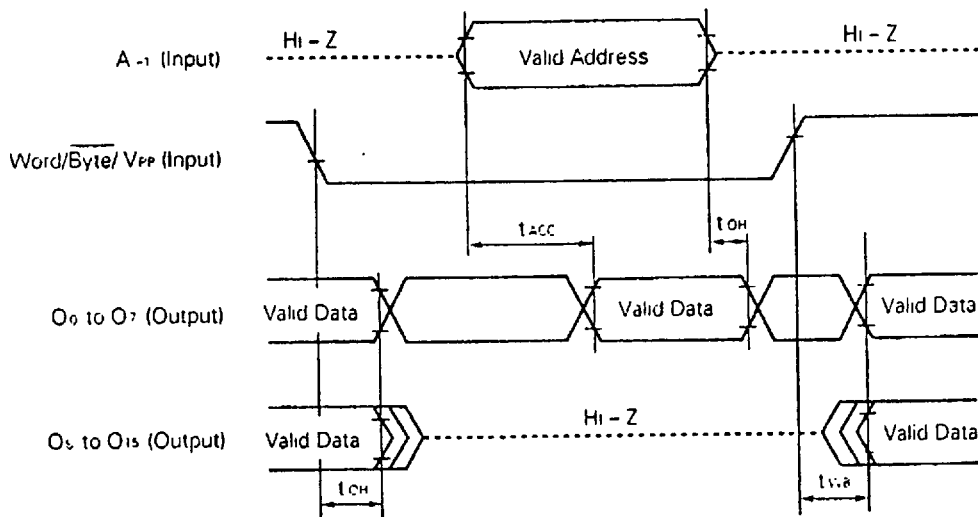
Notes: (1) For read operation, the definition of access time is as follows

$\overline{CE}$ Input Conditions	$\overline{OE}$ Input Conditions	Access Time Definition
before stabilizing address	before ( $t_{ACC} - t_{OE}$ )	$t_{ACC}$
	after ( $t_{ACC} - t_{OE}$ )	$t_{OE}$
after stabilizing address	before ( $t_{CE} - t_{OE}$ )	$t_{CE}$
	after ( $t_{CE} - t_{OE}$ )	$t_{OE}$

(2)  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first

(3) In the byte mode, O<sub>8</sub> to O<sub>14</sub> are high-impedance (O<sub>15</sub> is A-1)

### Word/Byte Switch Timing



Note: (1)  $\overline{CE} = V_{IL}$ ,  $\overline{OE} = V_{IL}$

## PROGRAM OPERATION

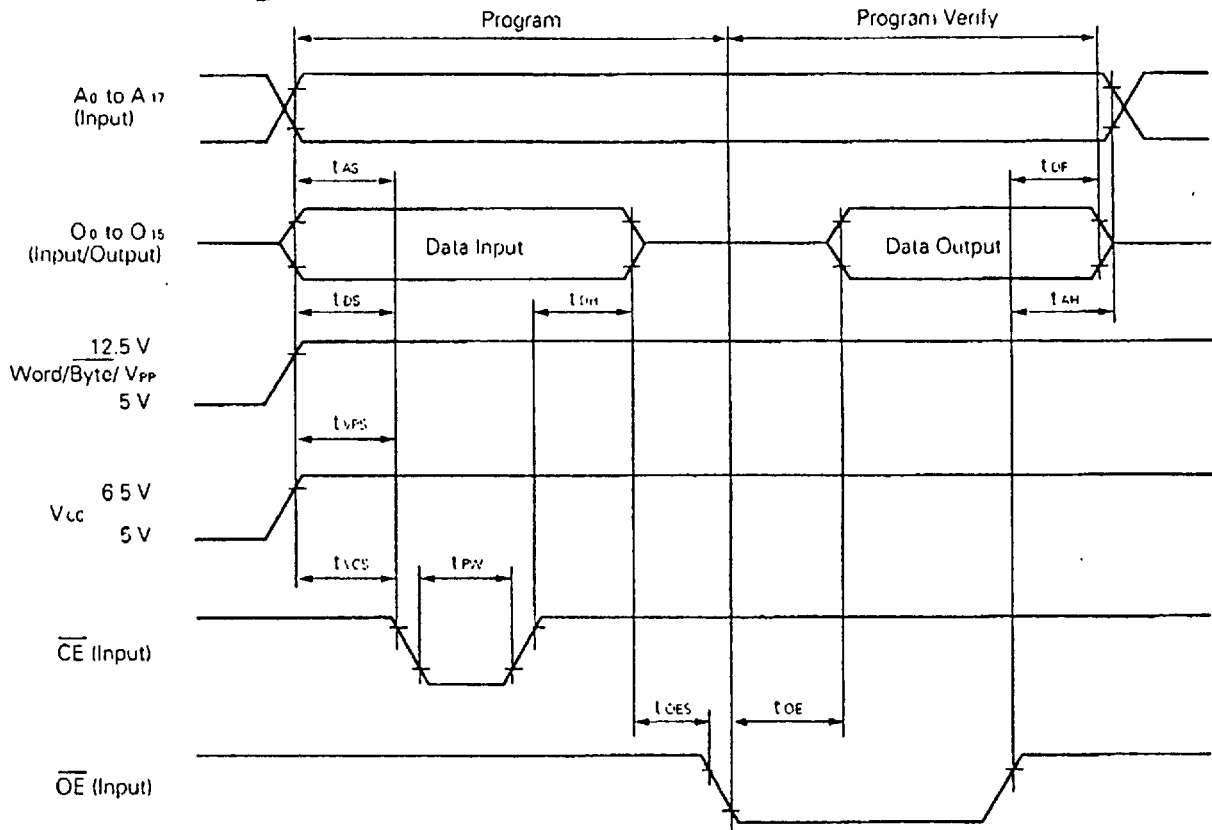
DC CHARACTERISTICS ( $T_a = 25 \pm 5 \text{ }^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25 \text{ V}$ ,  $\text{Word/Byte}/V_{PP} = 12.5 \pm 0.3 \text{ V}$ )

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Input High Voltage	$V_{IH}$	2.4		$V_{CC} + 0.3$	V	
Input Low Voltage	$V_{IL}$	-0.3		0.8	V	
Input Leakage Current	$I_{LI}$	-10		10	$\mu\text{A}$	$V_{IH} = 0 \text{ to } V_{CC}$
Output High Voltage	$V_{OH}$	2.4			V	$I_{OH} = -400 \mu\text{A}$
Output Low Voltage	$V_{OL}$			0.45	V	$I_{OL} = 2.1 \text{ mA}$
$V_{CC}$ Current	$I_{CC}$			50	mA	
Word/Byte/ $V_{PP}$ Current	$I_{PP}$			50	mA	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$

AC CHARACTERISTICS ( $T_a = 25 \pm 5 \text{ }^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25 \text{ V}$ ,  $\text{Word/Byte}/V_{PP} = 12.5 \pm 0.3 \text{ V}$ )

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Address Setup Time	$t_{AS}$	2			$\mu\text{s}$	
$\overline{OE}$ Setup Time	$t_{OES}$	2			$\mu\text{s}$	
Data Setup Time	$t_{DS}$	2			$\mu\text{s}$	
Address Hold Time	$t_{AH}$	2			$\mu\text{s}$	
Data Hold Time	$t_{DH}$	2			$\mu\text{s}$	
$\overline{OE}$ High to Output Float	$t_{OF}$	0		130	ns	
Word/Byte/ $V_{PP}$ Setup Time	$t_{VPS}$	2			$\mu\text{s}$	
$V_{CC}$ Setup Time	$t_{VCS}$	2			$\mu\text{s}$	
Program Pulse Width	$t_{PW}$	0.095	0.1	0.105	ms	
$\overline{OE}$ to Output Delay	$t_{OE}$			150	ns	

### Programming Mode Timing



- Notes:**
- (1) V<sub>CC</sub> must be applied simultaneously or before Word/Byte/V<sub>PP</sub> and removed simultaneously or after Word/Byte/V<sub>PP</sub>.
  - (2) Word/Byte/V<sub>PP</sub> must not be greater than +13.5 V including overshoot.
  - (3) Removing and reinserting the device while a voltage of 12.5 V is applied to pin Word/Byte/V<sub>PP</sub> may affect the device reliability.

### 3. ERASURE

Programmed data on the  $\mu$ PD27C4000DZ can be erased by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254 nm ultraviolet rays. A lighting level of 15 w · s/cm<sup>2</sup> (min.) is required to completely erase written data (ultraviolet ray intensity X exposure time).

It takes approximately 20 minutes to completely erase with an ultraviolet lamp rated at 12 mw/cm<sup>2</sup>. Place the  $\mu$ PD27C4000DZ within 2.5 cm from the lamp tubes. Remove any filter on the lamp.

### 4. SCREENING OF ONE TIME PROM

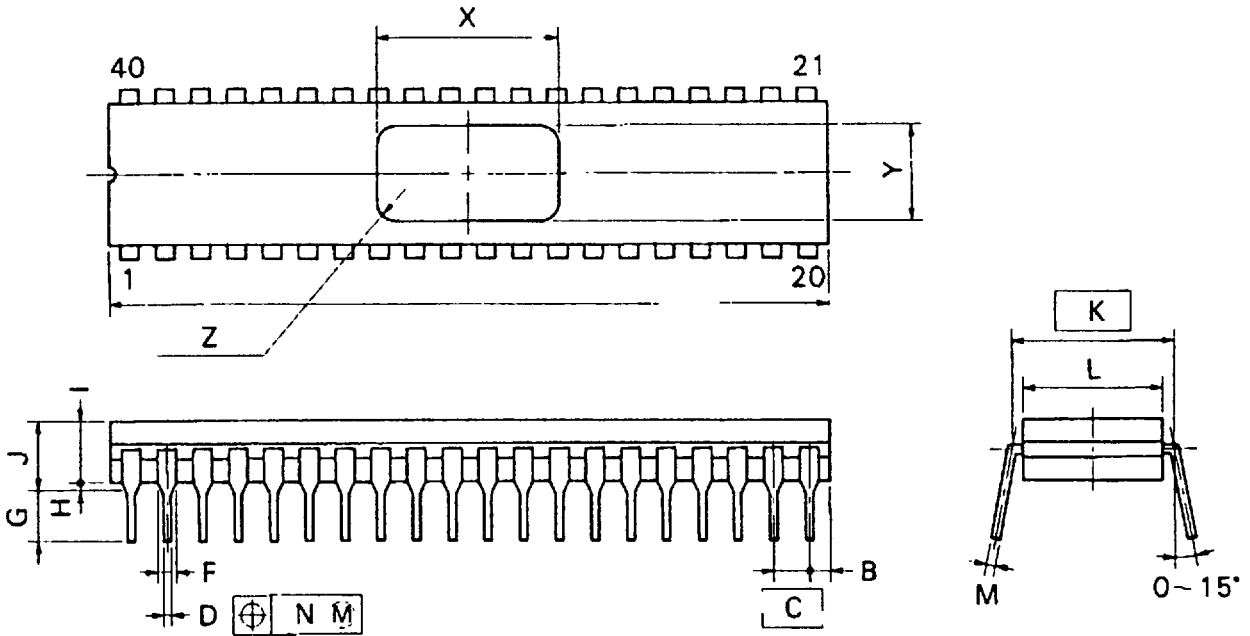
Initial-data-retention failure in the ONE TIME PROM cannot be eliminated before shipment to the customers due to the characteristic of this product itself.

In case of expecting reliability equivalent to conventional EPROM, NEC recommends the following screening at customer's site for the elimination of both programming failure and data retention failure.

- (1) After programming data, verify data and reject failures.
- (2) Perform high-temperature storage at 125 °C for 24 ± 4 hours.
- (3) Verify data again and reject failures.

PACKAGE INFORMATION

40 PIN CERAMIC DIP (CERDIP) (WINDOW) (600mil)



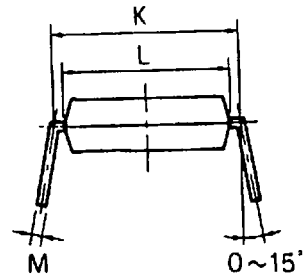
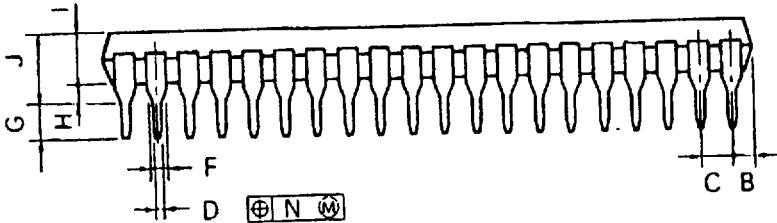
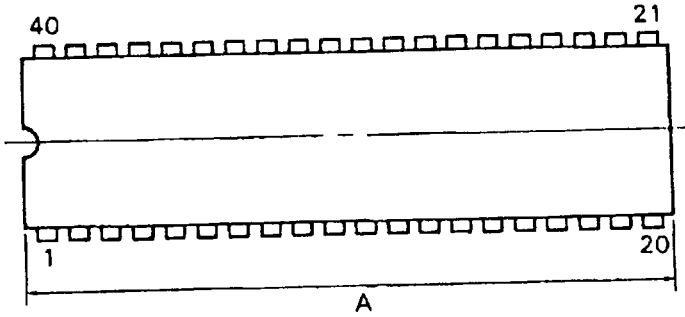
P40DW 100-600WA2

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 <sup>+0.10</sup>	0.020 <sup>+0.004</sup>
F	1.2 MIN.	0.047 MIN.
G	3.5 <sup>+0.3</sup>	0.138 <sup>+0.012</sup>
H	0.51 MIN.	0.020 MIN.
I	3.80	0.150
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	14.66	0.577
M	0.25 <sup>+0.05</sup>	0.010 <sup>+0.003</sup>
N	0.25	0.01
X	12.5	0.492
Y	8.5	0.335
Z	4 R20	4-RO 079

40PIN PLASTIC DIP (600 mil)



P40C-100-600A

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	53.34 MAX.	2.100 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 <sup>0.10</sup>	0.020 <sup>0.004</sup> / <sub>0.005</sub>
F	1.2 MIN.	0.047 MIN.
G	3.6 <sup>0.3</sup>	0.142 <sup>0.012</sup>
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	0.25 <sup>0.10</sup> / <sub>0.05</sub>	0.010 <sup>0.004</sup> / <sub>0.005</sub>
N	0.25	0.01

**RECOMMENDED SOLDERING CONDITIONS**

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

**TYPES OF THROUGH HOLE MOUNT DEVICE**

[ $\mu$ PD27C4000DZ, 27C4000CZ]

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below	WS60-00

[MEMO]

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Application examples recommended by NEC Corporation

Standard: Data processing and office equipment, Communication equipment (terminal, mobile), Test and Measurement equipment, Audio and Video equipment, Other consumer products, Industrial robots, etc.

Special: Automotive and Transportation equipment, Communication equipment (trunk line), Train and Traffic control devices, Burning control systems, antidisaster systems, anticrime systems etc