

# DATA SHEET

**74F1779**

8-bit bidirectional binary counter (-State)

Product specification  
IC15 Data Handbook

1989 Apr 06

## 8-bit bidirectional binary counter (3-State)

74F1779

## FEATURES

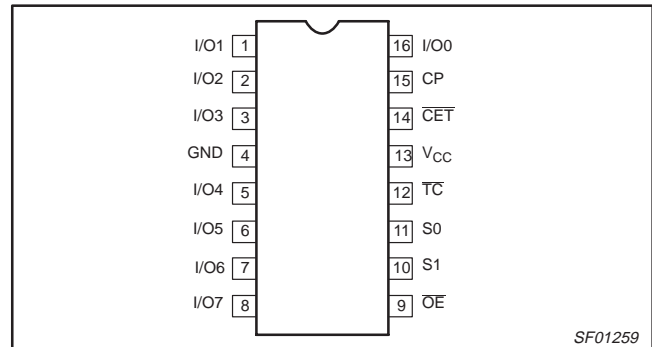
- Multiplexed 3-State I/O ports for bus oriented applications
- Built-in look-ahead carry capability
- Center power pins to reduce effects of package inductance
- Count frequency 145MHz typical
- Supply current 90mA typical
- See 74F269 for 24-pin separate I/O port version
- See 74F579 for 20-pin version
- See 74F779 for 16-pin version with abbreviated function table

## DESCRIPTION

The 74F1779 is a fully synchronous 8-stage up/down counter with multiplexed 3-State I/O ports for bus-oriented applications. All control functions (hold, count up, count down, synchronous load) are controlled by two mode pins (S0, S1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock. When  $\overline{CET}$  is High, the data outputs are held in their current state and  $\overline{TC}$  is held High. the  $\overline{TC}$  output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

The 74F1779 differs from 74F779 in that it has an additional hold mode as described in the Function Table.

## PIN CONFIGURATION



TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F1779	130MHz	100mA

## ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PACKAGE DRAWING NUMBER
16-pin Plastic DIP	N74F1779N	SOT38-4
16-pin Plastic SOL	N74F1779D	SOT162-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

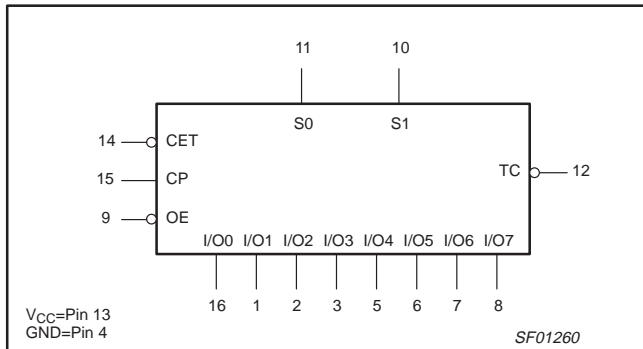
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/On	Data inputs	3.5/1.0	70 $\mu$ A/0.6mA
	Data outputs	150/40	3.0mA/24mA
S0, S1	Select inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/1.0	20 $\mu$ A/0.6mA
CP	Clock input (active rising edge)	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{TC}$	Terminal Count output (active Low)	50/33	1.0mA/20mA

**NOTE:** One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

# 8-bit bidirectional binary counter (3-State)

74F1779

## LOGIC SYMBOL



## FUNCTION TABLE

INPUTS					OPERATING MODE
S1	S0	CET	OE	CP	
X	X	X	H	X	I/O0 to I/O7 in High impedance
X	X	X	L	X	Flip-flop outputs appear on I/O lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ( $\overline{TC}$ held High)
H	H	X	X	↑	Hold
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level

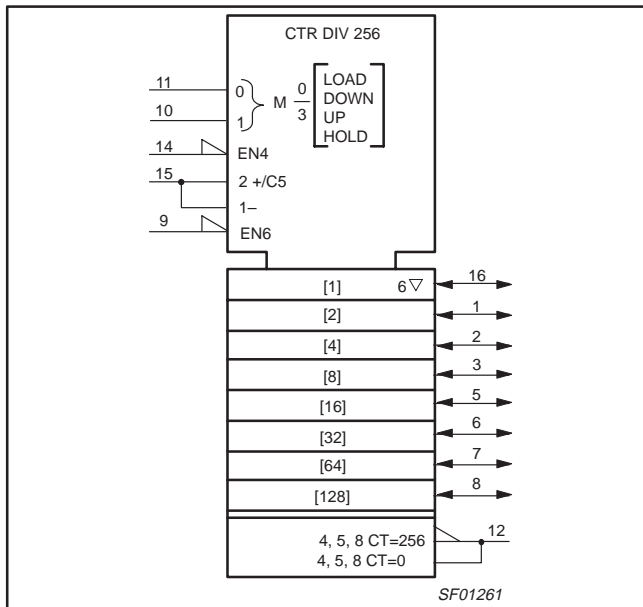
L = Low voltage level

X = Don't care

↑ = Low-to-High clock transition

(not LL) = S0 and S1 should never be Low voltage level at the same time in the hold mode only.

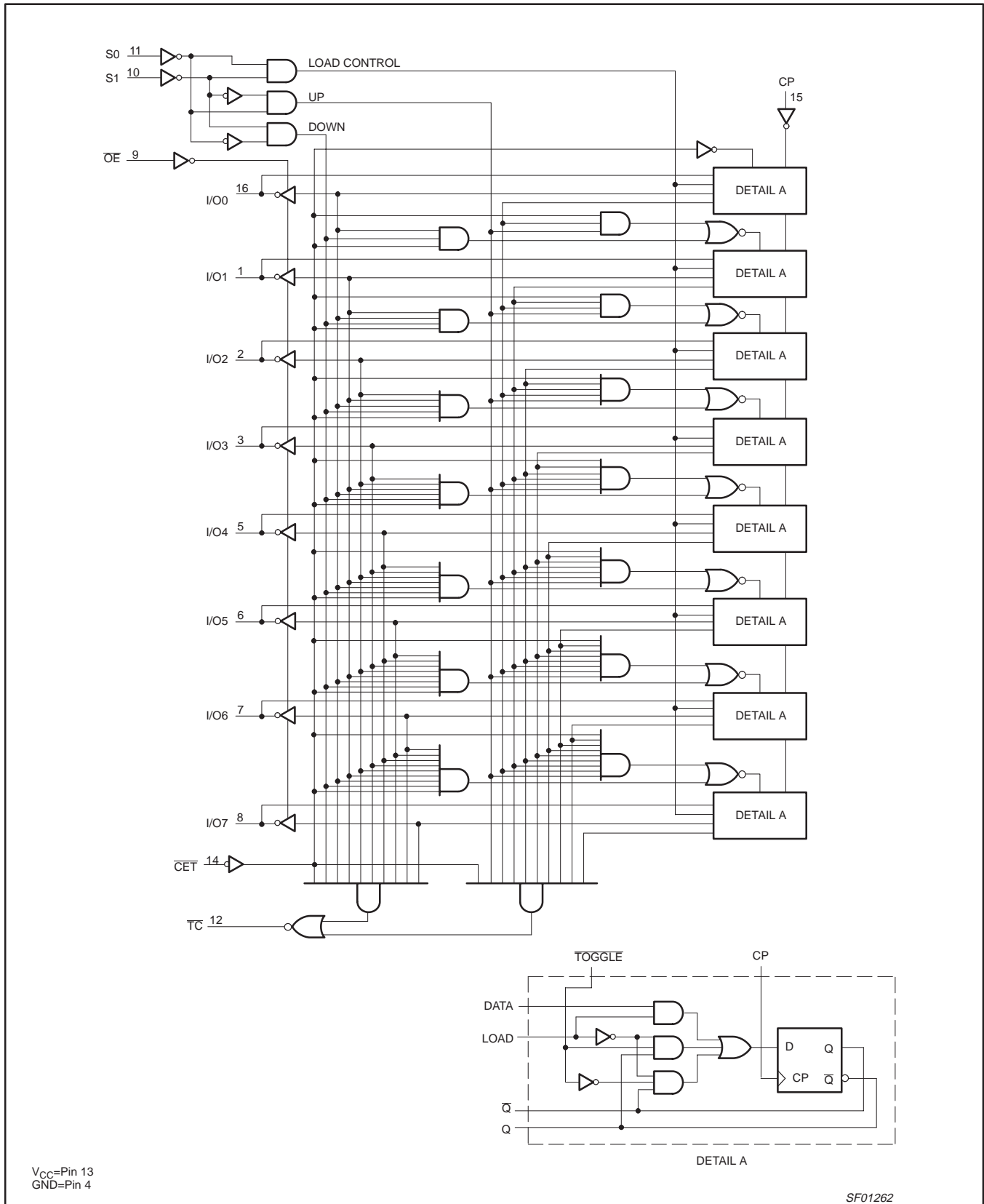
## IEC/IEEE SYMBOL



# 8-bit bidirectional binary counter (3-State)

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## LOGIC DIAGRAM



## 8-bit bidirectional binary counter (3-State)

74F1779

**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT	
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V	
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V	
I <sub>IN</sub>	Input current	-30 to +5	mA	
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V	
I <sub>OUT</sub>	Current applied to output in Low output state	TC	40	mA
		I/On	48	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C	
T <sub>stg</sub>	Storage temperature	-65 to +150	°C	

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current	TC		-1	mA
		I/On		-3	mA
I <sub>OL</sub>	Low-level output current	TC		20	mA
		I/On		24	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

## 8-bit bidirectional binary counter (3-State)

74F1779

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>			LIMITS			UNIT
						MIN	TYP <sup>2</sup>	MAX	
V <sub>OH</sub>	High-level output voltage	$\overline{TC}$	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN	I <sub>OH</sub> = -1mA	±10%V <sub>CC</sub>	2.5			V
					±5%V <sub>CC</sub>	2.7	3.4		V
		I/On	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN	I <sub>OH</sub> = -3mA	±10%V <sub>CC</sub>	2.4			V
					±5%V <sub>CC</sub>	2.7	3.3		V
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX V <sub>IH</sub> = MIN	I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.30	0.50	V
					±5%V <sub>CC</sub>		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>				-0.73	-1.2	V
I <sub>I</sub>	Input current at maximum input voltage	I/On	V <sub>CC</sub> = 5.5V, V <sub>I</sub> = 5.5V					1	mA
		others	V <sub>CC</sub> = 5.5V, V <sub>I</sub> = 7.0V					100	μA
I <sub>IH</sub>	High-level input current	except I/On	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V					20	μA
I <sub>IL</sub>	Low-level input current	I/On	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V					-0.6	mA
I <sub>IH</sub> +I <sub>OZH</sub>	Off-state output current High-level voltage applied	I/On	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V					70	μA
I <sub>IL</sub> +I <sub>OZL</sub>	Off-state output current Low-level voltage applied		V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V					-600	μA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>		V <sub>CC</sub> = MAX			-60		-150	mA
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX				100	145	mA
		I <sub>CCL</sub>					100	145	mA
		I <sub>CCZ</sub>					110	155	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V. T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**AC ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	115	130		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to I/On	Waveform 1	4.0 5.0	6.5 7.0	10.0 10.5	4.0 5.0	10.5 11.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to $\overline{TC}$	Waveform 1	4.0 4.5	6.5 6.5	9.0 9.0	3.5 4.0	9.5 9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CET to $\overline{TC}$	Waveform 2	2.0 2.5	4.0 4.5	6.5 7.0	2.0 2.5	7.5 7.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level	Waveform 4 Waveform 5	2.0 4.5	4.0 6.5	6.5 9.0	2.0 4.0	7.5 9.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Enable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.0 7.0	1.0 1.0	6.5 7.5	ns

# 8-bit bidirectional binary counter (3-State)

74F1779

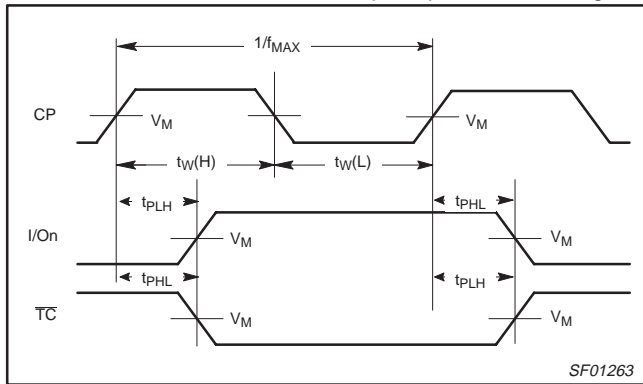
## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low I/O <sub>n</sub> to CP	Waveform 3	4.0 3.5			4.5 3.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low I/O <sub>n</sub> to CP	Waveform 3	0 0			0 0		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low CET to CP	Waveform 3	4.5 7.0			5.0 8.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low CET to CP	Waveform 3	0 0			0 0		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low Sn to CP	Waveform 3	7.5 8.5			8.0 9.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low Sn to CP	Waveform 3	0 0			0 0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse width, High or Low	Waveform 1	3.0 4.5			3.0 5.5		ns

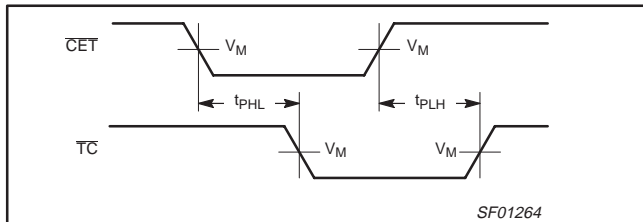
## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V.

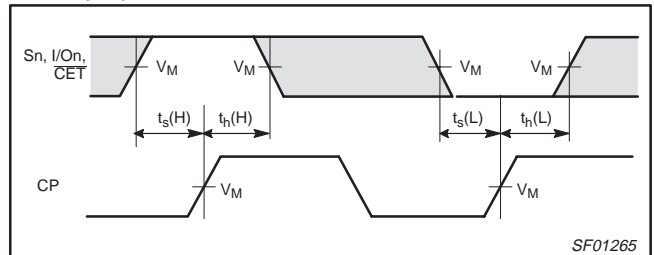
The shaded areas indicate when the input is permitted to change for predictable output performance.



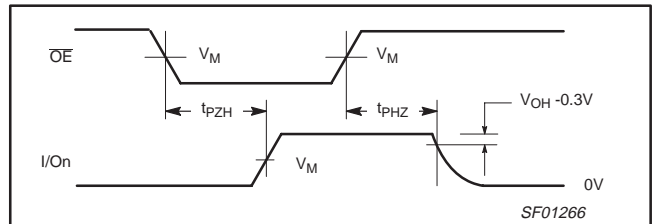
**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**



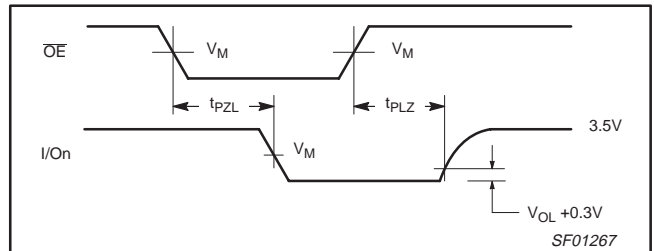
**Waveform 2. Propagation Delay, CET Input to Terminal Count Output**



**Waveform 3. Data Setup and Hold Times**



**Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

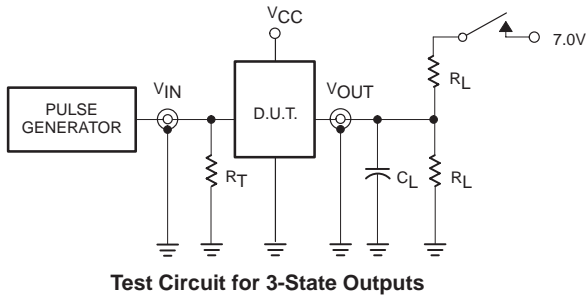


**Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

# 8-bit bidirectional binary counter (3-State)

74F1779

## TEST CIRCUIT AND WAVEFORMS



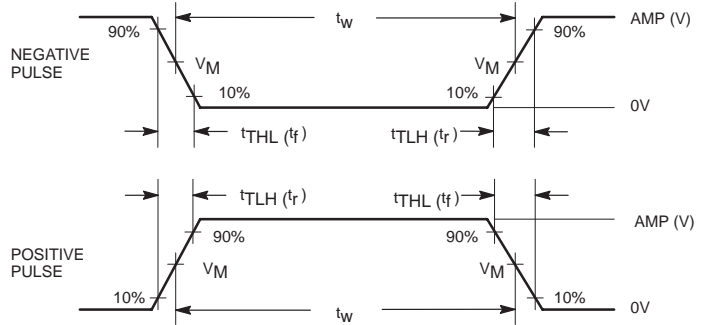
Test Circuit for 3-State Outputs

### SWITCH POSITION

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

### DEFINITIONS:

- $R_L$  = Load resistor; see AC electrical characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

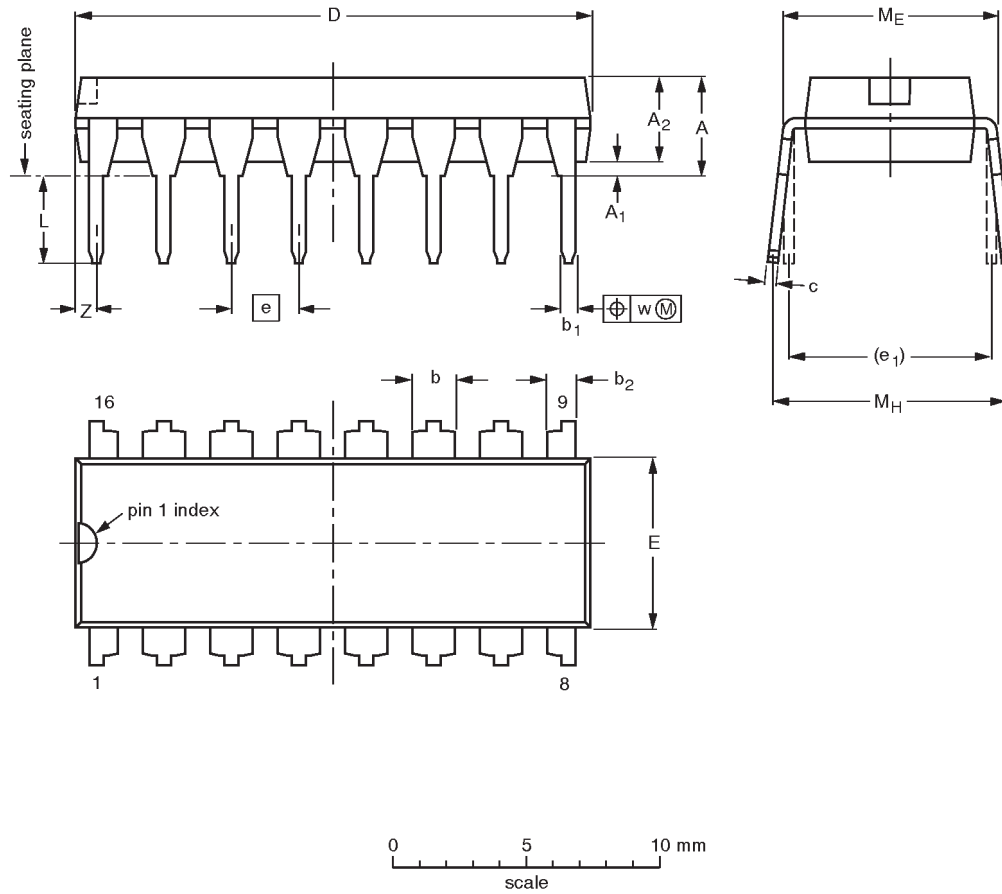


# 8-bit bidirectional binary counter (3-State)

74F1779

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

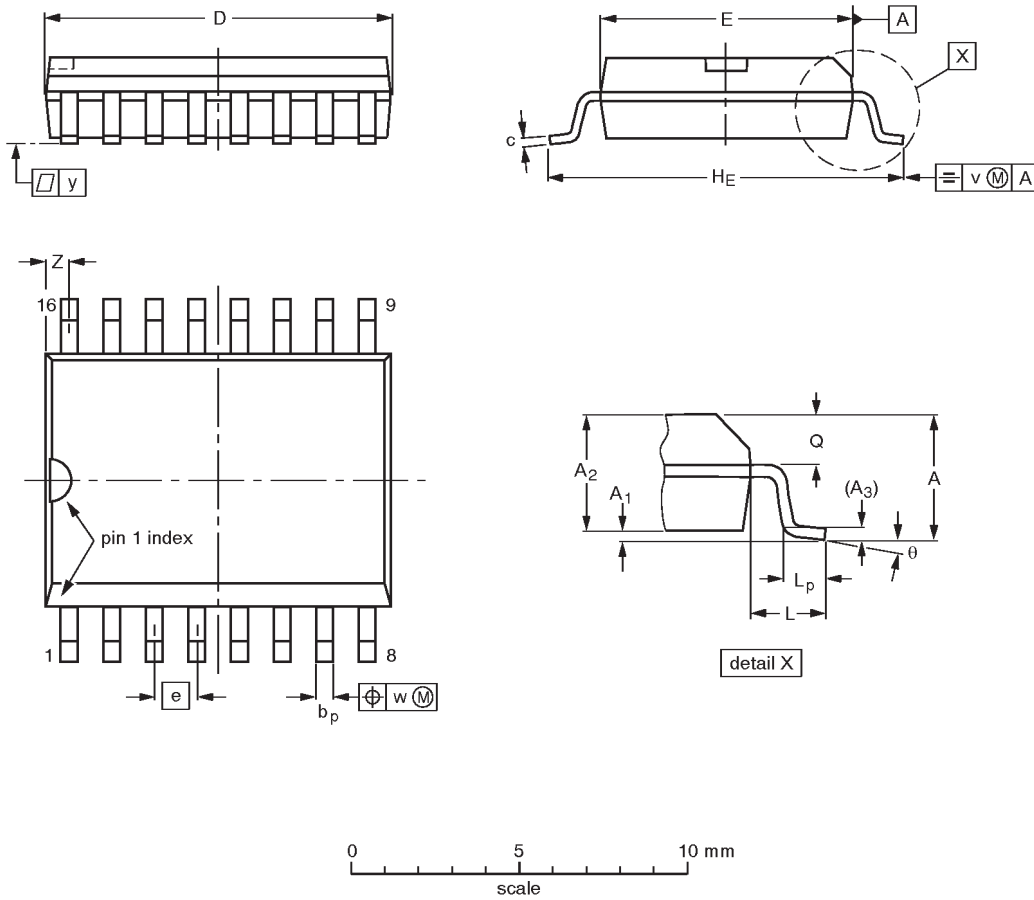
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

# 8-bit bidirectional binary counter (3-State)

74F1779

**SO16: plastic small outline package; 16 leads; body width 7.5 mm**

**SOT162-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				-92-11-17 95-01-24

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8-bit bidirectional binary counter (3-State)

74F1779

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**NOTES**

## 8-bit bidirectional binary counter (3-State)

74F1779

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	<b>Full Production</b>	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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