OKI semiconductor
MSM6976RS

BAND SPRIT FILTER FOR DUPLEX COMMUNICATION OF VOICE AND DATA

GENERAL DESCRIPTION

The MSM6976 is an one chip band split filter LSI which is fabricated by OKI's low power consumption silicon gate CMOS based on switched capacitor filter technology. In conbination with CCITT V.21 modem set, the MSM6976 performs band split filter function for duplex communication of voice and data over the switched telephone network.
The MSM6976 consists of 2 x BPF (band pass filter), 2 x BEF (band elimination filter), attenuator, switch circuit and OSC circuit.
BPF implements data channel by being located in modem transmission line, and BEF prevents voice signal crosstalk from voice channel to data channel by being located in voice channel.

Some application examples are as follows:

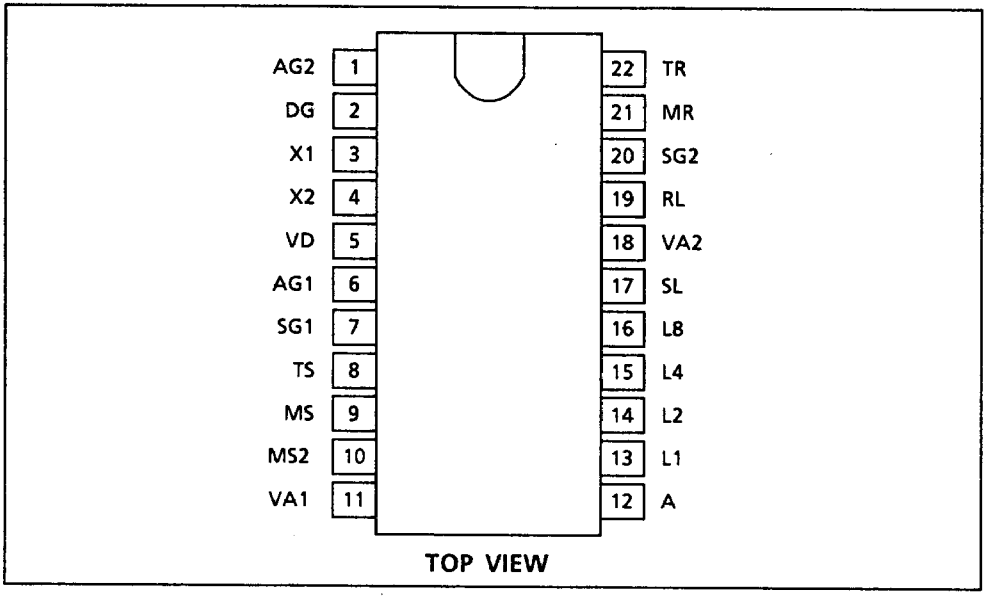
- Telewriting system
- Duplex communication of personal computer and telephone
- Telemetry system

Duplex communication system of voice and data can easily be constructed by combining the MSM6976 with OKI's MSM6926 (CCITT V.21 FSK modem).

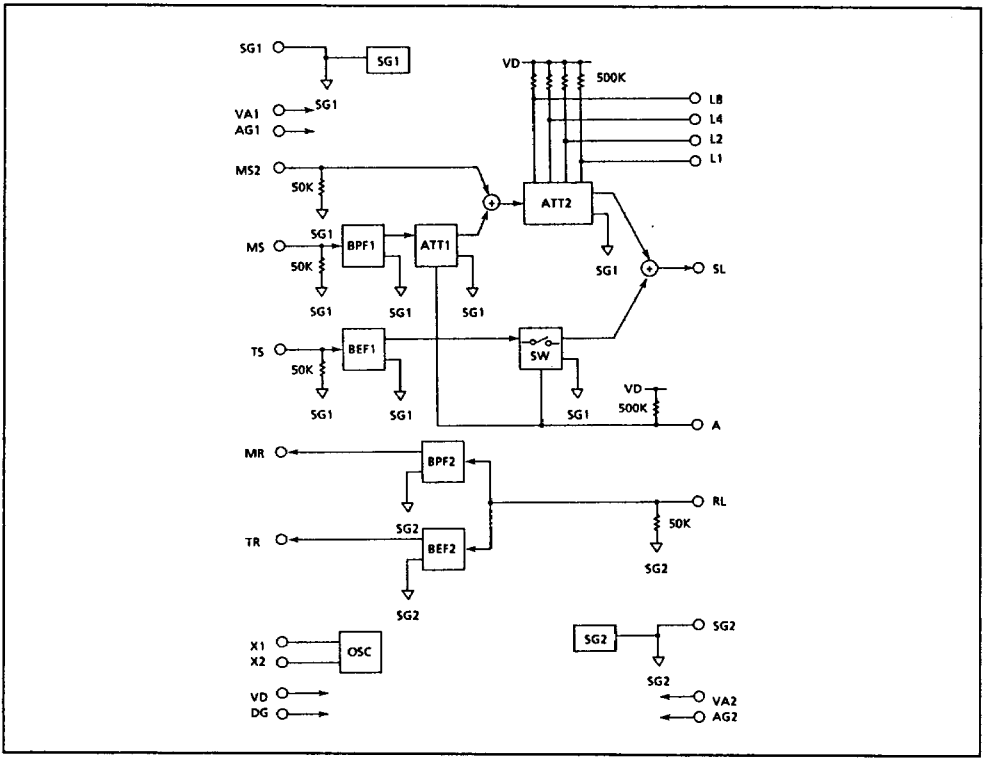
FEATURES

- High-accuracy, high-stability operation by adoption of the SCF circuit
- Built-in variable attenuator for modem data transmission level setting
- Possible selection of duplex voice and data communication or data communication only
- Built-in pull up resistor for digital input
- Low power consumption: Typ. 180 mW

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Remarks
Supply voltage	VA1 VA2	Ta = 25°C	− 0.3~ + 15	V	VA1 = VA2 VA1, VA2 > VD AG1 = AG2 = DG
	VD		− 0.3~ + 7	V	
Input voltage	V_{IA}		− 0.3~VA1 (or VA2) + 0.3	V	MS, MS2, TS, RL
	V_{ID}		− 0.3~VD + 0.3	V	A, L1, L2, L4, L8
Output voltage	V_O		− 0.3~VA1 (or VA2) + 0.3	V	SL, MR, TR
Storage temperature	Tstg		− 55~ + 150	°C	

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Supply voltage	VA1 VA2		10.8	12.0	13.2	V	VA1 = VA2 AG1 = AG2 = DG
	VD		4.75	5.0	5.25	V	
Operating temperature	Top		0		+ 70	°C	
Input signal level	V_{IN}				+ 8	dBm	MS, MS2, TS, RL 0dBm = 0.775Vrms
Load impedance	Z_{LOAD}		50			KΩ	SL, MR, TR
External parts	X'tal			3.579545		MHz	See Fig. 3
	C_1		1			µF	
	C_2			22		pF	
	C_3			0.1		µF	
	C_4			0.047		µF	
	C_5			2.2		µF	
	R_1			600		Ω	
	R_2			51		KΩ	

ELECTRICAL CHARACTERISTICS

(VA1 = VA2 = 12V ± 10%, VD = 5V ± 5%, Ta = 0~ + 70°C)

• DC and Digital Interface Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Current consumption	I_A	$I_A = I_{A1} + I_{A2}$		15	35	mA	VA1, VA2
	I_D	A, L1~L8 open			0.5	mA	VD
Input voltage	V_{IL}		0		0.8	V	A, L1, L2, L4, L8 (Pull-up resistance: 500KΩ Typ)
	V_{IH}		2.4		VD	V	
Input leakage current	I_{IL}	$V_I = 0V$	− 2	− 10	− 50	μA	
	I_{IH}	$V_I = VD$	− 10		+ 10	μA	
Input pin DC bias voltage	V_{BI}		VA/2-1	VA/2	VA/2 + 1	V	MS, MS2, TS, RL
Output pin DC bias voltage	V_{BO}		VA/2-1	VA/2	VA/2 + 1	V	SL, MR, TR

• Analog Interface Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Input impedance	Z_I		25	50	100	KΩ	MS, MS2, TS, RL
Output impedance	Z_O				200	Ω	SL, MR, TR
Transmission loss	G_{MS2}	ATT2 = 0dB	− 1.0	0	+ 1.0	dB	MS2→SL
Voice signal crosstalk	C_{TALK}	A = VD			− 60	dB	TS→SL

• ATT1

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Attenuation	G_{ATT1}	A = VD	− 0.5	0	+ 0.5	dB	
		A = GND	3.5	4.0	4.5	dB	

• ATT2

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Attenuation setting range	R_{ATT2}		0		15	dB	
Attenuation setting error	E_{ATT2}		− 0.5	0	+ 0.5	dB	

- **BEF1, BEF2**

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Frequency characteristic	f_{BEF}						See Fig. 1
Output noise	ICN_{BEF}				– 58	dBmp	Psophometer

- **BPF1, BPF2**

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks
Frequency characteristic	f_{BPF}						See Fig. 2
Group delay distorsion	D_{BPF}	f = 1600~ 1900 Hz		900	2000	μS	
Output noise	ICN_{BPF}				– 58	dBmp	Psophometer

● BPF1, BPF2 Frequency Characteristic

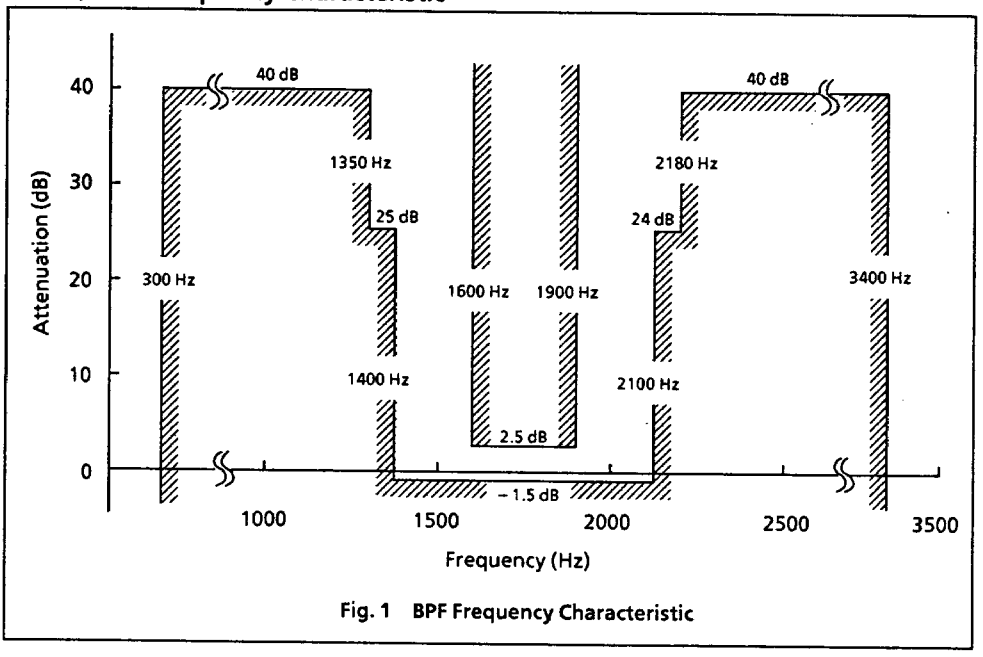


Fig. 1 BPF Frequency Characteristic

● BEF1, BEF2 Frequency Characteristic

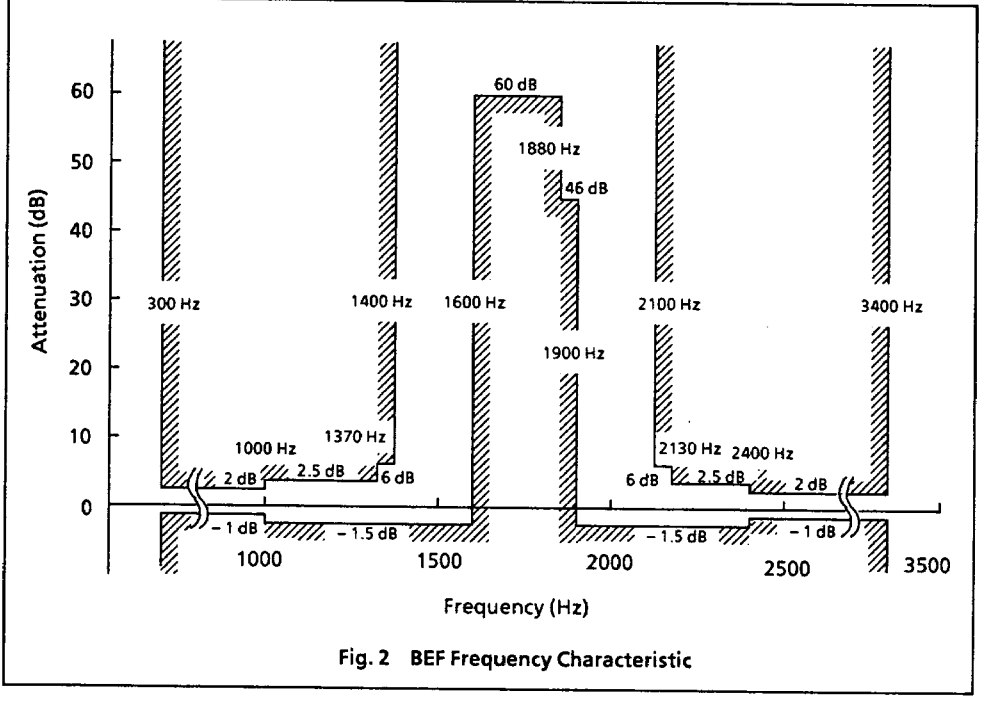


Fig. 2 BEF Frequency Characteristic

PIN ASSIGNMENT

Pin No.	Name	Explanation
1	AG2	Analog ground 0V
2	DG	Digital ground 0V
3	X1	Crystal oscillator connecting pins
4	X2	
5	VD	+ 5V power supply
6	AG1	Analog grond 0V
7	SG1	Analog bias circuit output
8	TS	Voice signal input (from telephone set)
9	MS	Send signal input from modem (300 bps)
10	MS2	Send signal input from modem (1200 bps)
11	VA1	+ 12V power supply
12	A	Selection of duplex voice and data communication or data communication only
13	L1	Modem data transmission level setting (0~15 dB)
14	L2	
15	L4	
16	L8	
17	SL	Send signal output
18	VA2	+ 12V power supply
19	RL	Receive signal input
20	SG2	Analog bias circuit output
21	MR	Receive signal output to modem (300 bps)
22	TR	Voice signal output (to telephone set)

INSTRUCTIONS FOR USE

1. Analog Interface Pins

Since the annalog interface pins (MS, MS2, TS, MR, TR, SL, and RL) are DC-biased in the IC, provide AC couping with coupling capaciters as shown in Fig. 3.

2. Attenuator Seting

- ATT1 : Ground the A pin for duplex voice and data communication. The modem data is attenuated by 4 dB by ATT1 and combined with the voice signal for output to the SL pin.

  When the modem data is sent and received exclusively, set the A pin to the same potential as VD or open the A pin. The voice signal is out off, and only the modem data is output.

- ATT2 : Sets the modem data transmission level.
  The attenuation level can be set by 1 dB steps between 0 dB and 15 dB.

(L1: LSB, L8: MSB)

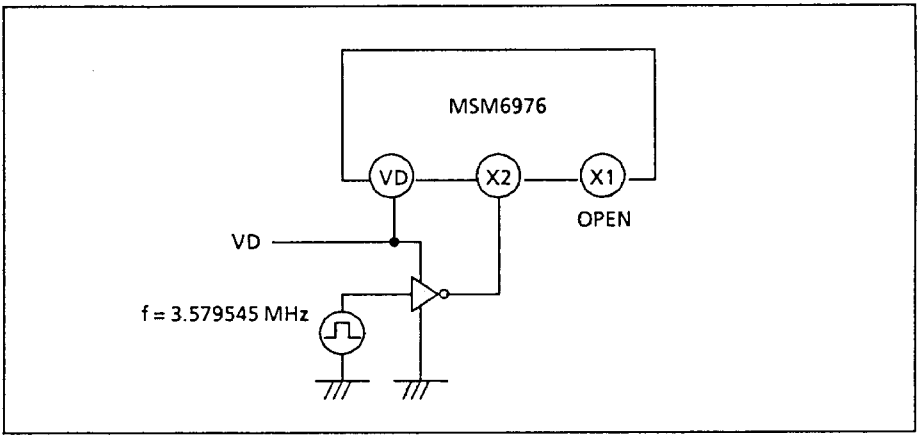
Attenuation (dB)	L1	L2	L4	L8
0	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0
10	1	0	1	0
11	0	0	1	0
12	1	1	0	0
13	0	1	0	0
14	1	0	0	0
15	0	0	0	0

0: Ground
1: Same potential as VD or open

3. Crystal Oscillator Connection

Connect the crystal oscillator and capacitors to the X1 and X2 pins as shown in Fig. 3. Place the crustal oscillator as close to the IC pins as possible.

To use an external clock in place of the crystal oscillator, connect it as shown below.



4. Power Supply and GND

Bypass capacitors to be connected between power supply pins (VA1, VA2, and VD) and the GND (AG1, AG2, and DG) shall be placed as close to the IC pins as possible.

To prevent the digital system noise from influencing the analog system, connect DG with AG1 and AG2 at a point near the system ground.

5. SG1 and SG2

Since the analog circuits in this IC are operated by a single 12V power supply (VA1 and VA2), DC bias circuits as the operating points of analog circuits are built in the IC. SG1 and SG2 are their output pins. To prevent the influence of the noise on the analog circuits, connect bypass capacitors near the IC pins.

APPLICATION EXAMPLE

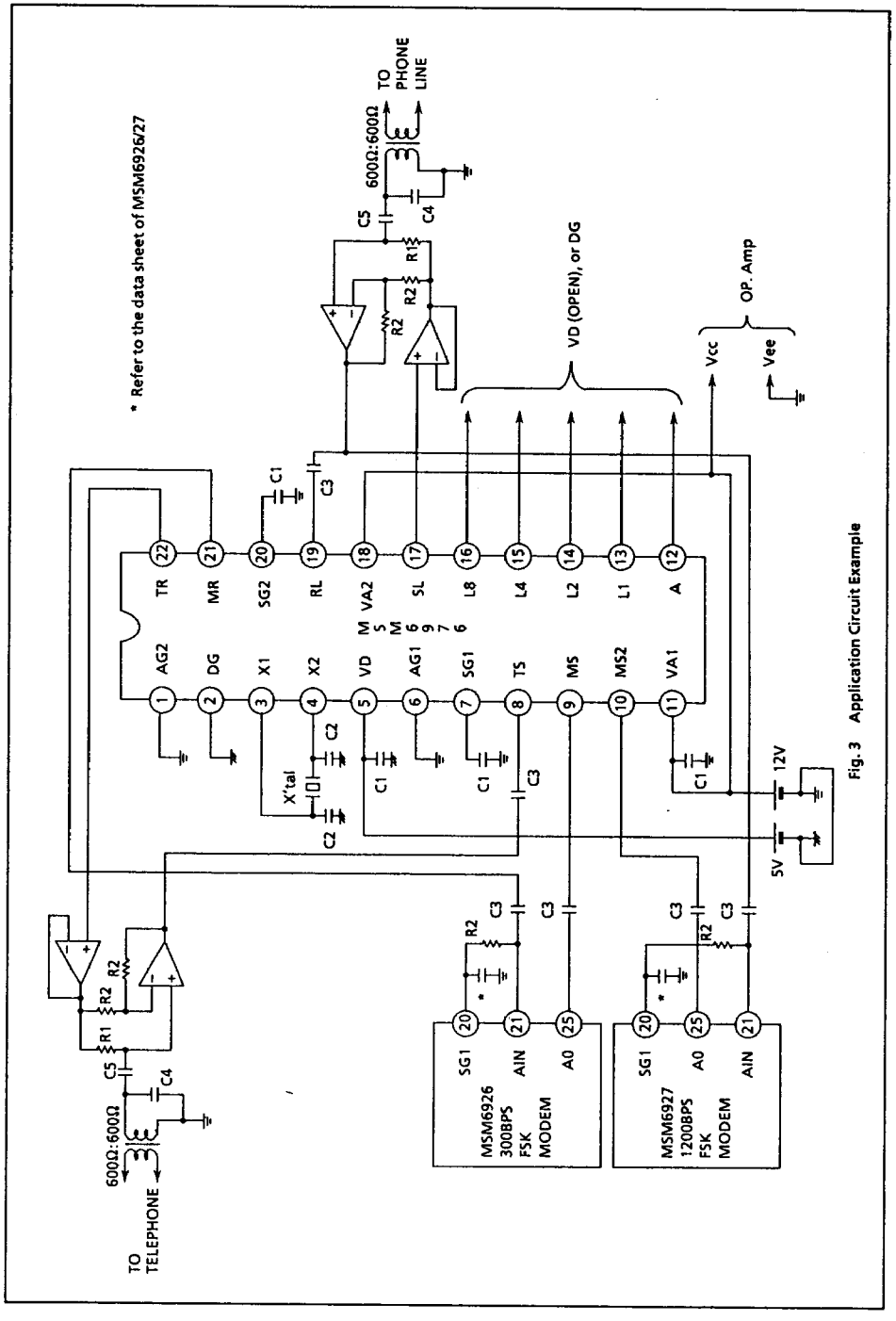


Fig. 3 Application Circuit Example