Single Channel Protector in an SOT-23 Package

ADG465

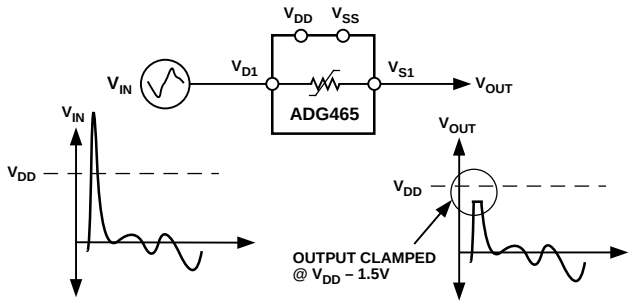
FEATURES

Fault and Overvoltage Protection up to ±40 V
Signal Paths Open Circuit with Power Off
Signal Path Resistance of R_{ON} with Power On
44 V Supply Maximum Ratings
Low On Resistance 80 Ω Typ
1 nA Max Path Current Leakage @ +25°C
Low Power Dissipation 0.8 μW Typ
Latchup-Proof Construction

APPLICATIONS

ATE Equipment
Sensitive Measurement Equipment
Hot-Insertion Rack Systems
ADC Input Channel Protection

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG465 is a single channel protector in an SOT-23 package. The channel protector is placed in series with the signal path, and will protect sensitive components from voltage transience in the signal path whether or not the power supplies are present. Because the channel protection works regardless of the presence of the supplies, the channel protectors are ideal for use in applications where correct power sequencing cannot always be guaranteed to protect analog inputs (e.g., hot-insertion rack systems). This is discussed further, and some example circuits are given, in the Applications section of this data sheet.

A channel protector consists of an n-channel MOSFET, a p-channel MOSFET and an n-channel MOSFET, connected in series. The channel protector behaves like a series resistor during normal operation, i.e., $(V_{SS} + 2\ V) < V_{IN} < (V_{DD} - 1.5\ V)$. When a channel's analog input exceeds the power supplies (including V_{DD} and V_{SS} = 0 V), one of the MOSFETs will switch off, clamping the output to either V_{SS} + 2 V or V_{DD} – 1.5 V. Circuitry and signal source protection is provided in the event of an overvoltage or power loss. The channel protectors can withstand overvoltage inputs from –40 V to +40 V. See the Circuit Information section of this data sheet.

The ADG465 can operate from both bipolar and unipolar supplies. The channels are normally on when power is connected, and open circuit when power is disconnected. With power supplies of ±15 V, the on-resistance of the ADG465 is 80 Ω typ, with a leakage current of ±1 nA max. When power is disconnected, the input leakage current is approximately ±5 nA typ.

The ADG465 is available in a 6-lead plastic surface mount SOT-23 package, and an 8-lead μSOIC package.

PRODUCT HIGHLIGHTS

1. Fault Protection.
   The ADG465 can withstand continuous voltage inputs from –40 V to +40 V. When a fault occurs due to the power supplies being turned off, or due to an overvoltage being applied to the ADG465, the output is clamped. When power is turned off, current is limited to the nanoampere level.
2. Low Power Dissipation.
3. Low R_{ON} 80 Ω typ.
4. Trench Isolation Latchup-Proof Construction.
   A dielectric trench separates the p- and n-channel MOSFETs thereby preventing latchup.

REV. A

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
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ADG465–SPECIFICATIONS

Dual Supply[1] (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, unless otherwise noted)

Parameter	+25°C	B	Units	Test Conditions/Comments
FAULT PROTECTED CHANNEL				
Fault-Free Analog Signal Range[2]		V_{SS} + 1.2	V min	Output Open Circuit
		V_{DD} – 0.8	V max	
R_{ON}	80		Ω typ	–10 V ≤ V_S ≤ +10 V, I_S = 1 mA
	95	115	Ω max	
ΔR_{ON}	4	5	Ω max	–5 V ≤ V_S ≤ +5 V
LEAKAGE CURRENTS				
Channel Output Leakage, $I_{S(ON)}$				V_S = V_D = ±10 V
(Without Fault Condition)	±0.1	±1	nA typ	
	±1	±5	nA max	
Channel Input Leakage, $I_{D(ON)}$				V_S = ±25 V
(With Fault Condition)	±0.2	±0.4	nA typ	V_D = Open Circuit
	±2	±5	nA max	
Channel Input Leakage, $I_{D(OFF)}$				V_{DD} = 0 V, V_{SS} = 0 V
(With Power Off and Fault)	±0.5	±2	nA typ	V_S = ±35 V
	±2	±10	nA max	V_D = Open Circuit
Channel Input Leakage, $I_{D(OFF)}$				V_{DD} = 0 V, V_{SS} = 0 V
(With Power Off and Output S/C)	±0.005	±0.1	µA typ	V_S = ±35 V, V_D = 0 V
	±0.015	±0.5	µA max	
POWER REQUIREMENTS				
I_{DD}	±0.05		µA typ	
	±0.5	±5	µA max	
I_{SS}	±0.05		µA typ	
	±0.5	±5	µA max	
V_{DD}/V_{SS}	0	0	V min	
	±20	±20	V max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . . +44 V
V_S, V_D, Analog Input Overvoltage with Power ON[2]
. . . . . V_{SS} – 20 V to V_{DD} + 20 V
V_S, V_D, Analog Input Overvoltage with Power OFF[2]
. . . . . –35 V to +35 V
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D . . . . . 40 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +125°C
Junction Temperature . . . . . +150°C
SOT-23 Package
θ_{JA}, Thermal Impedance . . . . . 230°C/W
µSOIC Package
θ_{JA}, Thermal Impedance . . . . . 205°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

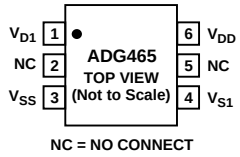
NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at S or D will be clamped by the channel protector, see Circuit Information section of the data sheet.

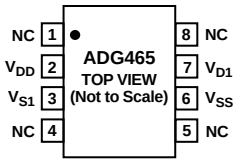
PIN CONFIGURATIONS

(RT-6)



NC = NO CONNECT

(RM-8)



NC = NO CONNECT

PIN FUNCTION DESCRIPTIONS

Pin RT-6	Pin RM-8	Pin Description
1	7	V_{D1}, this is one terminal of the channel protector. The channel protector is bidirectional so this terminal may be used as an input or an output.
2	1, 4	NC, this is a no connect pin.
3	6	V_{SS}, Negative Power Supply (0 V to –20 V). The clamping point for a negative overvoltage is also defined by V_{SS}, see Overvoltage Protection section.
4	3	V_{S1}, this is one terminal of the channel protector. The channel protector is bidirectional so this terminal may be used as an output or an input.
5	5, 8	NC, this is a no connect pin.
6	2	V_{DD}, Positive Power Supply (0 V to 20 V). The clamping point for a positive overvoltage is also defined by V_{DD}, see Overvoltage Protection section.

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Brand	Package Options
ADG465BRT	–40°C to +85°C	6-Lead Plastic Surface Mount SOT-23	S1B	RT-6
ADG465BRM	–40°C to +85°C	8-Lead µSOIC	S1B	RM-8

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG465 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADG465—Typical Performance Characteristics

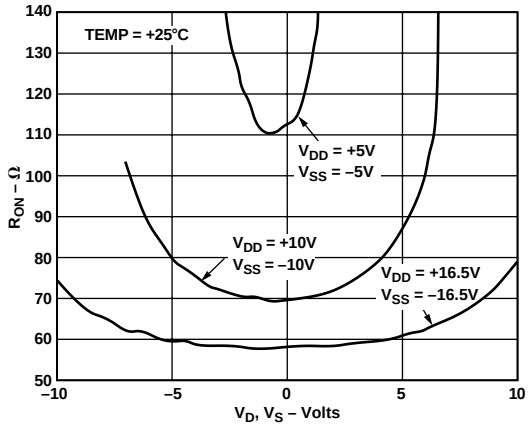


Figure 1. On Resistance as a Function of V_{DD} and V_D (Input Voltage)

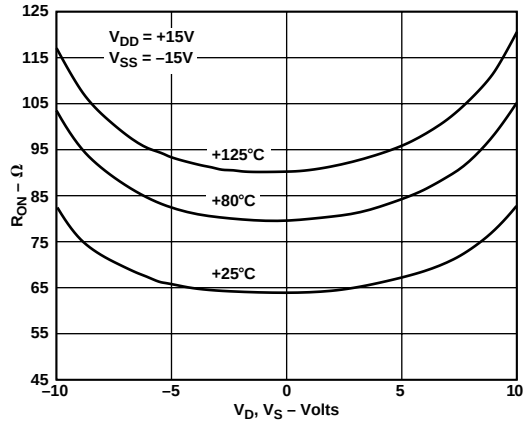


Figure 2. On Resistance as a Function of Temperature and V_D (Input Voltage)

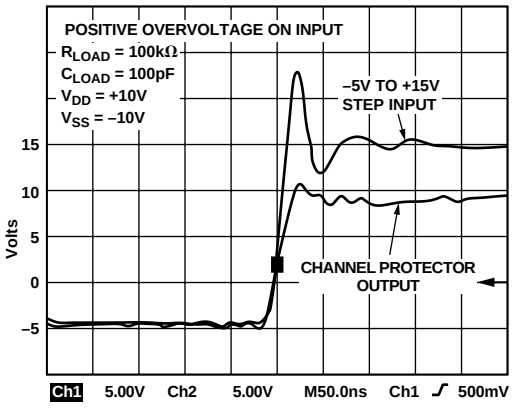


Figure 3. Positive Overvoltage Transience Response

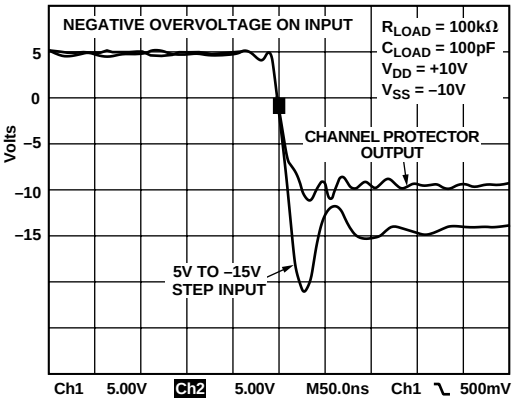


Figure 4. Negative Overvoltage Transience Response

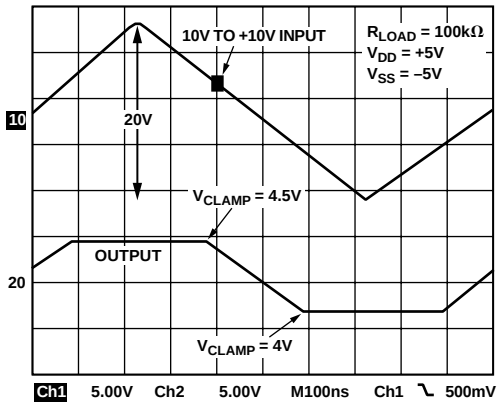


Figure 5. Overvoltage Ramp

CIRCUIT INFORMATION

Figure 6 below shows a simplified schematic of a channel protector circuit. The circuit is comprised of four MOS transistors—two NMOS and two PMOS. One of the PMOS devices does not lie directly in the signal path, but is used to connect the source of the second PMOS device to its backgate. This has the effect of lowering the threshold voltage and increasing the input signal range of the channel for normal operation. The source and backgate of the NMOS devices are connected for the same reason. During normal operation the channel protectors have a resistance of 80 Ω typ. The channel protectors are very low power devices; even under fault conditions the supply current is limited to sub-microampere levels. All transistors are dielectrically isolated from each other using a trench isolation method. This makes it impossible to latch up the channel protectors. For an explanation, see Trench Isolation section.

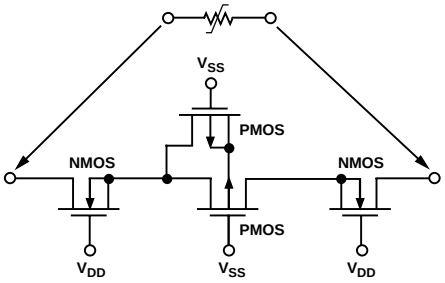


Figure 6. The Channel Protector Circuit

Overvoltage Protection

When a fault condition occurs on the input of a channel protector, the voltage on the input has exceeded some threshold voltage set by the supply rail voltages. The threshold voltages are related to the supply rails as follows: for a positive overvoltage, the threshold voltage is given by $V_{DD} - V_T$ where V_{TN} is the threshold voltage of the NMOS transistor (1.5 V typ). In the case of a negative overvoltage the threshold voltage is given by $V_{SS} - V_{TP}$ where V_{TP} is the threshold voltage of the PMOS device (2 V typ). If the input voltage exceeds these threshold voltages, the output of the channel protector (no load) is clamped at these threshold voltages. However, the channel protector output will clamp at a voltage inside these thresholds if the output is loaded. For example, with an output load of 1 kΩ, V_{DD} = 15 V and a positive overvoltage. The output will clamp at $V_{DD} - V_{TN} - \Delta V$ = 15 V – 1.5 V – 0.6 V = 12.9 V where ΔV is due to I. R voltage drops across the channels of the MOS devices (see Figure 8). As can be seen from Figure 8, the current during fault condition is determined by the load on the output (i.e., V_{CLAMP}/R_L). However, if the supplies are off, the fault current is limited to the nanoampere level.

Figures 7, 9 and 10 show the operating conditions of the signal path transistors during various fault conditions. Figure 7 shows how the channel protectors operate when a positive overvoltage is applied to the channel protector.

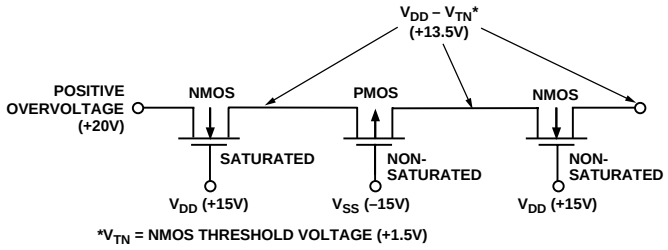


Figure 7. Positive Overvoltage on the Channel Protector

The first NMOS transistor goes into a saturated mode of operation as the voltage on its Drain exceeds the Gate voltage (V_{DD}) – the threshold voltage (V_{TN}). This situation is shown in Figure 8. The potential at the source of the NMOS device is equal to $V_{DD} - V_{TN}$. The other MOS devices are in a nonsaturated mode of operation.

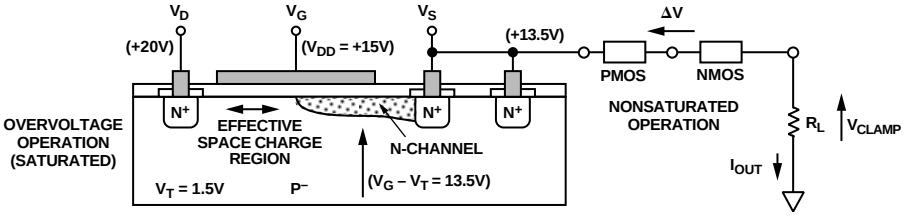


Figure 8. Positive Overvoltage Operation on the Channel Protector

When a negative overvoltage is applied to the channel protector circuit, the PMOS transistor enters a saturated mode of operation as the drain voltage exceeds $V_{SS} - V_{TP}$. See Figure 9 below. As in the case of the positive overvoltage, the other MOS devices are nonsaturated.

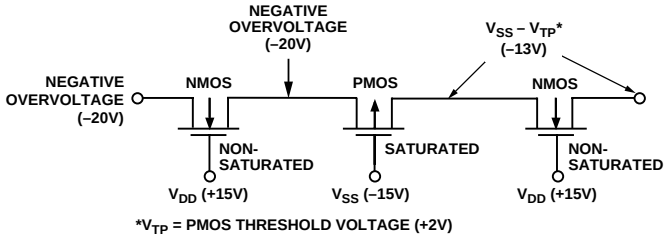


Figure 9. Negative Overvoltage on the Channel Protector

The channel protector is also functional when the supply rails are down (e.g., power failure) or momentarily unconnected (e.g., rack system). This is where the channel protector has an advantage over more conventional protection methods such as diode clamping (see Applications Information). When V_{DD} and V_{SS} equal 0 V, all transistors are off and the current is limited to microampere levels (see Figure 10).

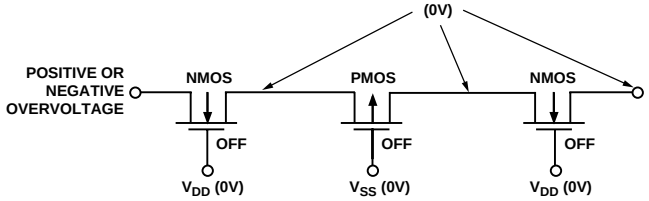


Figure 10. Channel Protector Supplies Equal to Zero Volts

TRENCH ISOLATION

The MOS devices that make up the channel protector are isolated from each other by an oxide layer (trench) (see Figure 11). When the NMOS and PMOS devices are not electrically isolated from each other, there exists the possibility of "latchup" caused by parasitic junctions between CMOS transistors. Latchup is caused when P-N junctions that are normally reverse biased, become forward biased, causing large currents to flow. This can be destructive.

CMOS devices are normally isolated from each other by *Junction Isolation*. In Junction Isolation, the *N* and *P* wells of the CMOS transistors form a diode that is reverse biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A Silicon-Controlled Rectifier (SCR) type circuit is formed by the two transistors, causing a significant amplification of the current that, in turn, leads to latchup. With Trench Isolation, this diode is removed; the result is a latchup-proof circuit.

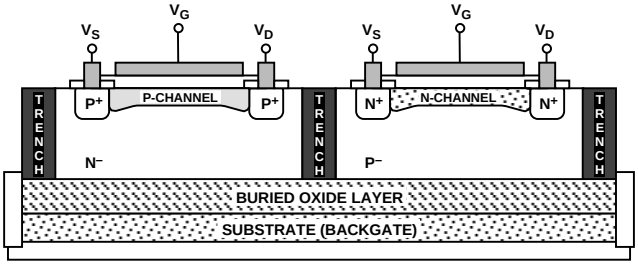


Figure 11. Trench Isolation

APPLICATIONS INFORMATION

Overvoltage and Power Supply Sequencing Protection

The ADG465 is ideal for use in applications where input overvoltage protection is required and correct power supply sequencing cannot always be guaranteed. The overvoltage protection ensures that the output voltage of the channel protector will not exceed the threshold voltages set by the supplies (see Circuit Information section) when there is an overvoltage on the input. When the input voltage does not exceed these threshold voltages, the channel protector behaves like a series resistor (80 Ω typ). The resistance of the channel protector does vary slightly with operating conditions (see Typical Performance Graphs).

The power sequencing protection is afforded by the fact that when the supplies to the channel protector are not connected, the channel protector becomes a high resistance device. Under this condition all transistors in the channel protector are off and the only currents that flow are leakage currents, which are at the μA level.

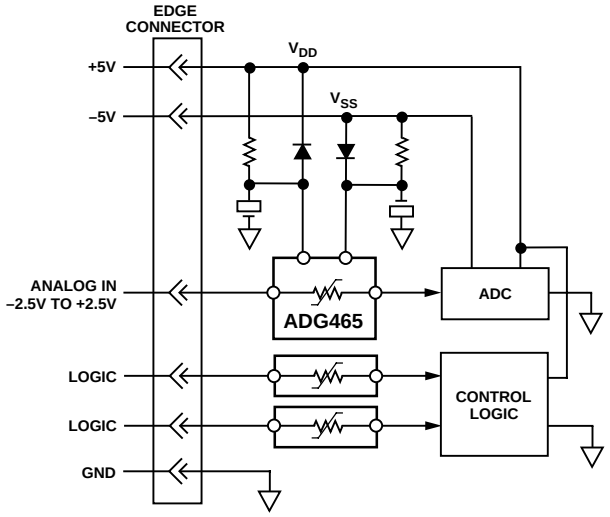


Figure 12. Overvoltage and Power Supply Sequencing Protection

Figure 12 shows a typical application requiring overvoltage and power supply sequencing protection. The application shows a Hot-Insertion rack system. This involves plugging a circuit board or module into a live rack via an edge connector. In this type of application it is not possible to guarantee correct power supply sequencing. Correct power supply sequencing means that the power supplies should be connected prior to any external signals. Incorrect power sequencing can cause a CMOS device to "latch up," see Trench Isolation section. This is true of most CMOS devices, regardless of the functionality. RC networks are used on the supplies of the channel protector (Figure 12) to ensure that the rest of the circuitry is powered up before the channel protectors. In this way, the outputs of the channel protectors are clamped well below V_{DD} and V_{SS} until the capacitors are charged. The diodes ensure that the supplies on the channel protector never exceed the supply rails of the board when it is being disconnected. Again, this ensures that signals on the inputs of the CMOS devices never exceed the supplies.

High Voltage Surge Suppression

The ADG465 are not intended for use in high voltage applications such as surge suppression. The ADG465 has breakdown voltages of V_{SS} – 20 V and V_{DD} + 20 V on the inputs when the power supplies are connected. When the power supplies are disconnected, the breakdown voltages on the input of the channel protector are ±35 V. In applications where inputs are likely to be subject to overvoltages exceeding the breakdown voltages quoted for the channel protectors, transient voltage suppressors (TVSs) should be used. These devices are commonly used to protect vulnerable circuits from electric overstress such as that caused by electrostatic discharge, inductive load switching and induced lightning. However, TVSs can have a substantial standby (leakage) current (300 μA typ) at the reverse standoff voltage. The reverse standoff voltage of a TVS is the normal peak operating voltage of the circuit. In addition, TVSs offer no protection against latchup of sensitive CMOS devices when the power supplies are off. To provide the best leakage current specification and circuit protection, the best solution is to use a channel protector in conjunction with a TVS.

Figure 13 shows an input protection scheme that uses both a TVS and channel protector. The TVS is selected with a reverse standoff voltage much greater than the operating voltage of the circuit (TVSs with higher breakdown voltages tend to have better standby leakage current specifications), but inside the breakdown voltage of the channel protector. This circuit protects the circuitry whether or not the power supplies are present.

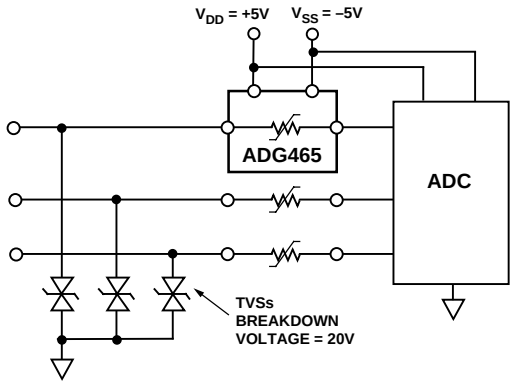
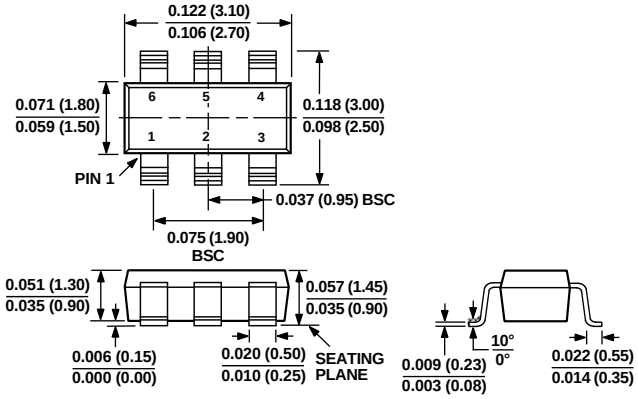


Figure 13. High Voltage Protection

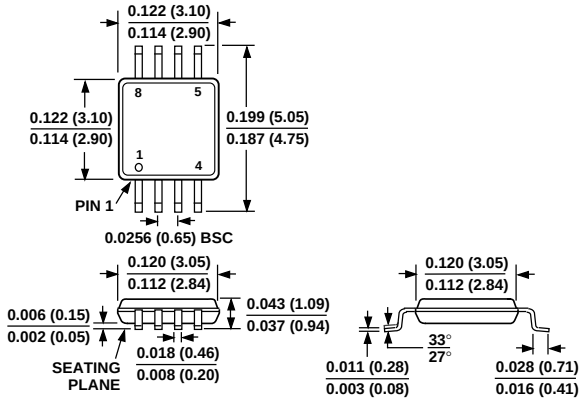
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

6-Lead Plastic Surface Mount SOT-23 Package (RT-6)



8-Lead μSOIC (RM-8)



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