Non-Linear High Speed Termination IC

Features

- 16 channel, dual rail clamping action in a single package
- Provides bus termination independent of line impedance or loading conditions
- Uses CAMD's patented EZterm™ technology
- 24-pin QSOP package saves board space and eases layout in space critical areas.
- One IC replaces and outperforms up to 32 discrete components.
- Enable pin included

Application

- High speed, low voltage buses

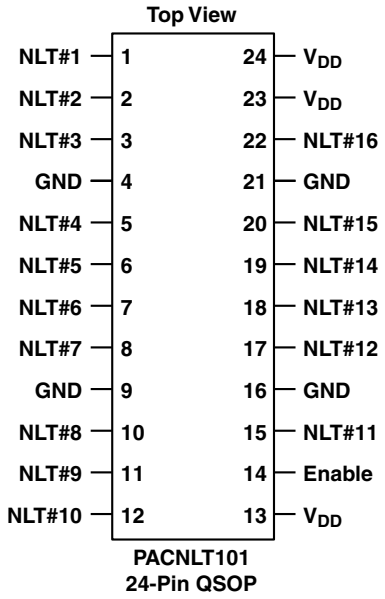
Product Description

CAMD's non-linear termination IC is specifically designed to minimize overshoot/undershoot disturbances caused by impedance mismatch reflections and noise on high-speed transmission lines.

Reflections on high-speed data lines lead to voltage overshoot and undershoot disturbances, which may result in data loss or improper system operation. Resistive terminations, when used to terminate these high-speed data lines, increase power consumption and degrade output levels, resulting in reduced noise immunity. Clamping-type termination is the best overall solution for applications in which these may be considerations.

This highly integrated non-linear termination IC provides very effective termination performance for high-speed data lines under variable loading conditions. The device supports up to 16 terminated lines per package – each of which are clamped to both ground and power supply rail. A typical application may use 4 devices to replace (and outperform) 64 conventional Schottky diode pairs; thus providing significant reductions in component and assembly costs, improvements in manufacturing efficiency and reliability, and savings in allocated board area for space-critical designs.

Pin Configuration



Standard Part Ordering Information

Package		Ordering Part Number	
Pin	Style	Tape & Reel	Part Marking
24	QSOP	PACNLT101Q	PACNLT101Q

C1601100

Absolute Maximum Ratings		
Parameter	**Rating**	**Unit**
Maximum DC Voltage on any pin	3.6	V
Minimum DC Voltage on any pin	–0.5	V
Continuous current per channel	72	mA
Operating Temperature (Ambient)	–40 to 85	°C
Storage Temperature (Ambient)	–65 to 150	°C
Power Dissipation @ T = 25°C	0.9	W

Operating Characteristics - V_{DD} = 3.3V, Enable = 3.3V, Temperature = –40°C to 85°C

Operating Characteristics — 3.3V					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Signal Voltage	above V_{DD} @ I = 50mA		610	850	mV
	below GND @ I = –50mA		510	750	mV
V_{DD} current	all Channels floating		85	150	mA
Enable pin (pin 14) current	all Channels floating		10	15	mA
Input Capacitance*	Signal voltage = V_{DD}		3.4		pF
	Signal voltage = $V_{DD/2}$		3.0		pF
ESD protection	MIL-STD-883, method 3015*	4			kV
Response Time				400	ps

*These parameters are guaranteed by design and characterization.

Operating Characteristics - V_{DD} = 2V, Enable = 2V, Temperature = –40°C to 85°C

Operating Characteristics — 2.0V					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Signal Voltage	above V_{DD} @ I = 20mA		390	600	mV
	below GND @ I = –20mA		300	500	mV
V_{DD} current	all Channels floating		25	42	mA
Enable pin (pin 14) current	all Channels floating		3.5	5.5	mA
Input Capacitance*	Signal voltage = V_{DD}		3.5		pF
	Signal voltage = $V_{DD/2}$		3.2		pF
ESD protection	MIL-STD-883, method 3015*	4			kV
Response Time				400	ps

*These parameters are guaranteed by design and characterization.

Operating Characteristics - V_{DD} = 2.5V, Enable = 2.5V, Temperature = 27°C

Operating Characteristics — 2.5V					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Signal Voltage	above V_{DD} @ I = 30mA		470		mV
	below GND @ I = –30mA		375		mV
V_{DD} current	all Channels floating		50		mA
Enable pin current	all Channels floating		6		mA

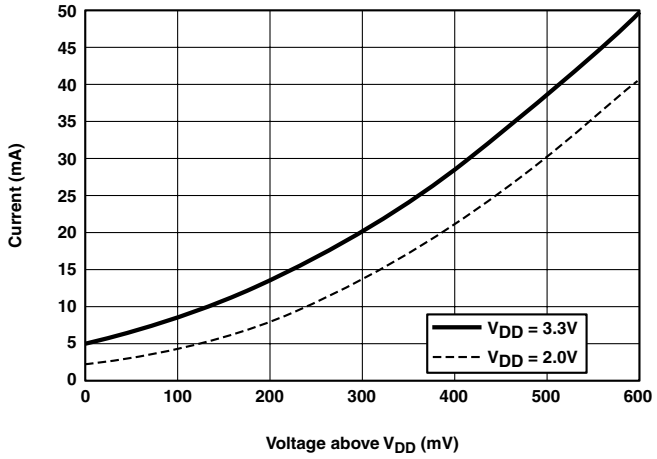


Figure 1. DC I-V Curves for V_{DD} = 2V and V_{DD} = 3.3V

Application Information

Figure 2 shows one method of configuring the printed circuit board such that all 16 terminated signals are easily accessible. The decoupling capacitor should be a high-frequency type, 0.1µF or larger, and placed as close to the IC as possible. This will minimize the positive overshoot voltage and also reduce EMI emissions. It should be noted that for optimum performance the PACNLT101 termination should be located as physically close to the receiving IC input as is possible.

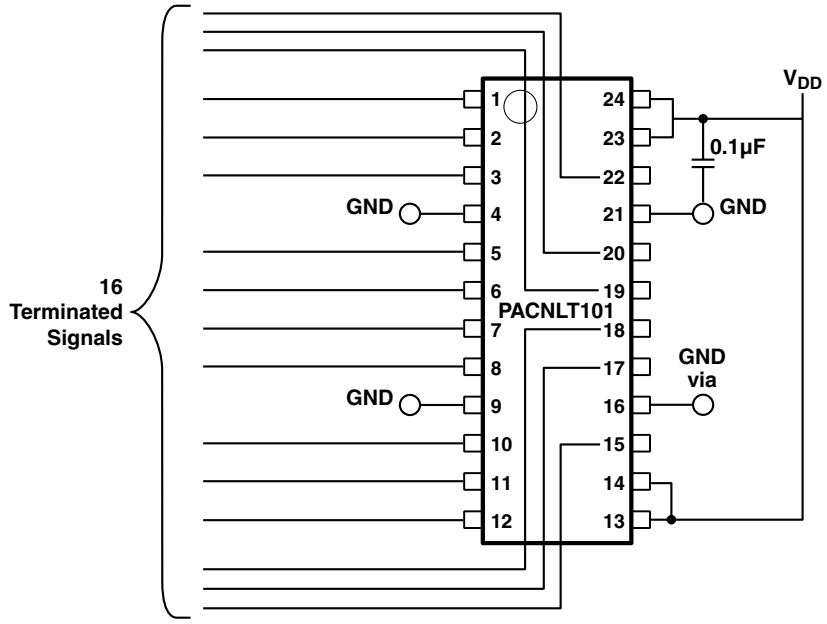


Figure 2. Printed Circuit Board with Accessible Configuration for 16 Terminated Signals

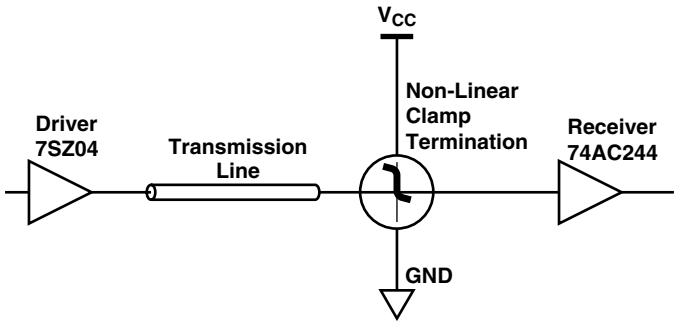


Figure 3. Example Circuit: Single-Driver/Single Receiver

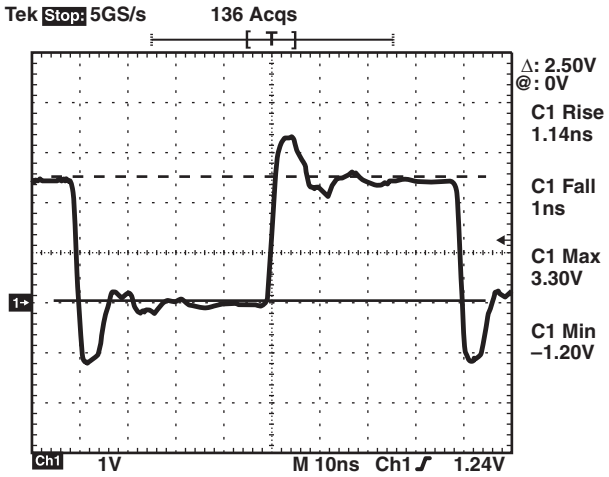


Figure 4. 74AC244 Termination Only

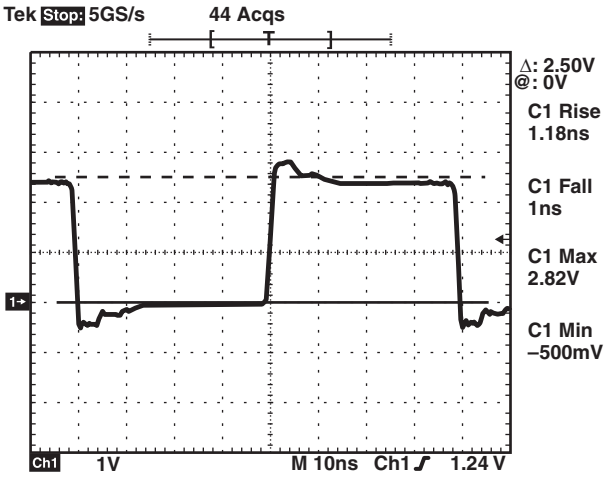


Figure 5. With PACNLT101 Termination

Enable pin

In normal use the Enable pin is connected to V_{DD}.

If the Enable pin is set to 0V or disconnected (high impedance), then the PACNLT101 will be disabled. The supply current will drop to almost zero and the clamping performance will be worsened.

The Enable pin can also be used to vary the supply current and clamping voltage. As the current into the Enable pin is increased the supply current will increase and the clamping voltage will be reduced. The minimum clamping voltage will occur when the Enable pin voltage equals the supply voltage. (The Enable pin voltage cannot exceed the supply voltage.)

Users who cannot tolerate the supply current quoted in the Operating Characteristics can connect a resistor in series with the Enable pin to reduce the supply current, at the cost of increasing the clamping voltage. See Figure 6.

The controller IC sets the powerdown pin to 0V to powerdown the PACNLT101, and sets the powerdown pin to V_{DD} to power up the PACNLT101. The system designer can vary the value of R1 to optimize the trade-off between power consumption and clamping voltage. See Figure 7, 8, 9, and 10.

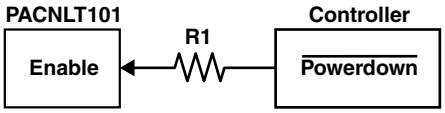


Figure 6. Resistor In Series with the Enable Pin

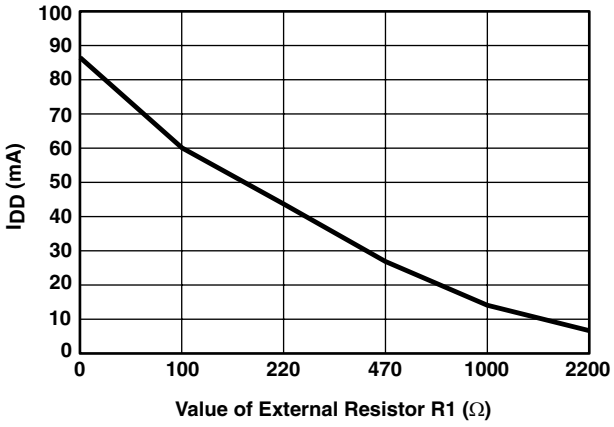


Figure 7. I_{DD} vs R1 @ V_{DD} = 3.3V

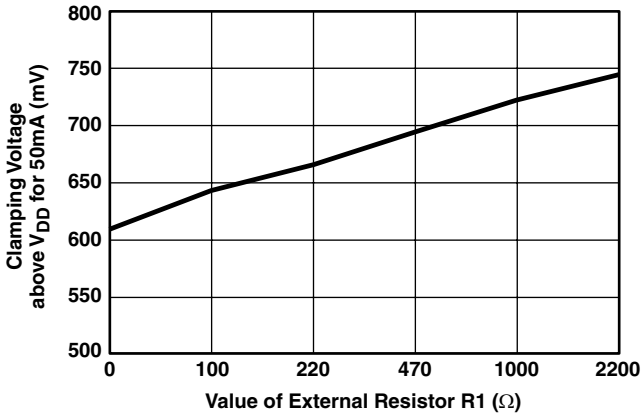


Figure 8. Clamping Voltage vs R1 @ V_{DD} = 3.3V

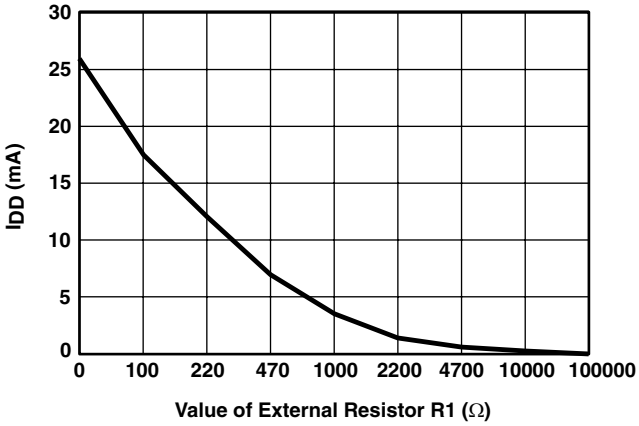


Figure 9. I_{DD} vs R1 @ V_{DD} = 2V

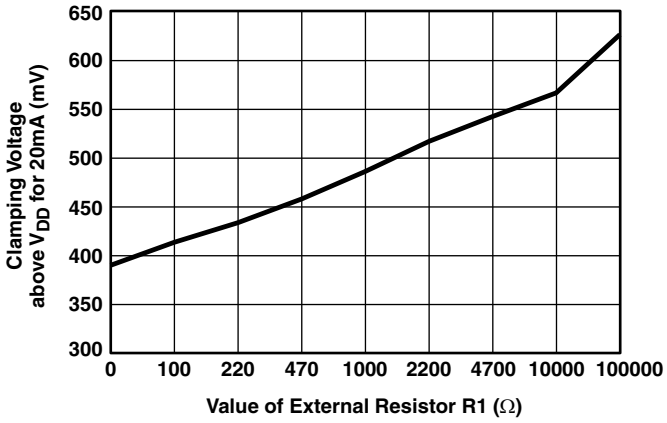


Figure 10. Clamping Voltage vs R1 @ V_{DD} = 2V