

# M5M5279P, J-20, -25, -35, -25L, -35L

294912-BIT (32768-WORD BY 9-BIT) CMOS STATIC RAM

## DESCRIPTION

The M5M5279 is a family of 32768-word by 9-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

## FEATURES

- Fast access time
  - M5M5279P, J-20 ..... 20ns(max)
  - M5M5279P, J-25, -25L ..... 25ns(max)
  - M5M5279P, J-35, -35L ..... 35ns(max)
- Low power dissipation
  - Active ..... 300mW(typ)
  - Stand by(-20, -25, -35) ..... 5mW(typ)
  - Stand by(-25L, -35L) ..... 50  $\mu$ W(typ)
- Power down by  $\overline{S_1}$
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ( $\overline{S_1}$ ,  $S_2$ ) input
- Output enable ( $\overline{OE}$ ) prevents data contention in the I/O bus
- All address inputs are changeable with each other

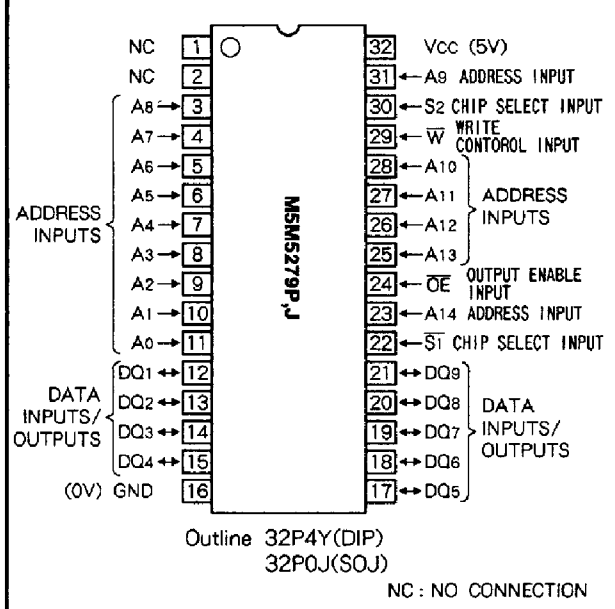
## APPLICATION

High-speed memory systems

## FUNCTION

A write operation is executed during the  $\overline{S_1}$  low,  $S_2$  high, and  $\overline{W}$  low overlap time. In this period, address signals must be stable. When  $\overline{W}$  is low, the DQ terminal is maintained in the high impedance state.

## PIN CONFIGURATION (TOP VIEW)

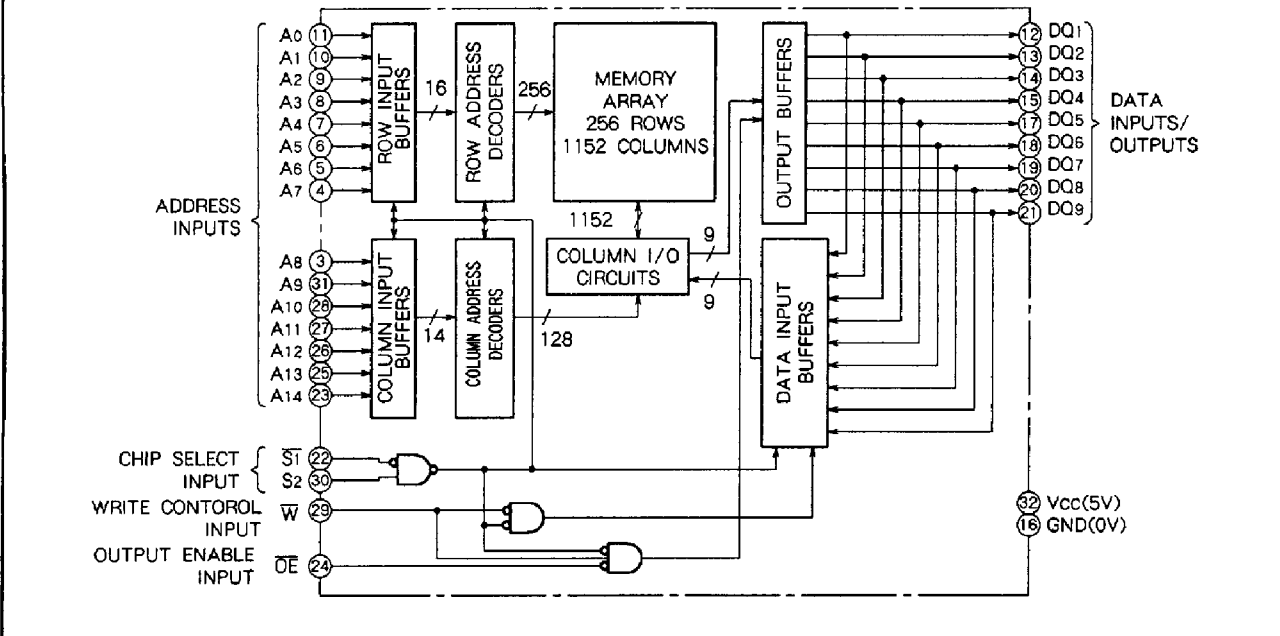


In a read operation, after setting  $\overline{W}$  to high,  $\overline{S_1}$  to low  $S_2$  high and  $\overline{OE}$  to low if the address signals are stable, the data is available at the DQ terminal.

When  $\overline{S_1}$  is high, or  $S_2$  is low, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal  $\overline{S_1}$  controls the power-down feature. When  $\overline{S_1}$  goes high, power dissipation is reduced extremely. The access time from  $\overline{S_1}$  is equivalent to the address access time.

## BLOCK DIAGRAM



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### MODE SELECTION

S <sub>1</sub>	S <sub>2</sub>	W	OE	Mode	Data input/output	I <sub>cc</sub>
H	X	X	X	Non selection	High-impedance	Stand by
L	L	X	X	Non selection	High-impedance	Active
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

H: V<sub>IH</sub> L: V<sub>IL</sub> X: V<sub>IH</sub> or V<sub>IL</sub>

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Supply voltage	With respect to GND	-3.5*~7	V
V <sub>i</sub>	Input voltage		-3.5*~7	V
V <sub>o</sub>	Output voltage		-3.5*~7	V
P <sub>d</sub>	Maximum power dissipation		1	W
T <sub>opr</sub>	Operating temperature		0~70	°C
T <sub>stg(bias)</sub>	Storage temperature (bias)		-10~85	°C
T <sub>stg</sub>	Storage temperature		-65~150	°C

\* Pulse width ≤ 20ns, In case of DC: -0.5V

### DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0~70°C, V<sub>cc</sub> = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High-level input voltage		2.2		V <sub>cc</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage		-0.5*		0.8	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -4mA	2.4			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 8mA			0.4	V
I <sub>i</sub>	Input current	V <sub>i</sub> = 0~V <sub>cc</sub>			2	μA
I <sub>oz</sub>	Off-state output current	V <sub>i(s)</sub> = V <sub>IH</sub> , V <sub>o</sub> = 0~V <sub>cc</sub>			10	μA
I <sub>cc1</sub>	Supply current from V <sub>cc</sub>	V <sub>i(s)</sub> = V <sub>IL</sub> Output open	AC(20ns cycle)		140	mA
			AC(25ns cycle)		130	
			AC(35ns cycle)		120	
			DC	75	100	
I <sub>cc2</sub>	Stand by current	V <sub>i(s)</sub> = V <sub>IH</sub>	AC(20, 25, 35ns cycle)		40	mA
			Other V <sub>i</sub> ≥ V <sub>IH</sub> or ≤ V <sub>IL</sub>		30	
I <sub>cc3</sub>	Stand by current	V <sub>i(s)</sub> = V <sub>cc</sub> - 0.2V Other V <sub>i</sub> ≤ 0.2V or V <sub>i</sub> ≥ V <sub>cc</sub> - 0.2V	-20, -25, -35	1	10	mA
			-25L, -35L	10	100	

Note 1. Current flow into an IC is positive, out is negative. \* -3.0V in case of AC(Pulse width ≤ 20ns)

### CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>i</sub>	Input capacitance	V <sub>i</sub> = GND, V <sub>i</sub> = 25mVrms, f = 1MHz			5	pF
C <sub>o</sub>	Output capacitance	V <sub>o</sub> = GND, V <sub>o</sub> = 25mVrms, f = 1MHz			7	pF

### AC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0~70°C, V<sub>cc</sub> = 5V ± 10%, unless otherwise noted)

#### (1) MEASUREMENT CONDITIONS

Input pulse levels ..... V<sub>IH</sub> = 3V, V<sub>IL</sub> = 0V  
 Input rise and fall time ..... 3ns  
 Input timing reference levels ..... V<sub>IH</sub> = 2.4V, V<sub>IL</sub> = 0.6V  
 Output timing reference levels ..... V<sub>OH</sub> = 2.0V, V<sub>OL</sub> = 0.8V  
 Output loads ..... Fig.1, Fig.2

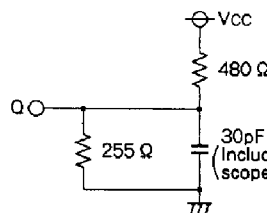


Fig.1 Output load

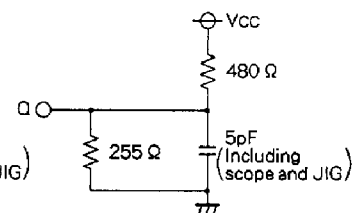


Fig.2 Output load for t<sub>en</sub>, t<sub>ds</sub>

# M5M5279P, J-20, -25, -35, -25L, -35L

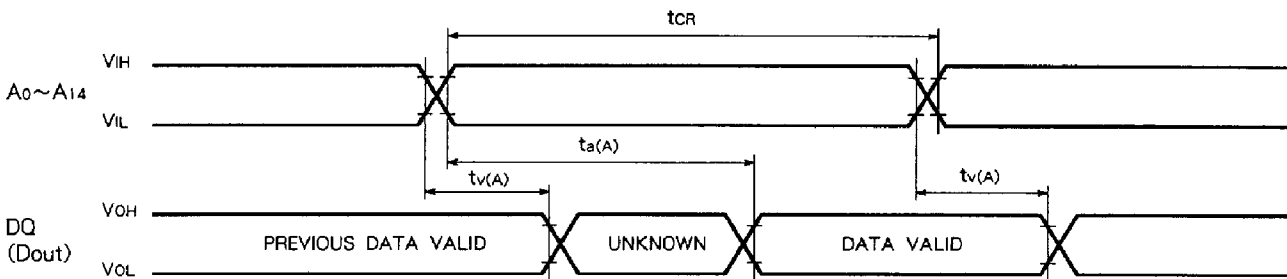
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## (2) READ CYCLE

Symbol	Parameter	Limits						Unit
		M5M5279-20		M5M5279-25, -25L		M5M5279-35, -35L		
		Min	Max	Min	Max	Min	Max	
t <sub>CR</sub>	Read cycle time	20		25		35		ns
t <sub>a(A)</sub>	Address access time		20		25		35	ns
t <sub>a(S1)</sub>	Chip select 1 access time		20		25		35	ns
t <sub>a(S2)</sub>	Chip select 2 access time		17		22		27	ns
t <sub>a(OE)</sub>	Output enable access time		10		12		15	ns
t <sub>v(A)</sub>	Data valid time after address change	3		5		5		ns
t <sub>en(S1)</sub>	Output enable time after $\overline{S1}$ low	3		5		5		ns
t <sub>en(S2)</sub>	Output enable time after S <sub>2</sub> high	0		0		0		ns
t <sub>en(OE)</sub>	Output enable time after $\overline{OE}$ low	0		0		0		ns
t <sub>dis(S1)</sub>	Output disable time after $\overline{S1}$ high	0	8	0	10	0	10	ns
t <sub>dis(S2)</sub>	Output disable time after S <sub>2</sub> low	0	8	0	10	0	10	ns
t <sub>dis(OE)</sub>	Output disable time after $\overline{OE}$ high	0	8	0	10	0	10	ns
t <sub>PU</sub>	Power-up time after chip selection	0		0		0		ns
t <sub>PD</sub>	Power-down time after chip selection		20		25		35	ns

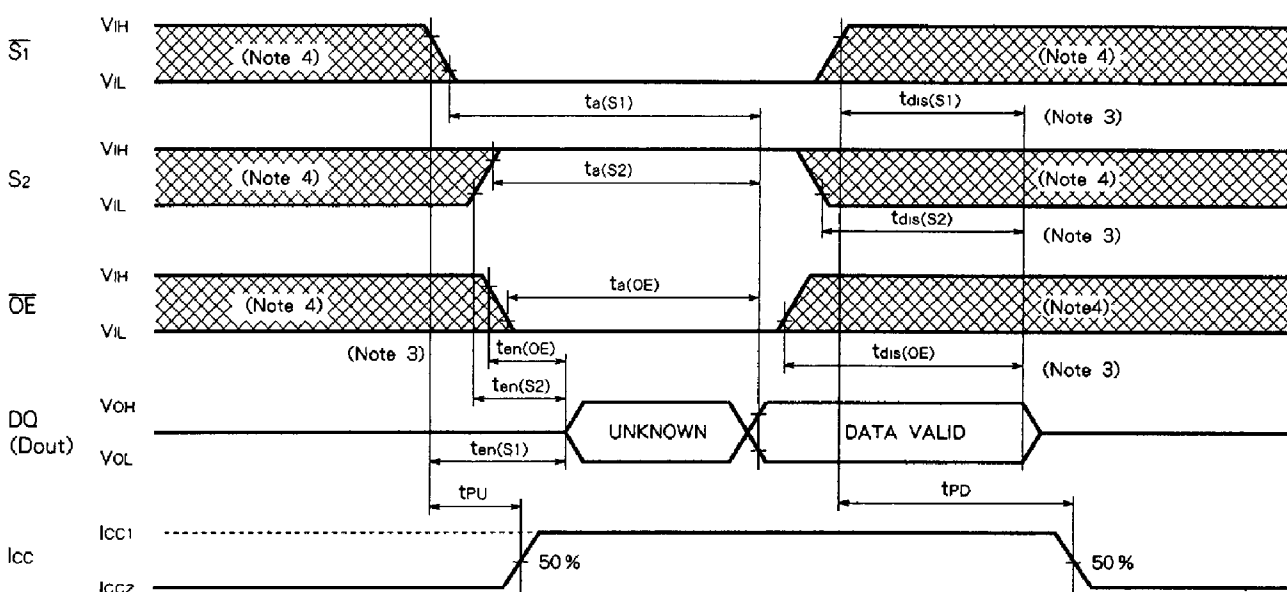
## (3) TIMING DIAGRAMS FOR READ CYCLE

### Read cycle 1



$\overline{W} = H$   $\overline{S1} = L$   $S2 = H$   $\overline{OE} = L$

### Read cycle 2 (Note 2)



Note 2. Addresses valid prior to or coincident with  $\overline{S1}$  transition low.

3. Transition is measured  $\pm 500$ mV from steady state voltage with specified loading in Figure 2.

4. Hatching indicates the state is don't care.

# M5M5279P, J-20, -25, -35, -25L, -35L

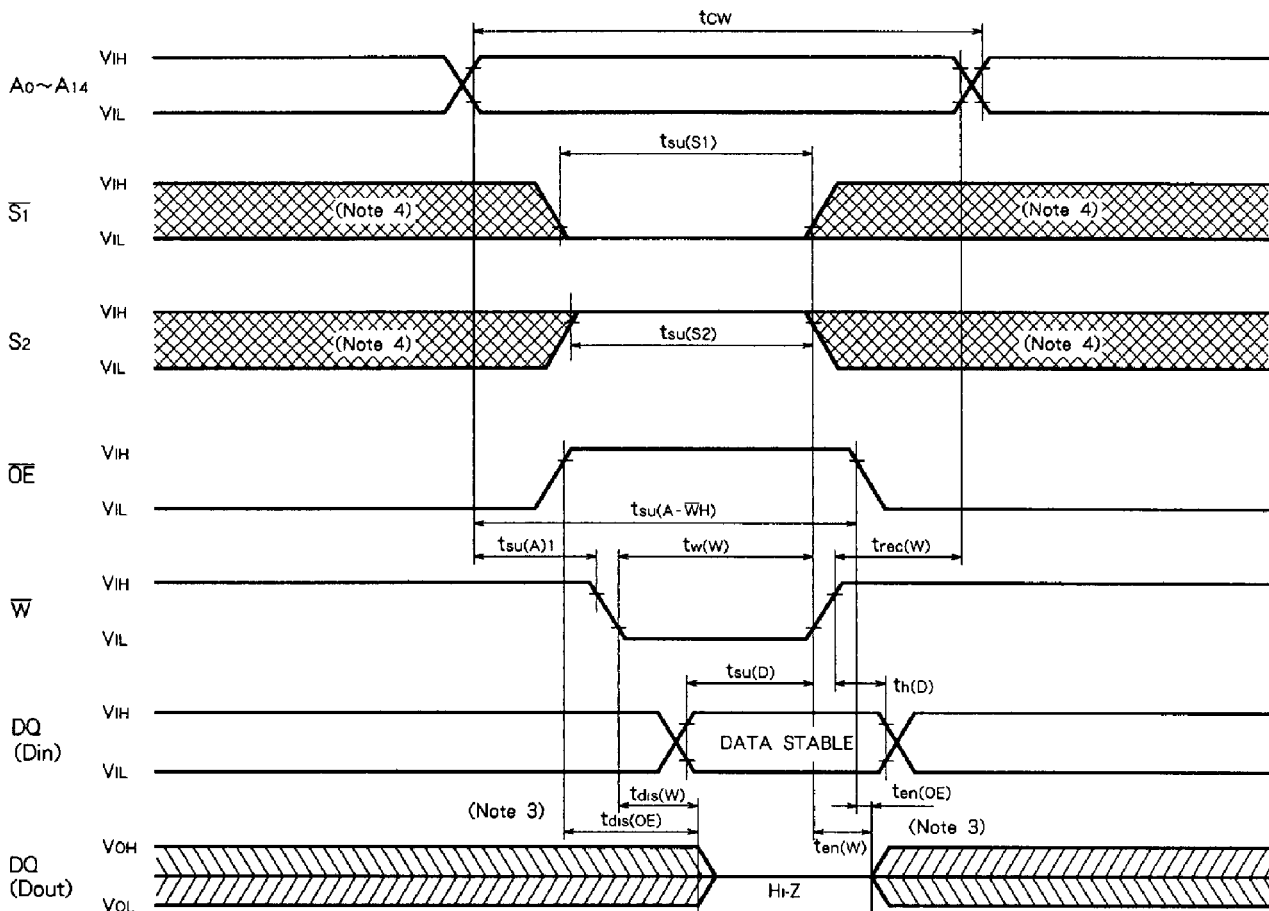
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## (4) WRITE CYCLE

Symbol	Parameter	Limits						Unit
		M5M5279-20		M5M5279-25, -25L		M5M5279-35, -35L		
		Min	Max	Min	Max	Min	Max	
t <sub>cw</sub>	Write cycle time	20		25		35		ns
t <sub>su(S1)</sub>	Chip select 1 setup time	15		20		30		ns
t <sub>su(S2)</sub>	Chip select 2 setup time	15		20		30		ns
t <sub>su(A)1</sub>	Address setup time( $\bar{W}$ )	0		0		0		ns
t <sub>su(A)2</sub>	Address setup time(S <sub>1</sub> , S <sub>2</sub> )	0		0		0		ns
t <sub>w(W)</sub>	Write pulse width	15		20		25		ns
t <sub>rec(W)</sub>	Write recovery time	0		0		0		ns
t <sub>su(D)</sub>	Data setup time	8		10		15		ns
t <sub>h(D)</sub>	Data hold time	0		0		0		ns
t <sub>dis(W)</sub>	Output disable time after $\bar{W}$ low	0	8	0	10	0	10	ns
t <sub>dis(OE)</sub>	Output disable time after $\bar{OE}$ high	0	8	0	10	0	10	ns
t <sub>en(W)</sub>	Output enable time after $\bar{W}$ high	0		0		0		ns
t <sub>en(OE)</sub>	Output enable time after $\bar{OE}$ low	0		0		0		ns
t <sub>au(A-<math>\bar{W}</math>)</sub>	Address to $\bar{W}$ high	15		20		30		ns

## (5) TIMING DIAGRAMS FOR WRITE CYCLE

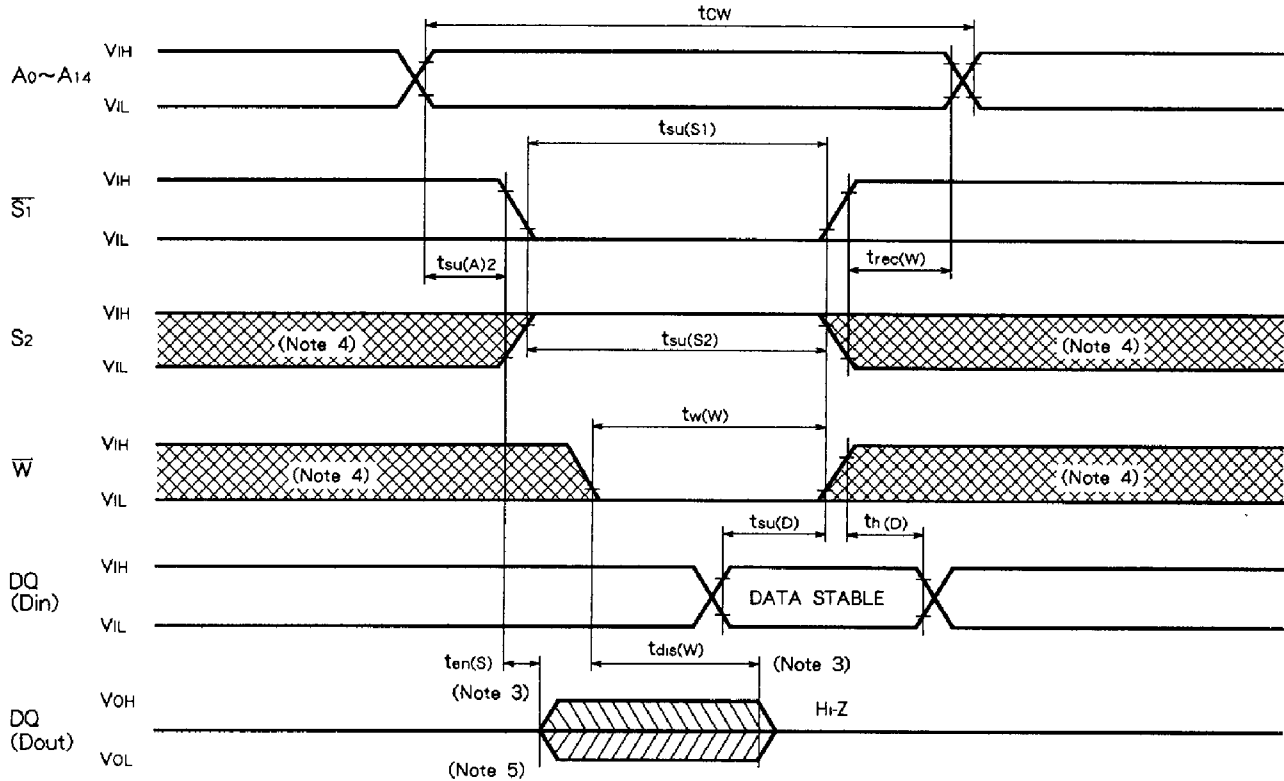
### Write cycle 1 ( $\bar{W}$ control mode)



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### Write cycle 2 ( $\overline{S1}$ , $S2$ control mode)



Note 5 When the falling edge of  $\overline{W}$  is simultaneous or prior to the falling edge of  $\overline{S1}$   $S2$ , the output is maintained in the high impedance.

### POWER DOWN CHARACTERISTICS ( $T_a = 0 \sim 70^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_i(S)$	Chip select input voltage	$V_i(S) \geq V_{CC} - 0.2V$	$V_{CC} - 0.2$			V
$t_{su(PD)}$	Power down setup time	$V_i \geq V_{CC} - 0.2V$ or $0V \leq V_i \leq 0.2V$	0			ns
$t_{rec(PD)}$	Power down recovery time		-25L	25		ns
			-35L	35		
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3.0V$			50	$\mu A$
		$V_{CC} = 5.5V$			100	

Note 6. This is only M5M5279P, J-25L, -35L

### TIMING WAVEFORM FOR POWER DOWN

