10-Port Gigabit Ethernet Controller

FEATURES

- Ten port full-duplex Gigabit Ethernet Controller with an industry standard POS-PHY Level 4™ system interface.
- Provides direct connection to optics.
- Incorporates ten SERDES, compliant with the IEEE 802.3 1998 PMA physical layer specification.
- Provides ten standard IEEE 802.3 Gigabit Ethernet MACs for frame verification.
- Provides on-chip data recovery and clock synthesis.
- Provides eight unicast exact-match address filters to filter frames based on DA, DA/VID, SA, or SA/VID.
- Each address filter can indicate whether to accept or discard based on a match.
- Provides 64-group multicast address filter.
- Internal 64 kbyte Tx and 224 kbyte Rx FIFOs per channel provisionable in quantities of 1 kbyte to accommodate system latencies.
- SATURN® compatible interface for Packet-Over-SONET Physical Layer and Link Layer devices Level 4 (POS-PHY Level 4 system interface).
- Line side loopback for system level diagnostic capability.
- 16 bit generic microprocessor interface for device initialization, control, register and per port statistics access.

GIGABIT ETHERNET MAC

- Verifies frame integrity (FCS and length checks).
- Errored frames can be filtered or passed to a higher layer device.
- Automatic Base Page Autonegotiation, extended Autonegotiation (Next Page) supported via host.
- Egress Ethernet frame encapsulation (pad to minimum size, add preamble, IFG and CRC generation).
- Supports Ethernet 2.0, IEEE 802.3 LLC and IEEE 802.3 SNAP/LLC encoding formats, and VLAN tagged frames.
- Minimum frame size 64 bytes.
- Supports jumbo frames up to 9.6 kbytes.
- Supports big endian data formats.
- Programmable inter-packet gap (IPG).
- Loopback for diagnostic capability through GMAC.

FLOW CONTROL

- Option to support IEEE 802.3-1998 flow control at each Ethernet port.
- Programmable watermarks for full/empty/starving FIFO conditions.
- Automatic generation of pause frames based on FIFO fill levels.
- Upper layer device can flow control Ethernet ports using side-band or host signaling to cause generation of a Pause frame.
- Provides per-port side-band Pause state indication for upstream devices.
- Loss-less flow control on all valid frames up to 9.6 kbytes.

STATISTICS

- 40 bit counters are used to ensure rollover compliance with IEEE 802.3-1998.
- Minimum 58 minutes before rollover.
- Provides statistic counters to support SNMP and RMON implementations.

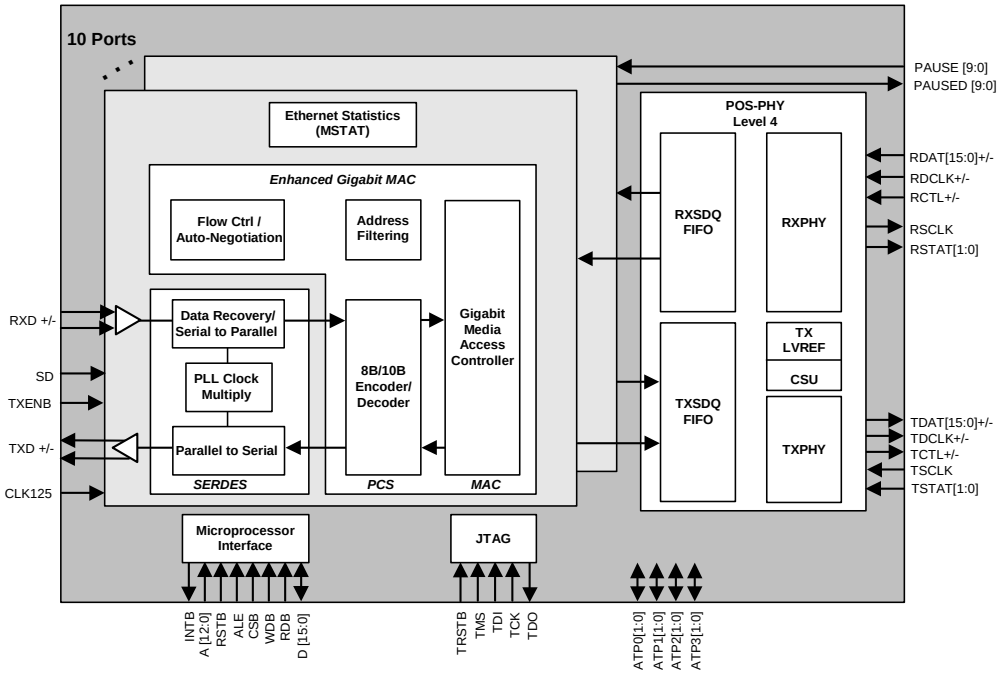
POS-PHY LEVEL 4 SYSTEM INTERFACE

- Designed to transmit cells, packets, or frames between physical and data-link layer devices.
- Requires fewer pins and draws less power than other 10 Gigabit interface options.
- Compliant with the following standards:
  - ATM Forum – Frame Based ATM Interface Level 4 (ATMF0161.00).
  - Optical Internetworking Forum – System Physical Interface Level 4 Phase II (OIF2000.088).

PACKAGING

- Flip Chip technology
- Implemented in low power 1.8 V CMOS technology with 3.3 V compatible I/O.
- Industrial temperature range (-40 °C to +85 °C).
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.

BLOCK DIAGRAM



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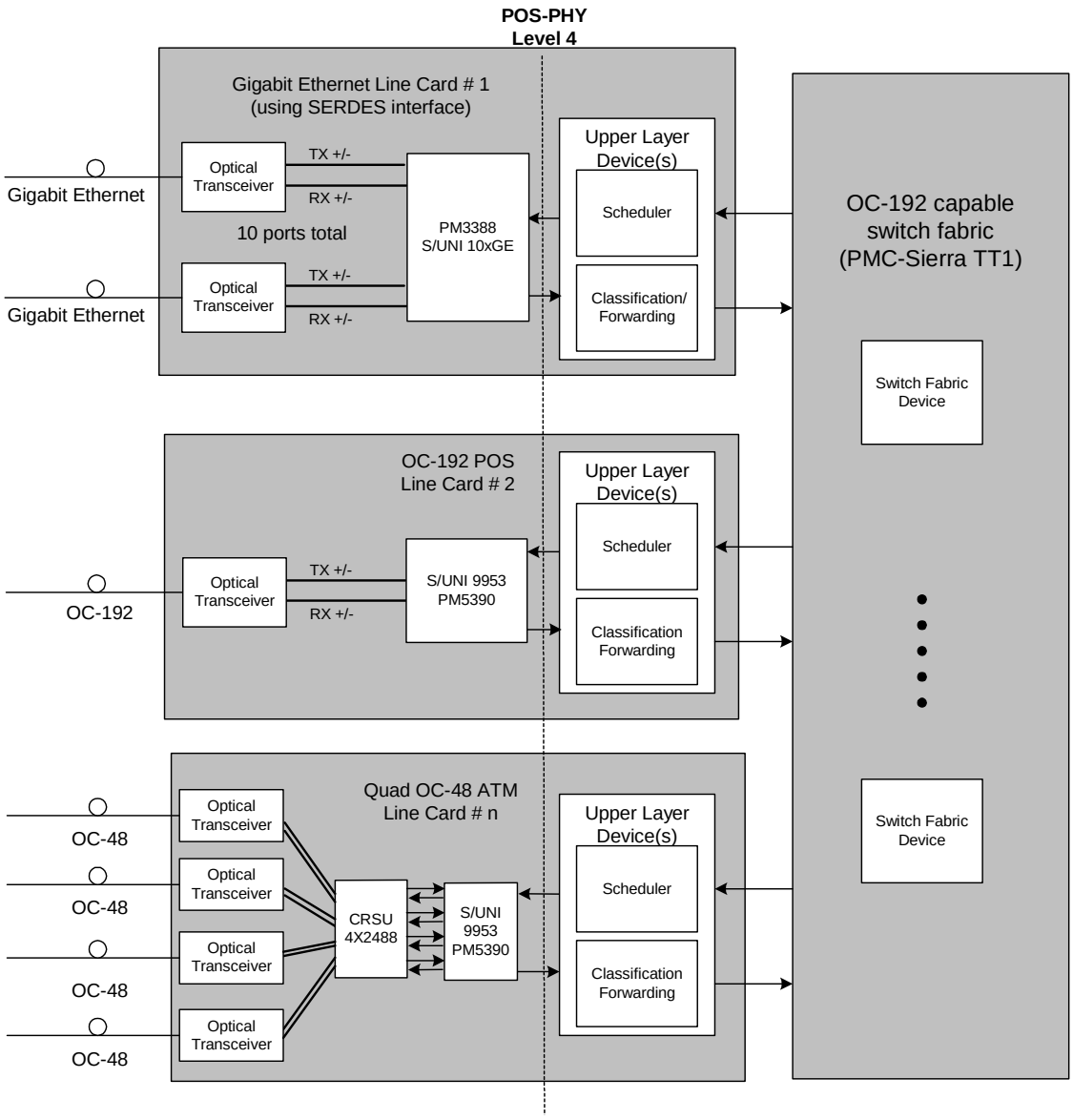
APPLICATIONS

- POS-PHY Level 4 provides consistent system interface for multiple PHY types.
- Edge and Core Routers.
- Multi-Service Switches.
- SONET/SDH Transport Equipment.

TYPICAL APPLICATIONS

SAMPLE LINE CARDS LINKED WITH POS-PHY LEVEL 4 INTERFACE



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