Low Voltage PLL Clock Driver

MPC954

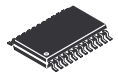
LOW VOLTAGE PLL ZERO DELAY BUFFER

The MPC954 is a 3.3V compatible, PLL based zero delay buffer targeted for high performance clock tree designs. With 11 outputs at frequencies of up to 100MHz and output skews of 200ps the MPC954 is ideal for the most demanding clock tree designs. The devices employ a fully differential PLL design to minimize cycle–to–cycle and phase jitter.

- Fully Integrated PLL
- Output Frequency up to 100MHz
- Outputs Disable in High Impedance
- TSSOP Packaging
- 50ps Cycle–to–Cycle Jitter Typical

The analog V_{CC} pin of the device also serves as a PLL bypass select pin. When driven low the V_{CCA} pin will route the REF_CLK input around the PLL directly to the outputs. The OE input is a logic enable for all of the outputs except QFB. A low on the OE pin forces Q0–Q9 to a logic low state.

The MPC954 is fully 3.3V compatible and requires no external loop filter components. All inputs accept LVCMOS or LVTTL compatible levels while the outputs provide LVCMOS levels with the ability to drive terminated 50Ω transmission lines. The output impedance of the MPC954 is ≈ 10Ω, therefore for series terminated 50Ω lines, each of the MPC954 outputs can drive two traces giving the device an effective fanout of 1:22. The device is packaged in a 24–lead TSSOP package to provide the optimum combination of board density and performance.



DT SUFFIX
24–LEAD TSSOP PACKAGE
CASE 948H–01

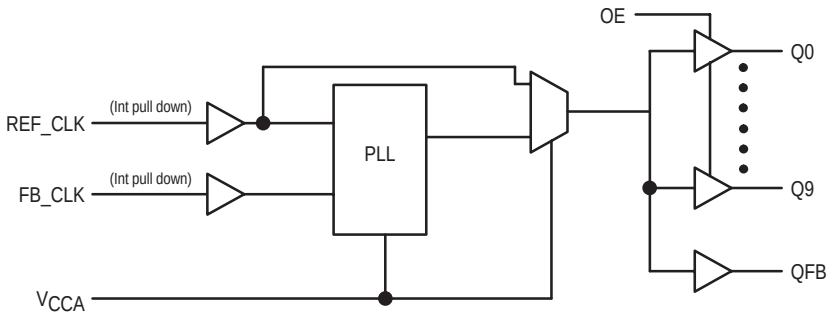


Figure 1. Block Diagram

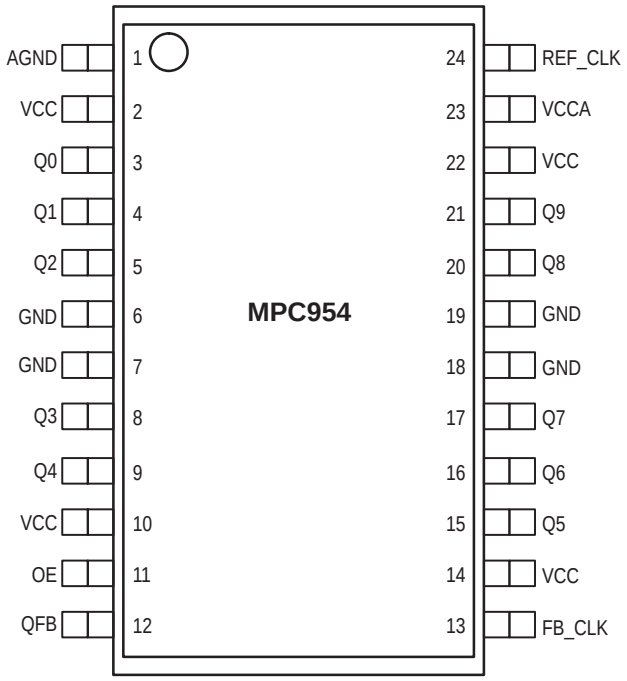


Figure 2. 24–Lead Pinout (Top View)

FUNCTION TABLES

V_{CCA}	Function
1	PLL Enabled
0	PLL Bypass

OE	Function
1	Q0 – Q9 Enabled
0	Q0 – Q9 Low

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage LVCMOS Inputs	2.0		3.6	V	
V_{IL}	Input LOW Voltage LVCMOS Inputs			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20mA, Note 1.
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20mA, Note 1.
I_{IN}	Input Current			±120	µA	Note 2.
C_{IN}	Input Capacitance			4	pF	
C_{pd}	Power Dissipation Capacitance		25		pF	Per Output
I_{CC}	Maximum Quiescent Supply Current		40		mA	All VCC Pins
I_{CCPLL}	Maximum PLL Supply Current		15		mA	VCCA Pin Only

1. The MPC954 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pullup resistor which affect input current.

PLL INPUT REFERENCE CHARACTERISTICS (T_A = 0 to 70°C)

Symbol	Characteristic	Min	Max	Unit	Condition
f_{ref}	Reference Input Frequency	50	100	MHz	
f_{refDC}	Reference Input Duty Cycle	25	75	%	

AC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time	0.3		1.5	ns	0.8 to 2.0V, (Note 3.)
t_{pw}	Output Duty Cycle	40	50	60	%	(Note 3.)
$t_{sk(O)}$	Output–to–Output Skews			300	ps	(Note 3.)
f_{max}	Maximum Output Frequency PLL Mode	50		100	MHz	(Note 3.)
t_{pd}(lock)	REF_CLK to FB_CLK Delay (with PLL Locked)	–300		0	ps	(Note 3.)
$t_{PLZ,HZ}$	Output Disable Time		7		ns	(Note 3.)
t_{PZL}	Output Enable Time		7		ns	(Note 3.)
t_{jitter}	Cycle–to–Cycle Jitter (Peak–to–Peak)		50		ps	(Note 3.)
t_{lock}	Maximum PLL Lock Time			10	ms	

3. Termination of 50Ω to V_{CC}/2.

Power Supply Filtering

The MPC954 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC954 provides separate power supplies for the output buffers (VCCO) and the phase–locked loop (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC954.

Figure 3 illustrates a typical power supply filter scheme. The MPC954 is most susceptible to noise with spectral content in the 1KHz to 10MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the VCCA pin of the MPC954. From the data sheet the I_{VCCA} current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

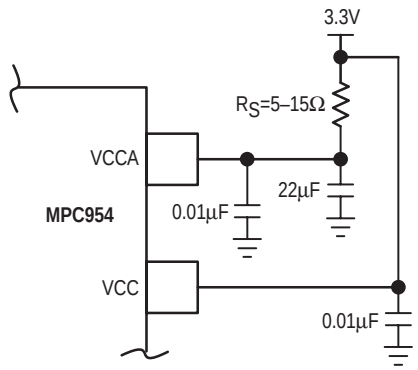


Figure 3. Power Supply Filter

Although the MPC954 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC954 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions brochure (BR1333/D).

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to VCC/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC954 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC954 clock driver is effectively doubled due to its capability to drive multiple lines.

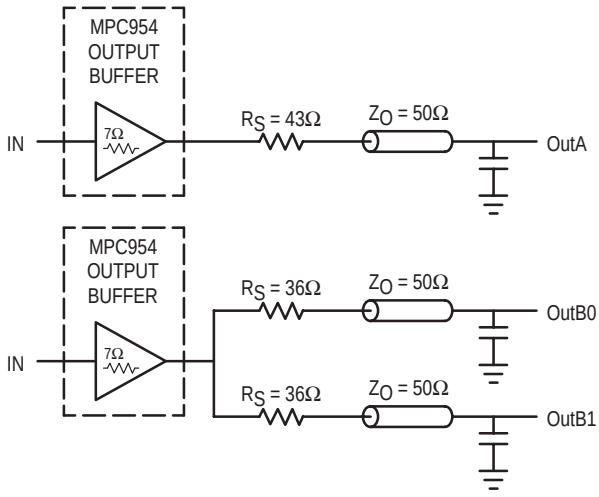


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC954 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC954. The output waveform in Figure 5 shows a step in the waveform, this step is caused

by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / (Rs + Ro + Zo))$$

$Zo = 50\Omega \parallel 50\Omega$
$Rs = 43\Omega \parallel 43\Omega$
$Ro = 7\Omega$

$$VL = 3.0 (25 / (21.5 + 7 + 25) = 3.0 (25 / 53.5)$$
$$= 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.80V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

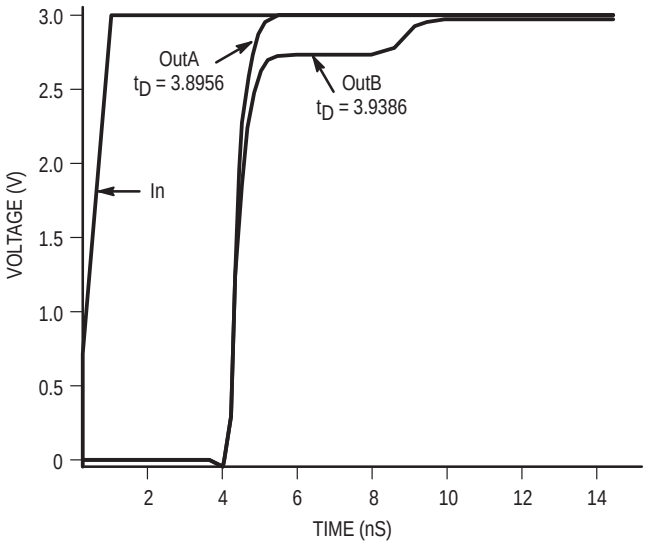
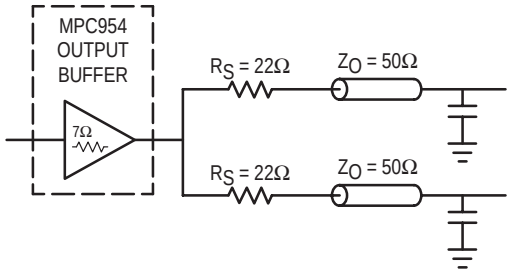


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



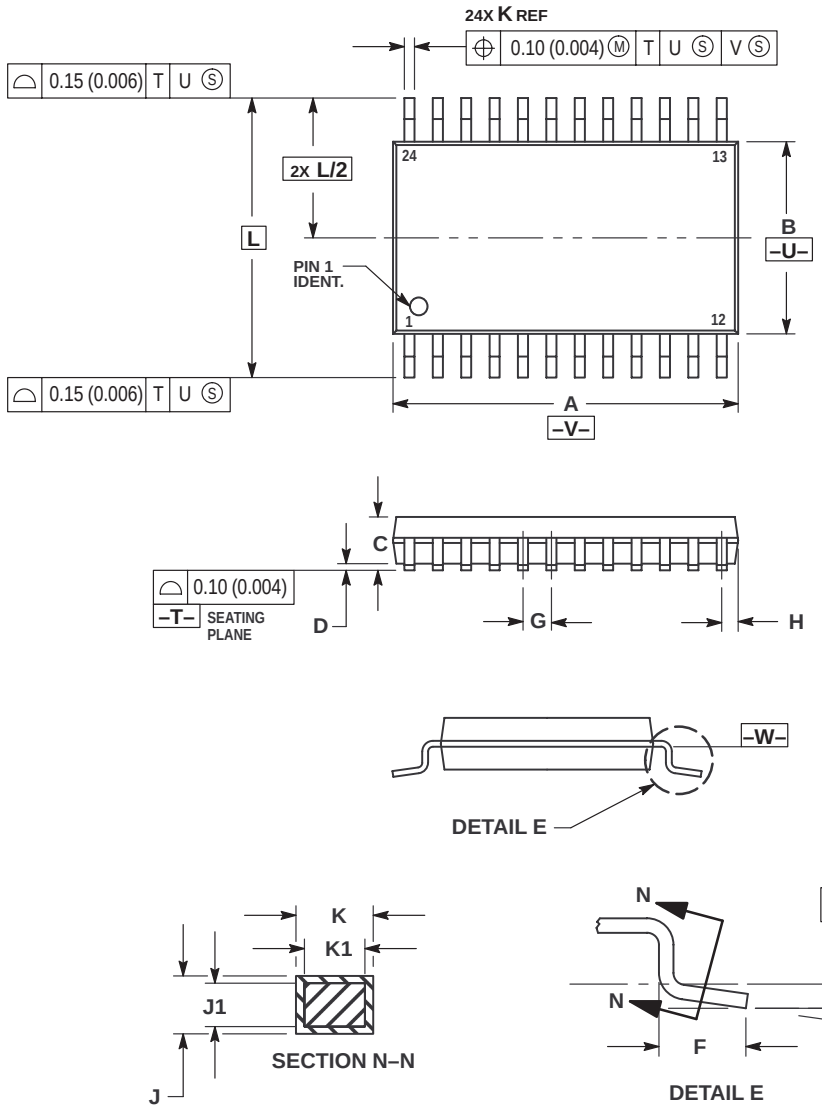
$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

Figure 6. Optimized Dual Line Termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

OUTLINE DIMENSIONS

DT SUFFIX
TSSOP PACKAGE
CASE 948H–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

NOTES

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