

M52342FP

PLL-SPLIT VIF/SIF IC

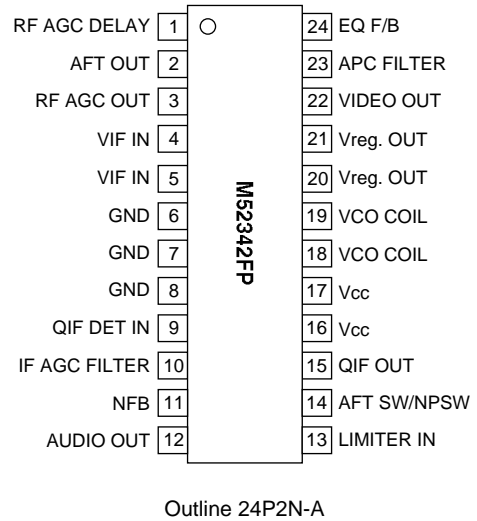
DESCRIPTION

The M52342FP is IF signal-processing IC for VCRs and TVs. It enable the PLL detection system despite size as small as that of conventional quasi-synchronous VIF/SIF detector, IF/RF AGC, SIF limiter, FM detector, QIF AGC and EQ AMP.

FEATURES

- Video detection output is 2V_{P-P}. It has built-in EQ AMP.
- The package is a 24-pin flat package, suitable for space saving.
- The video detector uses PLL for full synchronous detection circuit. It produces excellent characteristics of DG, DP, 920kHz beat, and cross color.
- Dynamic AGC realizes high speed response with only single filter.
- Video IF and sound IF signal processings are separated from each other. VCO output is used to obtain intercarrier. This PLL-SPLIT method and built-in QIF AGC provide good sound sensitivity and reduces buzz.
- As AFT output voltage uses the APC output voltage, VCO coil is not used.
- Audio FM demodulation uses PLL system, so it has wide frequency range with no external parts and no adjustment.

PIN CONFIGURATION (TOP VIEW)



APPLICATION

TV sets, VCR tuners

RECOMMENDED OPERATING CONDITION

In case of Vcc and Vreg. out short

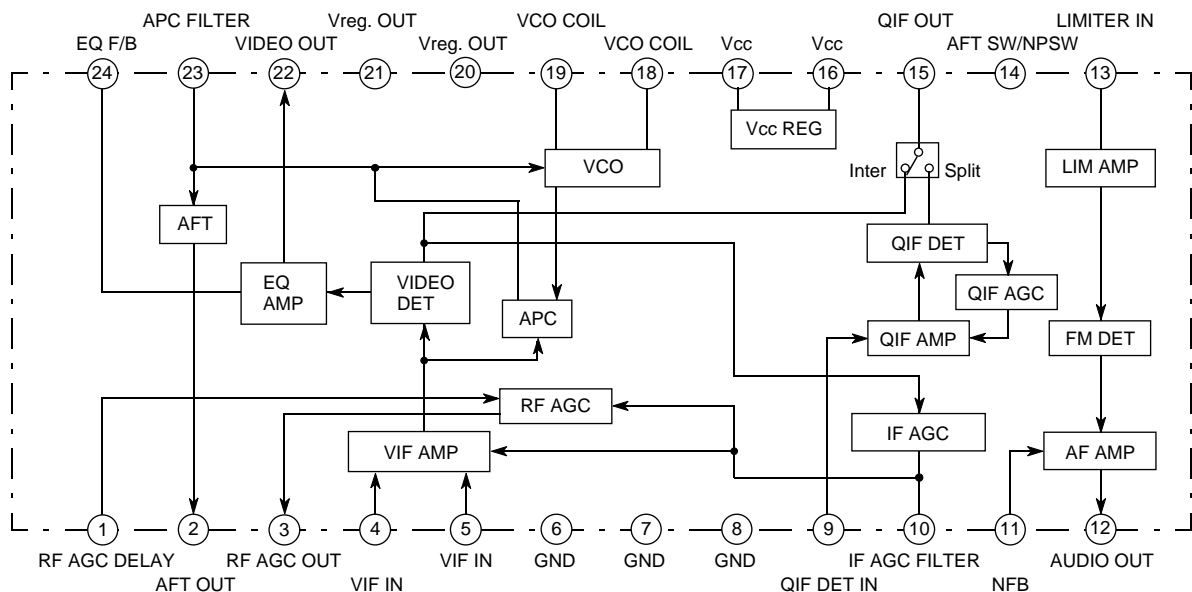
Supply voltage range.....4.75 to 5.25V

Recommended supply voltage.....5.0V

In case of Vreg. out open

Supply voltage range.....8.5 to 12.5V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C, surge protection capacitance 200pF resistance 0Ω, unless otherwise noted)

Symbol	Parameter	Condition	Ratings	Unit
Vcc	Supply voltage1	Vcc and Vreg. out is not connected to each other.	13.2	V
Vreg. OUT	Supply voltage Vreg. OUT	Vcc and Vreg. out is not connected to each other.	6.0	V
Pd	Power dissipation		1524	mW
Topr	Operating temperature		-20 to +75	°C
Tstg	Storage temperature		-40 to +150	°C
Surge	Surge voltage resistance		±200	V

AMBIENT OPERATING CONDITION (Ta=25°C, unless otherwise noted)

Supply voltage	Supply voltage range	Recommended supply voltage
In case of Vcc and Vreg. out short	4.75 to 5.25V	5.0V
In case of Vreg. out open	8.5 to 12.5V	–

ELECTRICAL CHARACTERISTICS (Vcc=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test circuit	Test point	Input point	Input SG	Measurement condition			Limits			Unit	
						External power supply			switches set to position 1 unless otherwise indicated	Min.	Typ.		Max.
						V7	V8	V12					
VIF section													
Icc1	Circuit current1 Vcc=5V	1	A	VIF IN	SG1	–	–	5	Vcc=5V SW17=1, SW14=2	33	46	59	mA
Icc2	Circuit current2 Vcc=12V	1	A	VIF IN	SG1	–	–	5	Vcc=12V SW14=SW17=2	33	46	59	mA
Vcc2	Vreg voltage	1	TP17	–	–	–	–	5	Vcc=12V SW7=2	4.60	4.95	5.30	V
V18	Video output DC voltage	1	TP18A	–	–	–	0	–	SW8=2	3.2	3.5	3.8	V
Vo det	Video output voltage	1	TP18A	VIF IN	SG1	–	–	–		1.8	2.1	2.4	Vp-P
Video S/N	Video S/N	1	TP18B	VIF IN	SG2	–	–	–	SW18=2	51	56	–	dB
BW	Video band width	1	TP18A	VIF IN	SG3	–	Variable	–	SW8=2	7.0	9.0	–	MHz
VIN MIN	Input sensitivity	1	TP18A	VIF IN	SG4	–	–	–		–	48	52	dBμ
VIN MAX	Maximum allowable input	1	TP18A	VIF IN	SG5	–	–	–		101	105	–	dBμ
GR	AGC control range input	–	–	–	–	–	–	–		50	57	–	dB
V8	IF AGC voltage	1	TP8	VIF IN	SG6	–	–	–		2.9	3.2	3.5	V
V8H	Maximum IF AGC voltage	1	TP8	–	–	–	–	–		4.0	4.4	–	V
V8L	Minimum IF AGC voltage	1	TP8	VIF IN	SG7	–	–	–		2.2	2.4	2.6	V
V3H	Maximum RF AGC voltage	1	TP3	VIF IN	SG6	–	–	–		4.2	4.7	–	V
									(Vcc=9V)	8.0	8.9	–	
									(Vcc=12V)	11.0	11.9	–	
V3L	Minimum RF AGC voltage	1	TP3	VIF IN	SG7	–	–	–		–	0.1	0.5	V
									(Vcc=9V)	–	0.2	0.7	
									(Vcc=12V)	–	0.2	0.7	
V3	RF AGC operation voltage	1	TP3	VIF IN	SG8	–	–	–		89	92	95	dBμ
CL-U	Capture range U	1	TP18A	VIF IN	SG9	–	–	–		1.0	1.7	–	MHz
CL-L	Capture range L	1	TP18A	VIF IN	SG9	–	–	–		1.8	2.4	–	MHz
CL-T	Capture range T	1	–	–	–	–	–	–		3.1	4.1	–	MHz
μ	AFT sensitivity	1	TP2	VIF IN	SG10	–	–	3.3		20	30	60	mV/kHz

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test circuit	Test point	Input point	Input SG	Measurement condition						Limits			Unit
						External power supply			switches set to position 1 unless otherwise indicated			Min.	Typ.	Max.	
						V7	V8	V12							
V2H	AFT maximum voltage	1	TP2	VIF IN	SG10	–	–	3.3	(Vcc=9V)	3.85	4.15	–	V		
								(Vcc=12V)	7.7	8.1	–				
									10.7	11.1	–				
V2L	AFT minimum voltage	1	TP2	VIF IN	SG10	–	–	3.3	(Vcc=9V)	–	0.7	1.2	V		
								(Vcc=12V)	–	0.7	1.2				
									–	0.7	1.2				
AFT def1	AFT defeat 1	1	TP2	VIF IN	SG10	–	–	1.65	(Vcc=9V)	2.2	2.5	2.8	V		
								(Vcc=12V)	4.1	4.5	4.9				
									5.5	6.0	6.5				
AFT def2	AFT defeat 2	1	TP2	VIF IN	SG10	–	–	4.6	(Vcc=9V)	2.2	2.5	2.8	V		
								(Vcc=12V)	4.1	4.5	4.9				
									5.5	6.0	6.5				
IM	Inter modulation	1	TP18A	VIF IN	SG11	–	Variable	–	SW8=2	35	40	–	dB		
DG	Differential gain	1	TP18A	VIF IN	SG12	–	–	–		–	2	5	%		
DP	Differential phase	1	TP18A	VIF IN	SG12	–	–	–		–	2	5	deg		
V18 SYNC	Sync. tip level	1	TP18A	VIF IN	SG2	–	–	–		0.85	1.15	1.45	V		
RINV	VIF input resistor	2	TP4							–	1.2	–	kΩ		
CINV	VIF input capacitance	2	TP4							–	5	–	pF		
SIF section															
QIF1	QIF output 1	1	TP13	VIF IN QIF IN	SG2 SG13	–	–	–		94	100	106	dBμ		
QIF2	QIF output 2	1	TP13	VIF IN QIF IN	SG2 SG14	–	–	–		94	100	106	dBμ		
Vos	SIF detection output	1	TP13	VIF IN	SG15	0	–	5	SW7=2	94	100	106	dBμ		
V1	AF output DC voltage	1	TP10	SIF IN	SG20	–	–	5		1.6	2.2	2.8	V		
VoAF1	AF output (4.5MHz)	1	TP10	SIF IN	SG16	–	–	5		400	560	800	mVrms		
VoAF2	AF output (5.5MHz)	1	TP10	SIF IN	SG21	–	–	0		320	450	630	mVrms		
THD AF1	AF output distortion (4.5MHz)	1	TP10	SIF IN	SG16	–	–	5		–	0.2	0.9	%		
THD AF2	AF output distortion (5.5MHz)	1	TP10	SIF IN	SG21	–	–	0		–	0.2	0.9	%		
LIM1	Limiting sensitivity (4.5MHz)	1	TP10	SIF IN	SG17 SG19	–	–	5		–	42	55	dBμ		
LIM2	Limiting sensitivity (5.5MHz)	1	TP10	SIF IN	SG22 SG24	–	–	0		–	42	55	dBμ		
AMR1	AM rejection (4.5MHz)	1	TP10	SIF IN	SG18	–	–	5		55	62	–	dB		
AMR2	AM rejection (5.5MHz)	1	TP10	SIF IN	SG23	–	–	0		55	64	–	dB		
AF S/N 1	AF S/N (4.5MHz)	1	TP10	SIF IN	SG20	–	–	5		55	62	–	dB		
AF S/N 2	AF S/N (5.5MHz)	1	TP10	SIF IN	SG25	–	–	0		55	64	–	dB		
RINS	SIF input resistance	2	TP7							–	1.5	–	kΩ		
CINS	SIF input capacitance	2	TP7							–	4	–	pF		
Control section															
CqIF	QIF control	1	TP7	–	–	Variable	–	–	SW7=2	–	0.7	1.0	V		

PIN12 VOLTAGE CONTROL

Pin12 voltage (V)		AF	AFT
0 to 2.3	0 to 0.6	PAL	NORMAL
	1.0 to 2.3		DEFEAT
2.7 to 5.0	2.7 to 4.0	NTSC	NORMAL
	4.4 to 5.0		DEFEAT

ELECTRICAL CHARACTERISTICS TEST METHOD

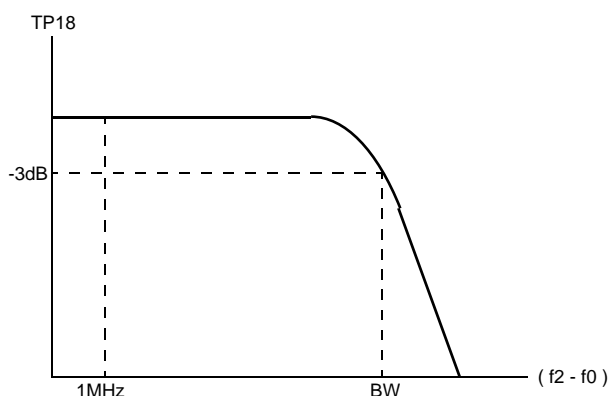
Video S/N

Input SG2 into VIF IN and measure the video out (Pin 18) noise in r.m.s at TP18B through a 5MHz (-3dB) L.P.F.

$$S/N=20 \log \left(\frac{0.7 \times V_o \text{ det}}{\text{NOISE}} \right) (\text{dB})$$

BW Video band width

1. Measure the 1MHz component level of EQ output TP18A with a spectrum analyzer when SG3 (f2=57.75MHz) is input into VIF IN. At that time, measure the voltage at TP8 with SW8, set to position 2, and then fix V8 at that voltage.
2. Reduce f2 and measure the value of (f2-f0) when the (f2-f0) component level reaches -3dB from the 1MHz component level as shown below.



VIN MIN Input sensitivity

Input SG4 (Vi=90dBμ) into VIF IN, and then gradually reduce Vi and measure the input level when the 20kHz component of EQ output TP18A reaches -3dB from Vo det level.

VIN MAX Maximum allowable input

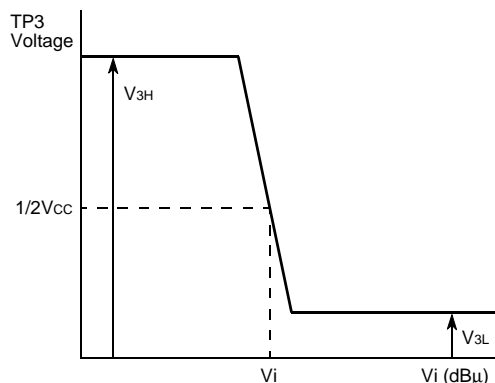
1. Input SG5 (Vi=90dBμ) into VIF IN, and measure the level of the 20kHz component of EQ output.
2. Gradually increase the Vi of SG and measure the input level when the output reaches -3dB.

GR AGC control range

$$GR=VIN \text{ MAX}-VIN \text{ MIN} (\text{dB})$$

V3 RF AGC operating voltage

Input SG8 into VIF IN, and gradually reduce Vi and then measure the input level when RF AGC output TP3 reaches 1/2 Vcc, as shown below.



CL-U Capture range

1. Increase the frequency of SG9 until the VCO is out of locked-oscillation.
2. Decrease the frequency of SG9 and measure the frequency fU when the VCO locks.

$$CL-U=fU-58.75 (\text{MHz})$$

CL-L Capture range

1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
2. Increase the frequency of SG9 and measure the frequency fL when the VCO locks.

$$CL-L=58.75-fL (\text{MHz})$$

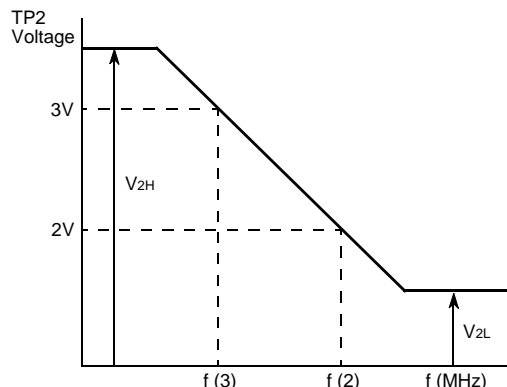
CL-T Capture range

$$CL-T=CL-U+CL-L (\text{MHz})$$

μ AFT sensitivity, V2H Maximum AFT voltage, V2L Minimum AFT voltage

1. Input SG10 into VIF IN, and set the frequency of SG10 so that the voltage of AFT output TP2 is 3V. This frequency is named f(3).
2. Set the frequency of SG10 so that the AFT output voltage is 2V. This frequency is named f(2)

3. IN the graph, maximum and minimum DC voltage are V_{2H} and V_{2L} , respectively.



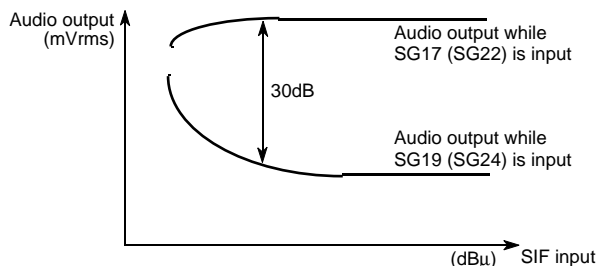
$$\mu = \frac{1000 \text{ (mV)}}{f(2) - f(3) \text{ (kHz)}} \text{ (mV/kHz)}$$

IM Intermodulation

1. Input SG11 into VIF IN, and measure EQ output TP18A with an oscilloscope.
2. Adjust AGC filter voltage V8 so that the minimum DC level of the output waveform is 1.0V.
3. At this time, measure, TP18A with a spectrum analyzer.
The intermodulation is defined as a difference between 920kHz and 3.58MHz frequency components.

LIM Limiting sensitivity

1. Input SG17 (SG22) into SIF input, and measure the 400Hz component level of AF output TP10.
2. Input SG19 (SG24) into SIF input, and measure the 400Hz component level of AF output TP10.
3. The input limiting sensitivity is defined as the input level when a difference between each 400Hz components of audio output (TP10) is 30dB, as shown below.



AMR AM Rejection

1. Input SG18 (SG23) into SIF input, and measure the output level of AF output TP10. This level is named VAM.
2. AMR is;

$$AMR = 20 \log \left(\frac{V_{oAF} \text{ (mVr.m.s)}}{V_{AM} \text{ (mVr.m.s)}} \right) \text{ (dB)}$$

AF S/N

1. Input SG20 (SG25) into SIF input, and measure the output noise level of AF output TP1. This level is named VN.
2. S/N is;

$$S/N = 20 \log \left(\frac{V_{oAF} \text{ (mVr.m.s)}}{V_N \text{ (mVr.m.s)}} \right) \text{ (dB)}$$

CaIF QIF control

Lower the voltage of V7, and measure the voltage of V7 when DC voltage of TP13 begins to change.

THE NOTE IN THE SYSTEM SETUP

M52342FP has 2 power supply pins of Vcc (pin 14) and Vreg. OUT (pin 17). Pin 14 is for AFT output, RF AGC output circuits and 5V regulated power circuit and Pin 17 is for the other circuit blocks.

In case M52342FP is used together with other ICs like VIF operating at more than 5V, the same supply voltage as that of connected ICs is applied to Vcc and Vreg. Out is opened. The other circuit blocks, connected to Vreg. OUT are powered by internal 5V regulated power supply.

In case the connecting ICs are operated at 5V, 5V is supplied to both Vcc and Vreg.OUT.

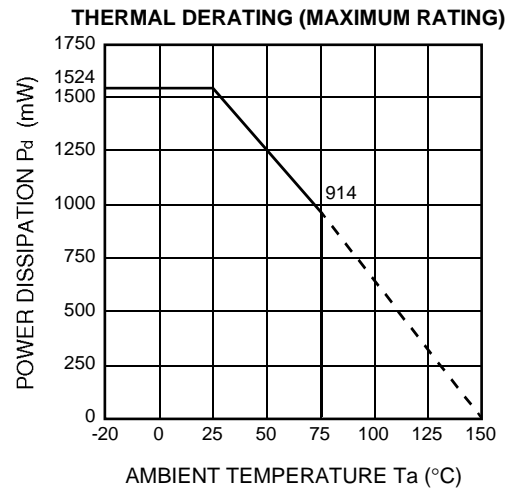
LOGIC TABLE

		AF	AFT
10k "H"	20k "H"	NTSC	DEFEAT
	20k "L"		NORMAL
10k "L"	20k "H"	PAL	DEFEAT
	20k "L"		NORMAL

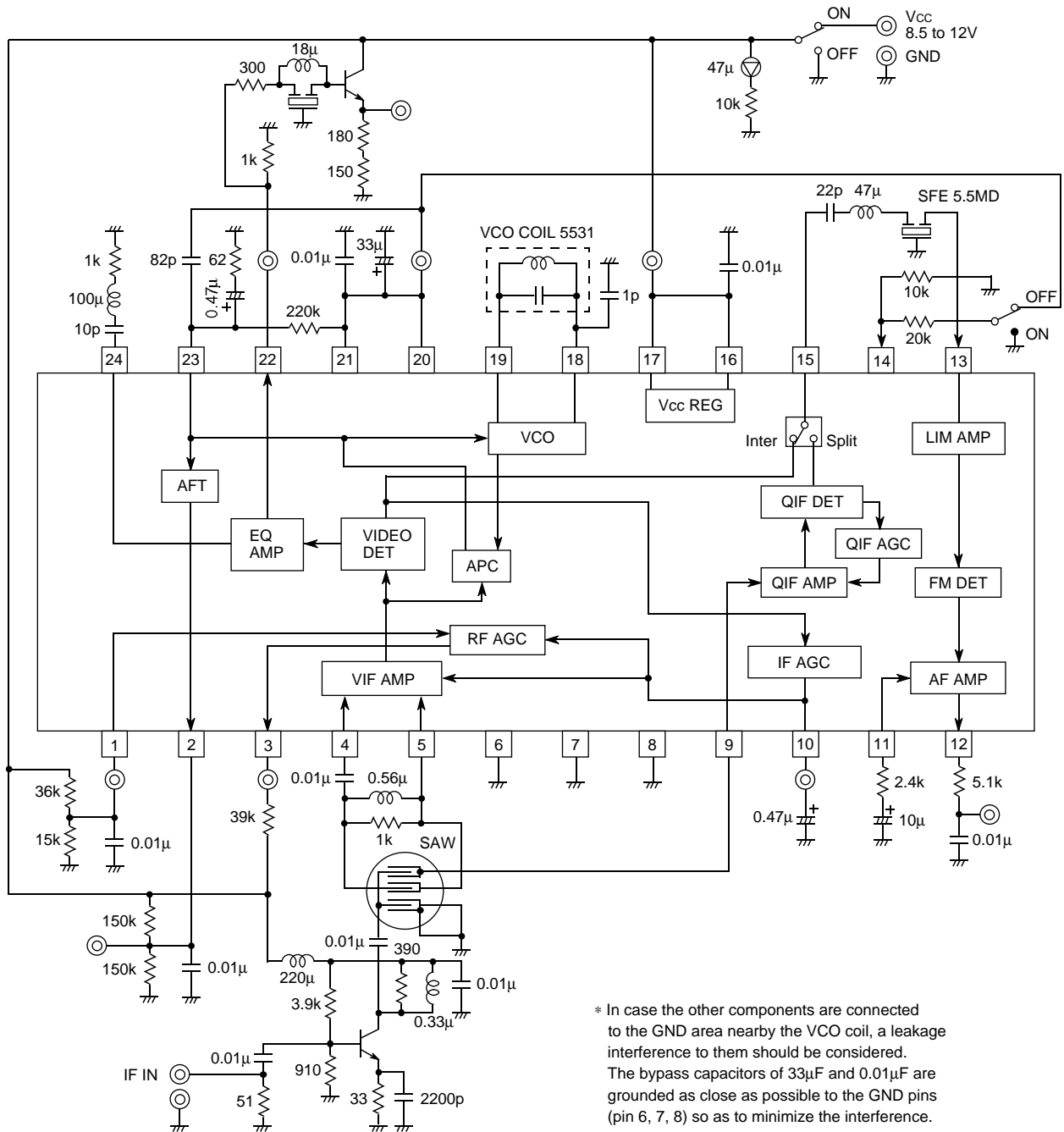
INPUT SIGNAL

SG No.	Signals (50Ω termination)
1	f ₀ =58.75MHz AM20kHz 77.8% 90dB _μ
2	f ₀ =58.75MHz 90dB _μ CW
3	f ₁ =58.75MHz 90dB _μ CW (Mixed signal) f ₂ =Frequency variable 70dB _μ CW (Mixed signal)
4	f ₀ =58.75MHz AM20kHz 77.8% level variable
5	f ₀ =58.75MHz AM20kHz 14.0% level variable
6	f ₀ =58.75MHz 80dB _μ CW
7	f ₀ =58.75MHz 110dB _μ CW
8	f ₀ =58.75MHz CW level variable
9	f ₀ =Variable AM20kHz 77.8% 90dB _μ
10	f ₀ =Variable 90dB _μ CW
11	f ₁ =58.75MHz 90dB _μ CW (Mixed signal) f ₂ =55.17MHz 80dB _μ CW (Mixed signal) f ₃ =54.25MHz 80dB _μ CW (Mixed signal)
12	f ₀ =58.75MHz 87.5% TV modulation ten-step waveform Sync tip level 90dB _μ
13	f ₁ =54.25MHz 95dB _μ CW
14	f ₁ =54.25MHz 75dB _μ CW
15	f ₁ =58.75MHz 90dB _μ CW (Mixed signal) f ₂ =54.25MHz 70dB _μ CW (Mixed signal)
16	f ₀ =4.5MHz 90dB _μ FM400Hz±25kHz dev
17	f ₀ =4.5MHz FM400Hz±25kHz dev level variable
18	f ₀ =4.5MHz 90dB _μ AM400Hz 30%
19	f ₀ =4.5MHz CW level variable
20	f ₀ =4.5MHz 90dB _μ CW
21	f ₀ =5.5MHz 90dB _μ FM400Hz±50kHz dev
22	f ₀ =5.5MHz FM400Hz±50kHz dev level variable
23	f ₀ =5.5MHz 90dB _μ AM400Hz 30%
24	f ₀ =5.5MHz CW level variable
25	f ₀ =5.5MHz 90dB _μ CW

TYPICAL CHARACTERISTICS

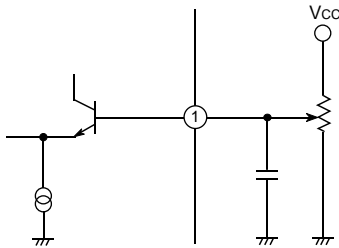


TYPICAL APPLICATION EXAMPLE (for 38.9MHz SPLIT)



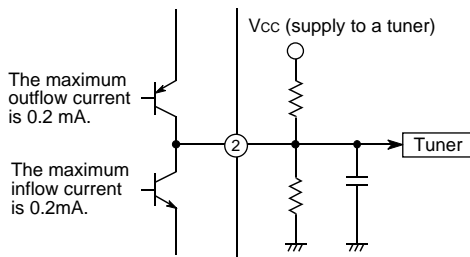
Units Resistance : Ω
Capacitance : F

Pin 1 (RF AGC DELAY)



An applied voltage to the pin1 is for changing a RF AGC delay point.

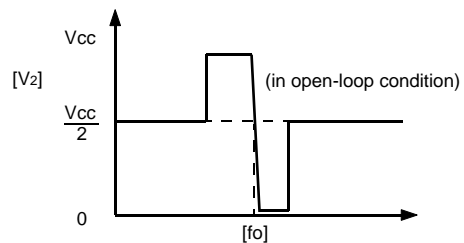
Pin 2 (AFT OUTPUT)



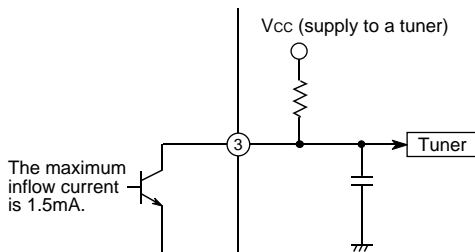
Since an AFT output is provided by a high impedance source, the detection sensitivity can be set by an external resistor.

The muting operation will be on in following two cases;

- 1) the APC is out of locking,
- 2) the video output becomes small enough in a weak electric field.

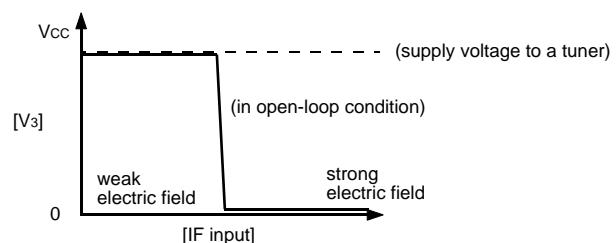


Pin 3 (RF AGC OUTPUT)



A current mode output is available in the reverse AGC operation.

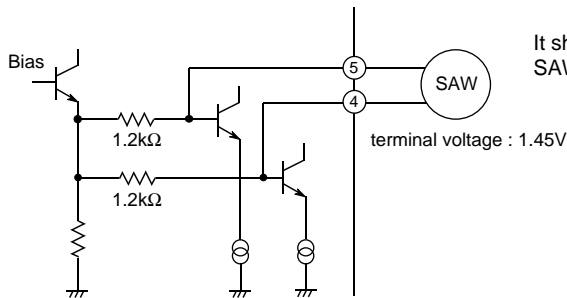
The fluctuation of a bottom voltage is made small by loading higher impedance for a deep saturation.



Note: Connecting a nonpolarity capacitor of 1μF between pin1 and pin 3 improves AGC operating speed.

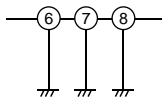
In that case, the capacitors between pin1/pin3 and ground should be removed.

Pin 4, Pin 5 (VIF INPUT)



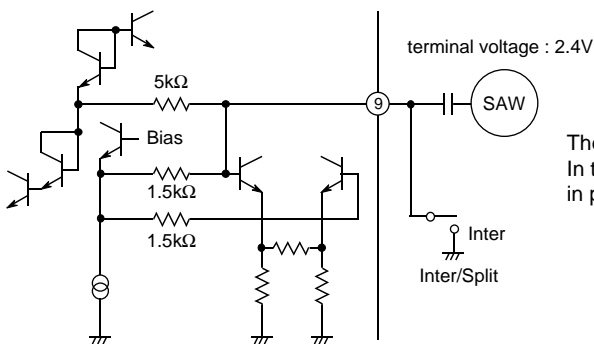
It should be designed considering careful impedance matching with the SAW filter.

Pin 6, Pin 7, Pin 8 (GND)



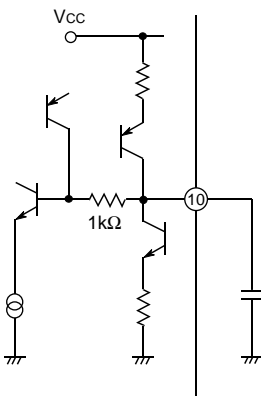
They are all ground pins.

Pin 9 (QIF INPUT, INTER SW)

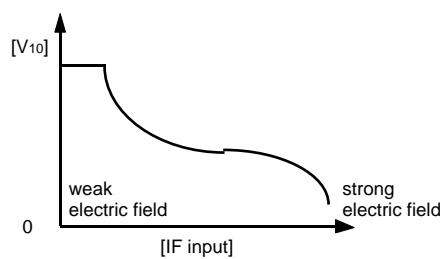


The input impedance is 1.5kΩ.
In the intercarrier system application, the intercarrier output is available in pin 15 by connecting pin 9 to ground.

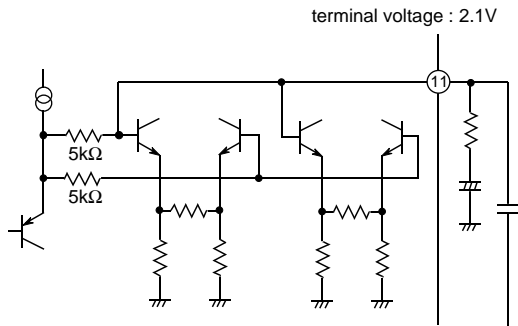
Pin 10 (IF AGC FILTER)



In spite of the 1-pin filter configuration, 2-pin filter characteristics are available by utilizing the dynamic AGC circuit.

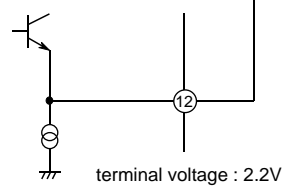


Pin 11 (AUDIO F/B)



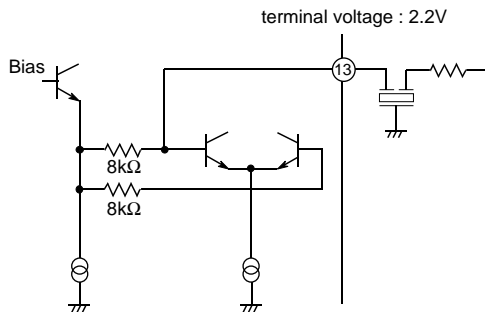
The FM detector can respond to several kinds of SIF signals without an adjustment and external components by adopting the PLL technique. It also is in compliance with the multi-SIF by selecting an appropriate deemphasis and audio output amplifier using the pin14 switch. The capacitor between pin 11 and 12, which fixes the deemphasis characteristics, can be determined considering the combination of an equivalent resistance of the IC and this capacitor itself.

Pin 12 (AF OUTPUT)



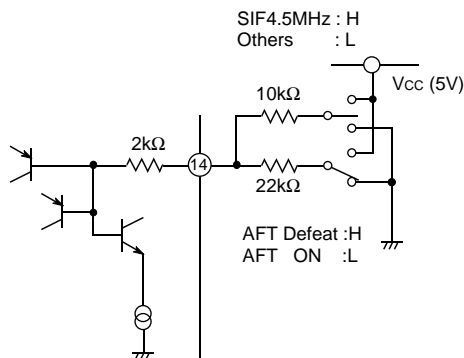
In the 4.5MHz application, the internal voltage gain is increased by 6-dB in comparison with the other applications and then the signals are delivered through an emitter follower.

Pin 13 (LIMITER INPUT)



The input impedance is 8kΩ.

Pin 14 (AFT SW, NP SW)

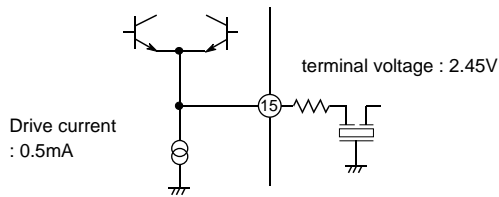


It works as a switch by connecting the resistor to 5V(High) or GND (Low), alternately.

10kΩ	20kΩ	AF AMP	AFT	Pin 14 applied voltage
H	H	4.5MHz	DEFFET	4.4 to 5.0V
H	L	4.5MHz	NORMAL	2.7 to 4.0V
L	H	OTHER	DEFFET	1.0 to 2.3V
L	L	OTHER	NORMAL	0 to 0.6V

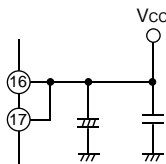
The terminal voltage is set by the external resistors because of an open base input.

Pin 15 (QIF OUTPUT / INTER OUTPUT)



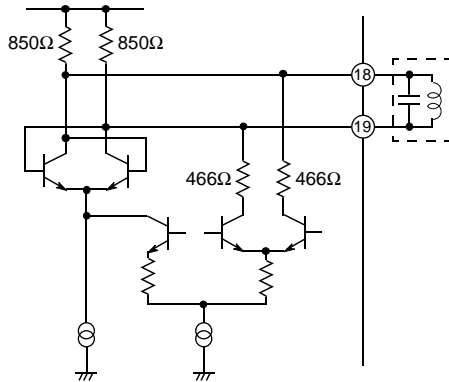
In both the split and intercarrier system, the carrier signal to SIF provided from pin 15 through an emitter follower.

Pin 16, Pin 17 (Vcc)



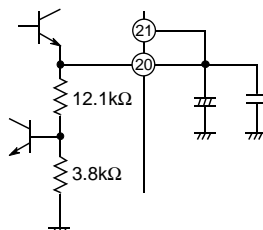
The recommended supply voltage is 5V or 9 to 12V.
 In the case of 5V supply, these pins should be tied to pin 20 and pin 21.
 In the case of 9 to 12V supply, a regulated output of 5V are available in pin 20 and 21.

Pin 18, Pin 19 (VCO COIL)



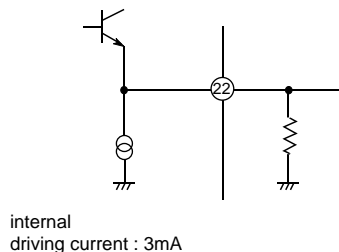
Connecting a tuning coil and capacitor to these pins enables an oscillation.
 The tuning capacitor of about 30pF is recommended.
 The oscillation frequency is tuned in f_0 .
 In the actual adjustment, the coil is tuned so that the AFT voltage is reached to $V_{cc}/2$ with f_0 as an input.
 The printed pattern around these pins should be designed carefully to prevent a pull-in error of VCO, caused by the leakage interference from the large signal level oscillator to adjacent pins.
 The interconnection also should be designed as short as possible.

Pin 20, Pin 21 (REG OUTPUT)

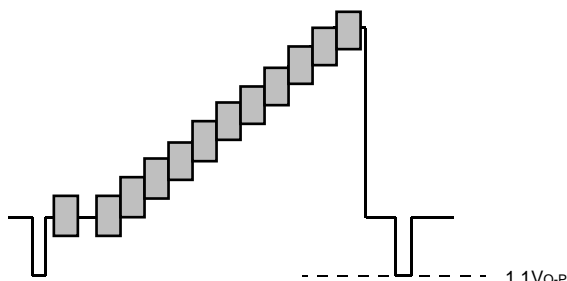


It is a regulated 5V output which has current drive capability of approximately 15mA.

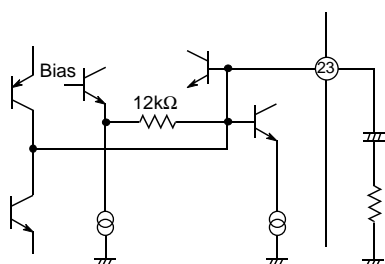
Pin 22 (VIDEO OUTPUT)



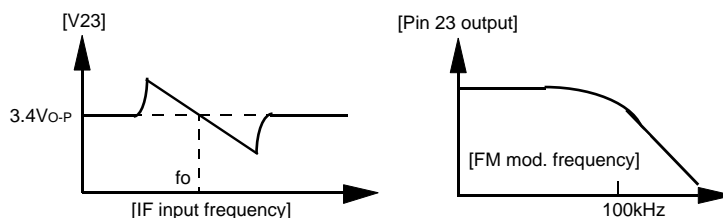
An output amplitude is positive 2V_{P-P} in the case of 87.5% video modulation.



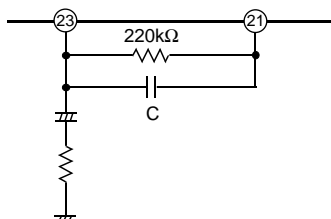
Pin 23 (APC FILTER)



In the locked state, the cut-off frequency of the filter is adjusted effectively by an external resistor so that it will be in the range of around 30 to 200kHz. In case the cut-off frequency is lower, the pull-in speed becomes slow. On the other hand, a higher cut-off frequency widens the pull-in range and band width, which results in a degradation in the S/N ratio. So, in the actual TV system design, the appropriate constant should be chosen for getting desirable performance considering above conditions.



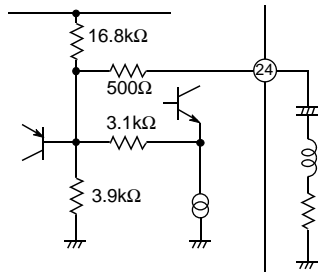
In the application, an offset between AFT center frequency and VCO free-running frequency, can be improved by connecting a 220kΩ resistor to Vcc supply (pin 21).



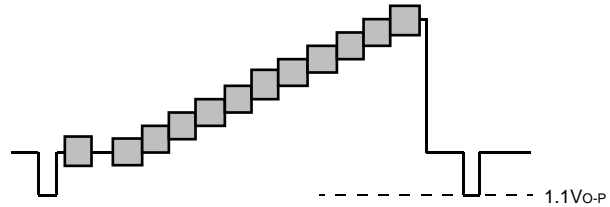
A buzz noise also decreases by connecting a capacitor from pin 23 to Vcc (pin 21) or GND. This effect utilizes the signal interference on the printed circuit board. So, the determination that which connection is effective, to Vcc or GND, is done by a cut and try method.

The capacitor of less than 680pF, which depends on Q of VCO coil, is recommended to prevent an APC pull-in range from narrowing. Taking it into consideration in the actual TV set design.

Pin 24 (EQ F/B)



Both the external coil and capacitor determine the frequency response of EQ output.
The series connected resistor is for damping.

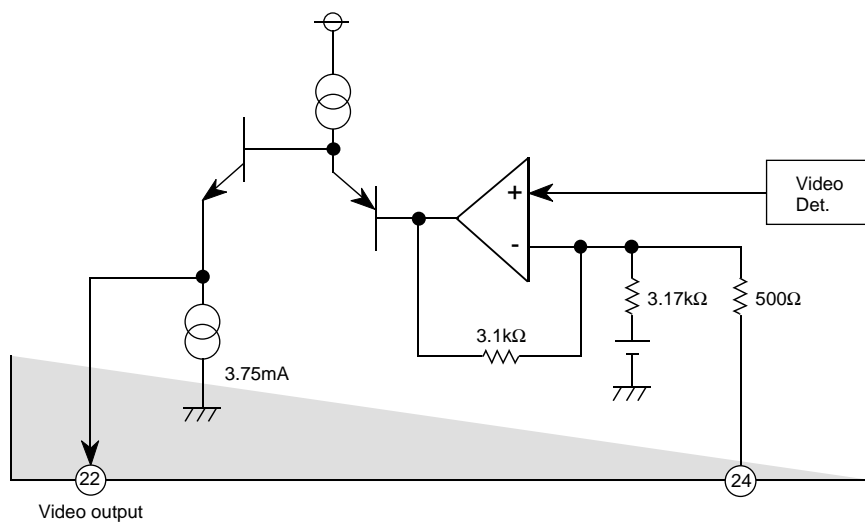


In the intercarrier system, the following phenomenon should be considered;

a strong equalization (EQ) enlarge the sound carrier output from pin 22, because the EQ is applied before an audio trap.

In that case, the next two solutions are recommended;

decrease in S level of SAW, avoiding to peak a sound carrier in EQ.



(Circuit Diagram of EQ Amp.)