

MSM52V1017LL**65,536-Word × 16-Bit CMOS STATIC RAM****DESCRIPTION**

The MSM52V1017LL is a 65,536-word by 16-bit CMOS static RAM featuring 2.7 V to 3.6 V power supply operation and direct LVC MOS input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM52V1017LL can be used in the high-speed operation of an access time 85 ns due to adopting a high-performance CMOS technology and in the very low current consumption of a standby current max. 20 μ A when there is no chip selection. In addition, the MSM52V1017LL is provided with a chip enable signal (CE) suited to the expansion of a memory capacity, an output enable signal (\overline{OE}) suited to the I/O bus line control, and a byte select signal (\overline{LB} , \overline{UB}) that can independently control the input/output of a lower byte and an upper byte.

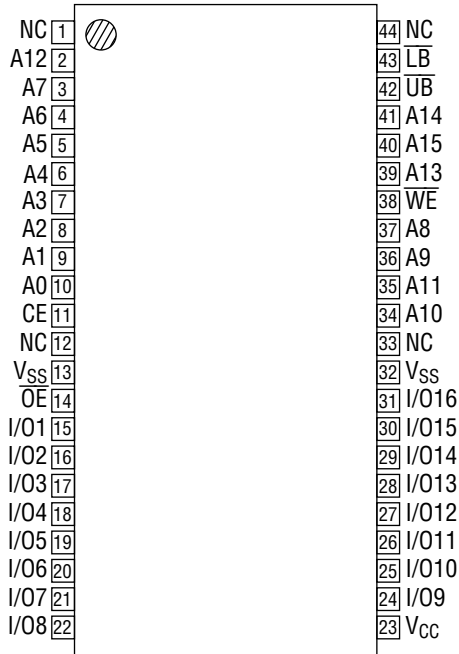
FEATURES

- 65,536-word × 16-bit configuration
- Power supply voltage: 2.7 V to 3.6 V
- Fully static operation
- Operating temperature range: $T_a = 0^\circ\text{C}$ to 70°C
- (Input/Output) LVC MOS compatible
- 3-state output
- Data retention available at power supply voltage 2 V
- Equal to Mask ROM/OTP in supply pin layout
- Package options:
 - 44-pin 400 mil plastic TSOP (Type II) (TSOPII44-P-400-0.80-K) (Product: MSM52V1017LL-xxTS-K)
 - (TSOPII44-P-400-0.80-L) (Product: MSM52V1017LL-xxTS-L)
 xx indicates speed rank.

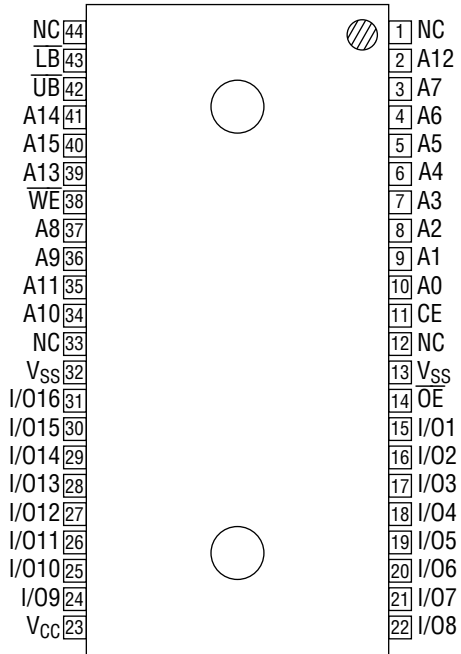
PRODUCT FAMILY

Family	Access Time (Max.)	Power Dissipation	
		Operating (Max.)	Standby (Max.)
MSM52V1017LL-85	85 ns	216 mW	0.072 mW
MSM52V1017LL-10	100 ns	180 mW	
MSM52V1017LL-12	120 ns	144 mW	

PIN CONFIGURATION (TOP VIEW)



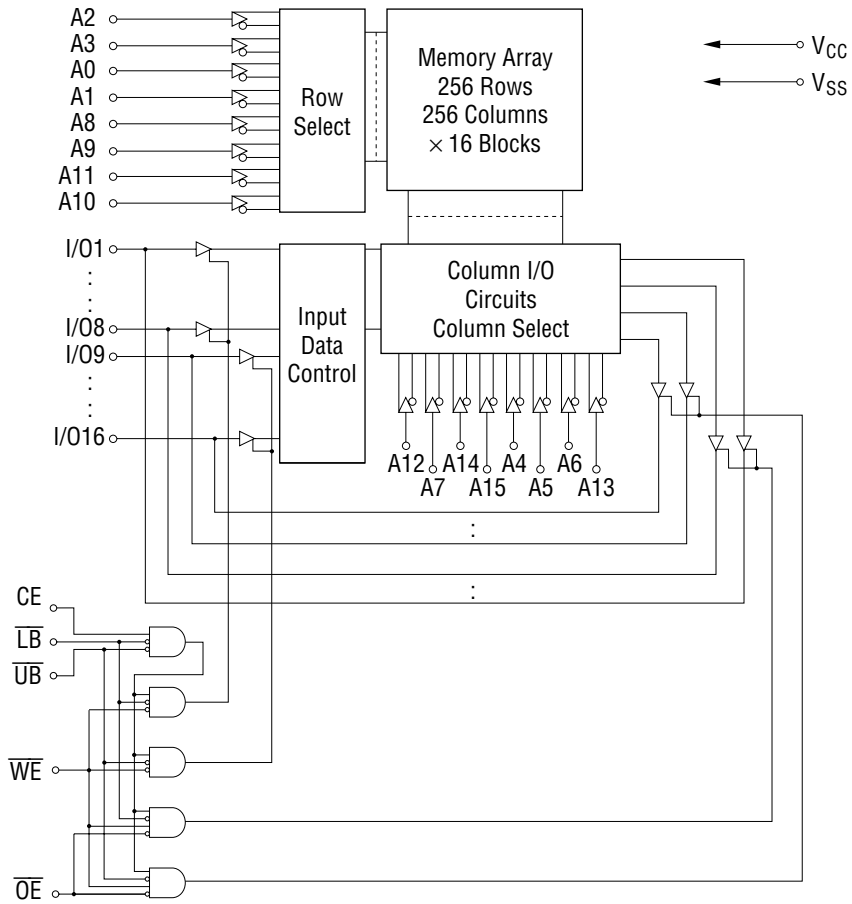
44-Pin Plastic TSOP (II)
(K Type)



44-Pin Plastic TSOP (II)
(L Type)

Pin Name	Function
A0 - A15	Address Input
I/O1 - I/O16	Data Input/Output
CE	Chip Enable
WE	Write Enable
OE	Output Enable
LB, UB	Byte Data Select
Vcc, Vss	Power Supply
NC	No Connection

BLOCK DIAGRAM



FUNCTION TABLE

Operating Mode	CE	LB	UB	WE	OE	I/O1 - I/O8	I/O9 - I/O16	Power Mode
Non Selectable	L	X	X	X	X	High-Z	High-Z	Standby
	X	H	H	X	X	High-Z	High-Z	Standby
Read Cycle	H	L	L	H	L	Data Read	Data Read	Active
	H	L	H	H	L	Data Read	High-Z	Active
	H	H	L	H	L	High-Z	Data Read	Active
	H	L	L	H	H	High-Z	High-Z	Active
	H	L	H	H	H	High-Z	High-Z	Active
	H	H	L	H	H	High-Z	High-Z	Active
Write Cycle	H	L	L	L	X	Data Write	Data Write	Active
	H	L	H	L	X	Data Write	High-Z	Active
	H	H	L	L	X	High-Z	Data Write	Active

X: Don't Care ("H" or "L")

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{CC}	$T_a = 25^\circ\text{C}$, for V_{SS}	-0.5 to 4.6	V
Pin Voltage	V_T		-0.5* to $V_{CC} + 0.5$	V
Power Dissipation	P_D	$T_a = 25^\circ\text{C}$	0.7	W
Operating Temperature	T_{opr}	—	0 to 70	$^\circ\text{C}$
Storage Temperature	T_{stg}	—	-55 to 125	$^\circ\text{C}$

* -1.2 V Min. for pulse width less than 30 ns.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	—	2.7	—	3.6	V
	V_{SS}		0	0	0	V
Data Retention Voltage	V_{CCH}	—	2	—	3.6	V
Input High Voltage	V_{IH}	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.2	—	$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}		-0.3*	—	0.4	V
Load Capacitance	C_L	—	—	—	100	pF
Fan Out	N	LVC MOS	—	—	1	—

* -1.2 V Min. for pulse width less than 30 ns.

Capacitance

($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	C_I	$V_I = 0\text{ V}$	—	10	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$	—	10	pF

Note: This parameter is periodically sampled and not 100% tested.

DC Characteristics

(V_{CC} = 2.7 V to 3.6 V, T_a = 0°C to 70°C)

Parameter	Symbol	Condition	MSM52V1017LL			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I _{LI}	V _{IN} = 0 to V _{CC}	-1.0	—	1.0	μA
Output Leakage Current	I _{LO}	CE = V _{IL} or $\overline{LB}, \overline{UB} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{OUT} = 0 to V _{CC}	-1.0	—	1.0	μA
Output High Voltage	V _{OH}	I _{OH} = -100 μA	V _{CC} - 0.2	—	—	V
Output Low Voltage	V _{OL}	I _{OL} = 100 μA	—	—	0.2	V
Standby Power Supply Current	I _{CCS}	$\overline{LB}, \overline{UB} \geq V_{CC} - 0.2 V$, CE ≥ V _{CC} - 0.2 V or 0 V ≤ CE ≤ 0.2 V, V _{IN} = 0 to V _{CC}	—	—	20	μA
	I _{CCS1}	$\overline{LB}, \overline{UB} = V_{IH}$ or CE = V _{IL}	—	—	0.6	mA
Operating Power Supply Current	I _{CCA}	$\overline{LB}, \overline{UB} = V_{IL}$, CE = V _{IH} , V _{IN} = V _{IH} / V _{IL} , T _{CYC} = Min. cycle, I _{OUT} = 0 mA	—	—	①	mA
		$\overline{LB}, \overline{UB} \leq 0.2 V$, CE ≥ V _{CC} - 0.2 V, V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V, T _{CYC} = 1 μs, I _{OUT} = 0 mA	—	—	15	mA

① 52V1017LL-85 60 mA
52V1017LL-10 50 mA
52V1017LL-12 40 mA

AC Characteristics

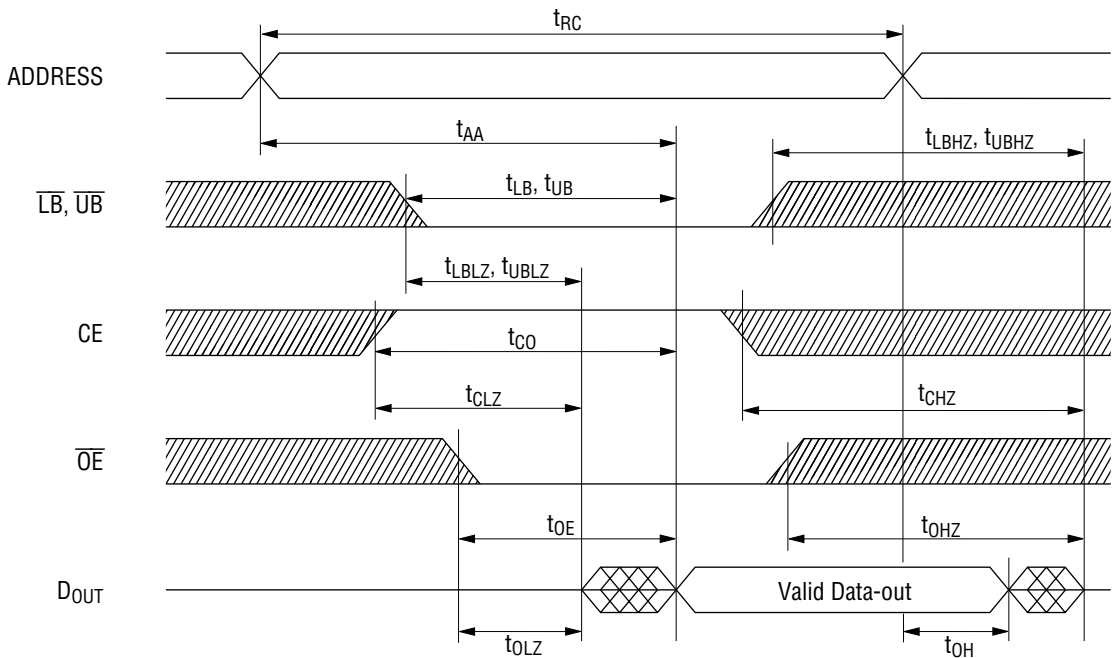
Test Conditions

Parameter	Condition
Input Pulse Level	V _{IH} = 2.4 V, V _{IL} = 0.4 V
Input Rise and Fall Times	5 ns
Input/Output Timing Level	1.4 V
Output Load	C _L = 100 pF, 1 LVCMOS

Read Cycle

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $T_a = 0^\circ\text{C to }70^\circ\text{C}$)

Parameter	Symbol	MSM52V1017LL-85		MSM52V1017LL-10		MSM52V1017LL-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85	—	100	—	120	—	ns
Address Access Time	t_{AA}	—	85	—	100	—	120	ns
\overline{LB} , \overline{UB} Access Time	t_{LB}	—	85	—	100	—	120	ns
	t_{UB}	—	85	—	100	—	120	
CE Access Time	t_{CO}	—	85	—	100	—	120	ns
\overline{OE} Access Time	t_{OE}	—	45	—	50	—	60	ns
\overline{LB} , \overline{UB} to Output in Low-Z	t_{LBLEZ}	10	—	10	—	10	—	ns
	t_{UBLEZ}	10	—	10	—	10	—	
CE to Output in Low-Z	t_{CLEZ}	10	—	10	—	10	—	ns
\overline{OE} to Output in Low-Z	t_{OLEZ}	5	—	5	—	5	—	ns
\overline{LB} , \overline{UB} to Output in High-Z	t_{LBHZ}	—	30	—	35	—	35	ns
	t_{UBHZ}	—	30	—	35	—	35	
CE to Output in High-Z	t_{CHZ}	—	30	—	35	—	35	ns
\overline{OE} to Output in High-Z	t_{OHZ}	—	30	—	35	—	35	ns
Output Hold Time from Address Change	t_{OH}	10	—	10	—	10	—	ns

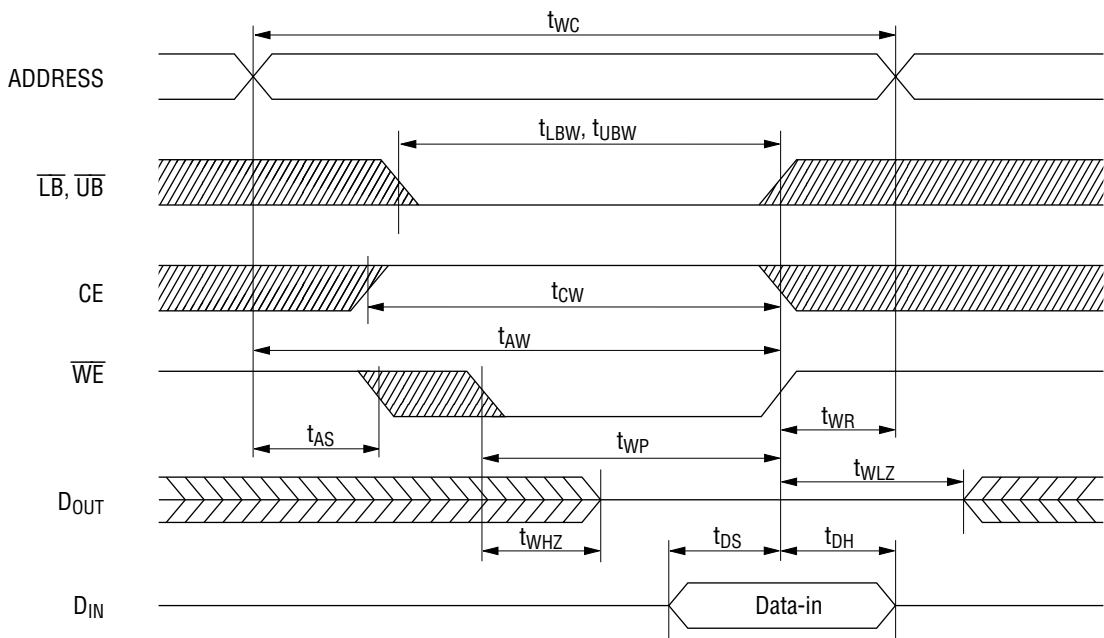


- Notes:
1. A read cycle occurs during the overlap of $\overline{LB} = "L"$ (or $\overline{UB} = "L"$), $CE = "H"$, $\overline{OE} = "L"$ and $\overline{WE} = "H"$.
 2. t_{LBHZ} , t_{UBHZ} , t_{CHZ} and t_{OHZ} are specified by the time when DATA is floating, not defined by the output level.

Write Cycle

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $T_a = 0^\circ\text{C to }70^\circ\text{C}$)

Parameter	Symbol	MSM52V1017LL-85		MSM52V1017LL-10		MSM52V1017LL-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85	—	100	—	120	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	65	—	75	—	90	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	5	—	ns
Data Setup Time	t_{DS}	35	—	40	—	50	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
\overline{LB} , \overline{UB} to End of Write	t_{LBW}	75	—	90	—	100	—	ns
	t_{UBW}	75	—	90	—	100	—	
CE to End of Write	t_{CW}	75	—	90	—	100	—	ns
Address Valid to End of Write	t_{AW}	75	—	90	—	100	—	ns
\overline{WE} to Output in High-Z	t_{WHZ}	—	30	—	35	—	35	ns
Output Active from End of Write	t_{WLZ}	5	—	5	—	5	—	ns



- Notes:
1. A write cycle occurs during the overlap of $\overline{LB} = "L"$ (or $\overline{UB} = "L"$), $CE = "H"$ and $\overline{WE} = "L"$.
 2. \overline{OE} may be either of "H" or "L" in the write cycle.
 3. t_{AS} is specified from $\overline{LB} = "L"$ (or $\overline{UB} = "L"$), $CE = "H"$ or $\overline{WE} = "L"$, whichever occurs last.
 4. t_{WP} is an overlap time of $\overline{LB} = "L"$ (or $\overline{UB} = "L"$), $CE = "H"$ and $\overline{WE} = "L"$.
 5. t_{WR} , t_{DS} and t_{DH} are specified from $\overline{LB} = "H"$ (or $\overline{UB} = "H"$), $CE = "L"$ or $\overline{WE} = "H"$, whichever occurs first.
 6. t_{WHZ} is specified by the time when DATA output is floating, not defined by the output level.
 7. When I/O pins are in the output mode, don't apply the inverted input signal to the output pins.

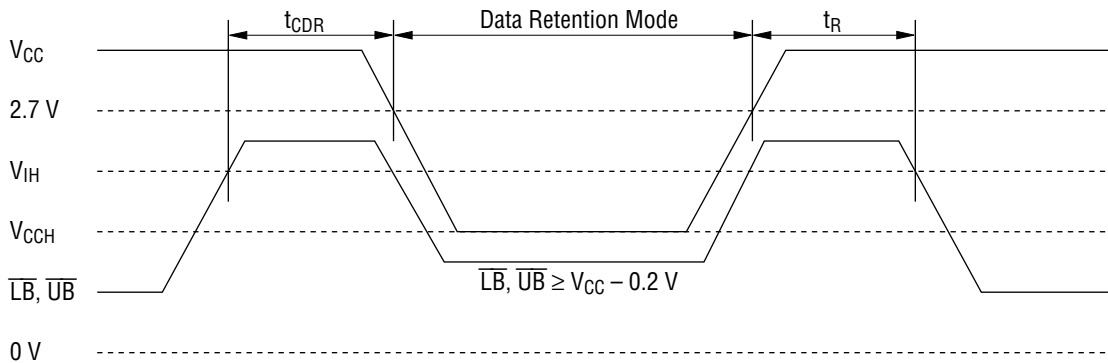
Data Retention Characteristics

(Ta = 0°C to 70°C)

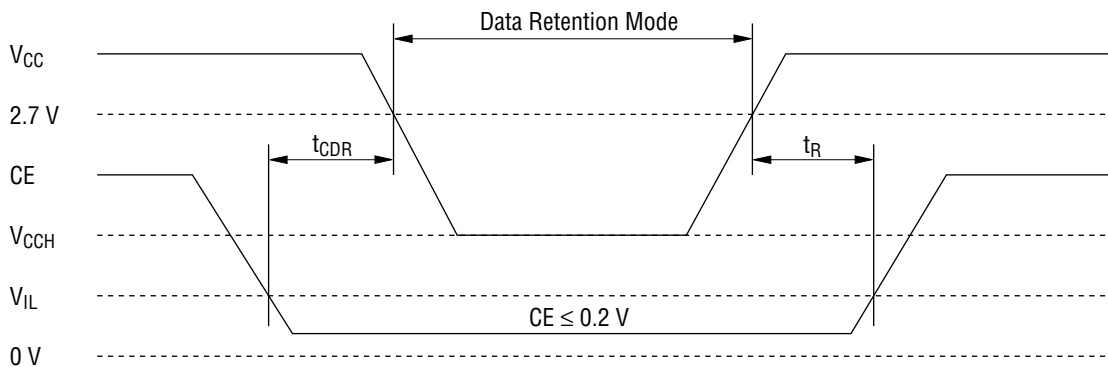
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data Retention Power Supply Voltage	V _{CCH}	$\overline{LB}, \overline{UB} \geq V_{CC} - 0.2 V,$ $CE \geq V_{CC} - 0.2 V$ or $0 V \leq CE \leq 0.2 V,$ $V_{IN} = 0 \text{ to } V_{CC}$	2.0	—	—	V
Data Retention Power Supply Current	I _{CCH}	$V_{CC} = 3 V,$ $\overline{LB}, \overline{UB} \geq V_{CC} - 0.2 V,$ $CE \geq V_{CC} - 0.2 V$ or $0 V \leq CE \leq 0.2 V,$ $V_{IN} = 0 \text{ to } V_{CC}$	—	—	15*	μA
Chip Deselect to Data Retention Time	t _{CDR}	—	0	—	—	ns
Operation Recovery Time	t _R	—	5	—	—	ms

* 4 μA Max. when Ta = 0°C to 40°C.

$\overline{LB}, \overline{UB}$ Control

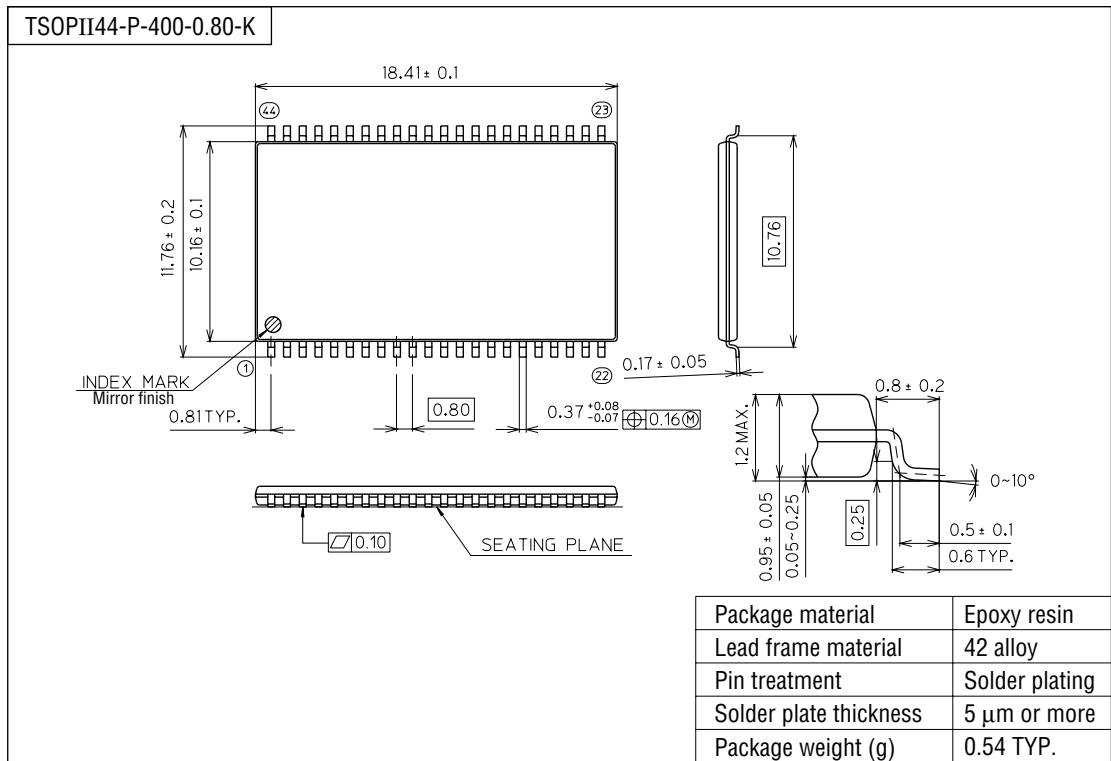


CE Control



PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).