MN5814

TFT AV Panel Controller IC

■ Overview

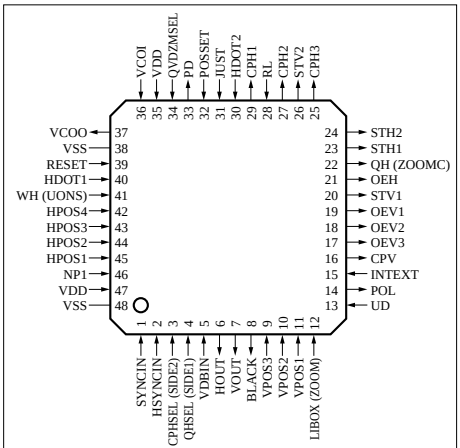
The MN5814 is a TFT LCD panel timing controller IC.

■ Features

- Supports both composite sync and separate sync signal video inputs.
- Horizontal and vertical position adjustment function
  - Horizontal: 5 bits (Adjustment range: 9.38 µs)
  - Vertical: 4 bits (Adjustment range: 14 H)
- Supports multiple panel types
  - From 2.5-type to 7-type wide-screen panels
  - For wide-screen panels:
    - Display with black side bands (3 modes)
    - Just-fit display
    - Zoom (2 modes)
- Switching between PAL and NTSC (PAL: decimation only)
- Underside on-screen display (UONS)
- An optimal zooming mode is possible according to the display panel through 2-zooming mode of ZOOM1 and ZOOM2.
- UONS display at arbitrary positions is possible by the black side control pins.
  Also provides full-screen black side display.

■ Applications

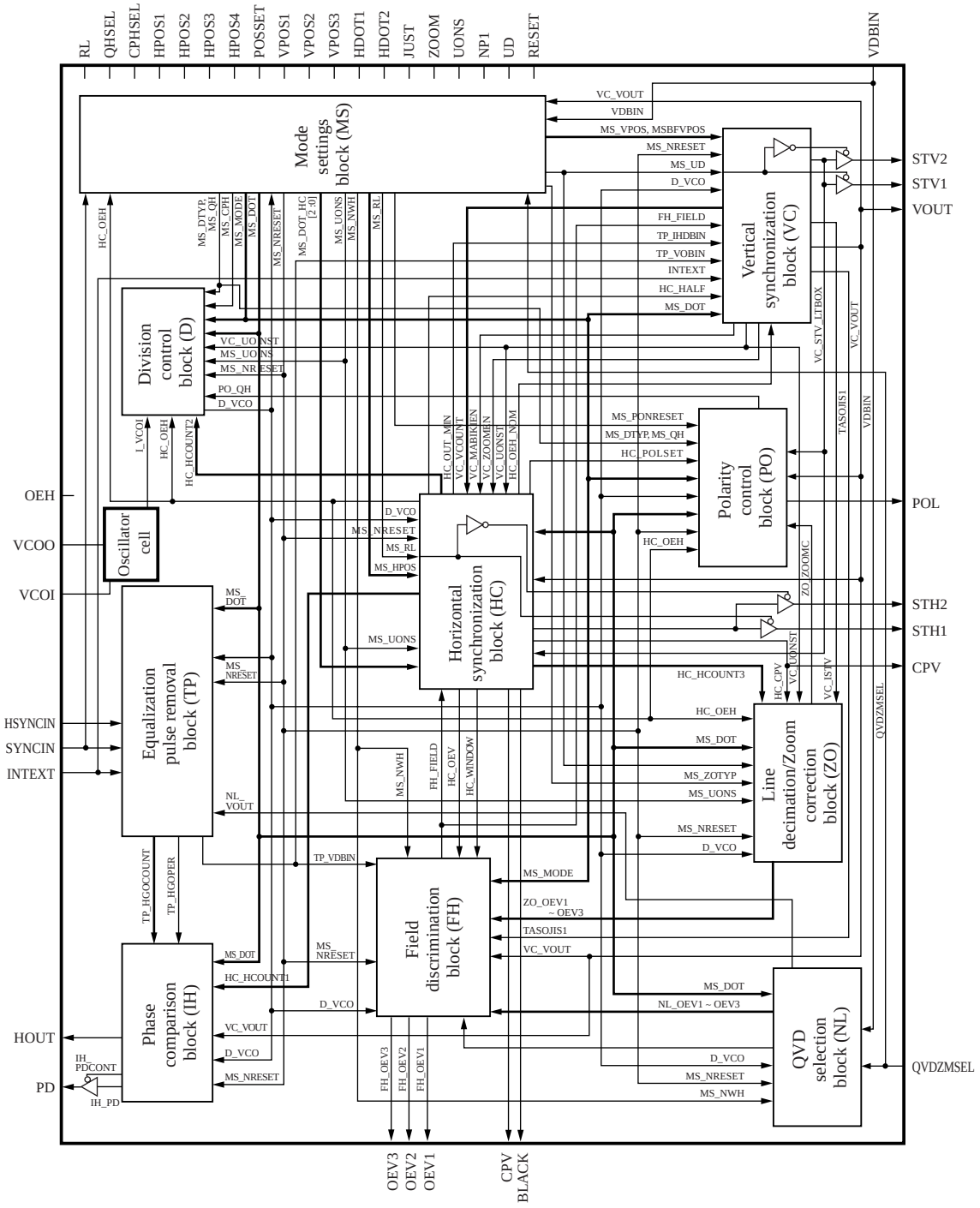
- TFT LCD panels



(TOP VIEW)

Note: Pin names in parentheses apply for use with the 1,200 and 1,440 stripe panel types.

■ Block Diagram



■ Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	SYNCIN	I	Composite sync input
2	HSYNCIN	I	Horizontal sync input (separate)
3	CPHSEL (SIDE2)	I	In 1,440 or 1,200-stripe mode: Black side and just-fit control In 960-stripe mode: Disabled In 480 or 960-delta mode: CPH pulse phase switching
4	QHSEL (SIDE1)	I	In 1,440 or 1,200-stripe mode: Black side and just-fit control In 960-stripe mode: Disabled In 480 or 960-delta mode: QH pulse phase switching
5	VDBIN	I	Vertical sync input (separate)
6	HOUT	O	Horizontal sync output
7	VOUT	O	Vertical sync output
8	BLACK	O	Black signal output
9	VPOS3	I	Vertical display position switching (STV1 and STV2 position switching)
10	VPOS2	I	
11	VPOS1	I	
12	LTBOX (ZOOM)	I	High: Zoom or letterbox display In 1,440 or 1,200-mode: Zoom display control In 480 or 960-delta or 960-stripe mode: Letterbox display control
13	UD	1	Up/down scan direction switching (STV1 and STV2 output switching)
14	POL	O	Video, opposite electrode reversal signal
15	INTEXT	I	Composite/separate input switching
16	CPV	O	Gate driver IC clock
17	OEV3	O	Gate driver IC output stage enable pulse signals
18	OEV2	O	
19	OEV1	O	
20	STV1	O	Gate driver IC start pulse 1
21	OEH	O	Source driver IC output stage enable pulse signal
22	QH (ZOOMC)	O	In 480 or 960-delta mode: Color arrangement switching pulse In 1,200 or 1,440-mode: Zoom control pulse In 960 stripe mode: Fixed low-level output
23	STH1	O	Source driver IC start pulse 1
24	STH2	O	Source driver IC start pulse 2
25	CPH3	O	Source driver IC clock 3
26	STV2	O	Source driver IC start pulse 2
27	CPH2	O	Source driver IC clock 2
28	RL	I	Left/right scan direction switching (STH1 and STH2 output switching)

■ Pin Descriptions (continued)

Pin No.	Pin Name	I/O	Description
29	CPH1	O	Source driver IC clock 1
30	HDOT2	I	Display pixel count mode switch 2
31	JUST	I	In 1,200 or 1,440-mode: Just-fit display switching In 960-mode: Stripe/delta control
32	POSSET	I	Horizontal/vertical display position offset switching
33	PD	O	Phase comparator output
34	QVDZMSEL	I	In 480 or 960-delta or stripe mode: QVD input In 1,200 or 1,400-mode: Zoom 1/zoom 2 display switching OEV pulse control in zoom mode
35	VDD	I	Power supply (VDD)
36	VCOI	I	VCO input (system clock input)
37	VCOO	O	VCO output
38	VSS	I	Ground (GND)
39	RESET	I	System reset
40	HDOT1	I	Display pixel count mode switching 1
41	WH (UONS)	I	In 1,200 or 1,440-mode: "Under on-screen" display control In 480 or 960-delta or stripe mode: WH (write/hold) control
42	HPOS4	I	Horizontal display position switching signals (STH1 and STH2 position switching)
43	HPOS3	I	
44	HPOS2	I	
45	HPOS1	I	
46	NP1	I	NTSC/PAL switching
47	VDD	I	Power supply (VDD)
48	VSS	I	Ground (GND)

■ Electrical Characteristics

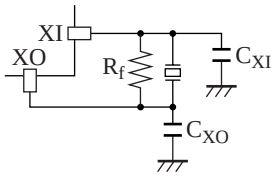
1. Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	– 0.3 to +4.6	V
Input pin voltage	V_I	– 0.3 to V_{DD}+0.3	V
Output pin voltage	V_O	– 0.3 to V_{DD}+0.3	V
Output current (HL2 pins)	I_O	±6	mA
Output current (HL4 pins)	I_O	±12	mA
Power dissipation	P_D	330	mW
Operating temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +150	°C

Note) 1. HL2 pins: QH, CPV, OEH, OEV1 to OEV3, POL, STH1, STH2, STV1, STV2, HOUT, VOUT, BLACK
HL4 pins: PD, CPH1 to CPH3
2. The absolute maximum ratings are limit values for stresses applied to the chip so that the chip will not be destroyed. Operation is not guaranteed within these ranges.
3. All the VDD and VSS pins must be connected externally to the corresponding power or ground.
4. The power dissipation rating applies at T_{opr} = 85°C when the MN5814 is mounted on a glass-epoxy printed circuit board. The actual value differs depending on the printed circuit board used and the thermal conditions in the end product.

2. Recommended Operating Conditions at V_{SS} = 0 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage	V_{DD}		2.7	3.3	3.6	V
Ambient temperature	T_a		–40	—	85	°C
Input rise time	t_r		0	—	100	ns
Input fall time	t_f		0	—	100	ns
Oscillator frequency	$f_{OSC}1$	30 MHz Xtal	—	30	—	MHz
Recommended values for external capacitors	$C_{XI}90$ $C_{XO}90$	V_{DD} = 3.3 V, with an external feedback resistor	—	33 (15 MHz to 25 MHz)	—	pF
			—	10 (25 MHz to 40 MHz)	—	
Recommended values for external resistors	R_f90	$V_I = V_{DD}$ or V_{SS} , V_{DD} = 3.3 V	—	2.2	—	kΩ



Note) Since the oscillator characteristics differ depending on the oscillator element used and the external capacitor conditions, consult the manufacturer of the oscillator element to determine the optimal oscillator circuit.

■ Electrical Characteristics (continued)

3. Electrical Characteristics at V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0 V, f_{TEST} = 30 MHz, T_a = -40°C to +85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Quiescent supply current	I_{DDS}	V_I (pulled-up pins) = OPEN, V_I (pulled-down pins) = OPEN, V_I (XI) = V_{DD} *, With either the V_{DD} or the V_{SS} level applied simultaneously to all of the other input pins and I/O pins in the high-impedance state.	—	—	500	µA
Operating supply current	I_{DDO}	$V_I = V_{DD}$ or V_{SS} , f = 30 MHz, V_{DD} = 3.3 V, outputs open	—	15	30	mA
1) CMOS input level Schmitt trigger pins: RESET, VDBIN, SYNCIN, HSYNCIN						
Input threshold voltage	VT+	V_{DD} = 2.7 V to 3.6 V	—	1.85	$V_{DD} \times 0.7$	V
	VT–		$V_{DD} \times 0.3$	1.45	—	
Input leakage current	I_{LI}	$V_I = V_{DD}$ or V_{SS}	—	—	±5	µA
2) CMOS input level pins with built-in pull-up resistor: RL, UD, HDOT1, HDOT2, INTEXT						
High-level input voltage	V_{IH}		$V_{DD} \times 0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.3$	V
Pull-up resistor	R_{IH}	V_I = 0 V	33	100	318	kΩ
Input leakage current	I_{LIH}	$V_I = V_{DD}$	—	—	±10	µA
3) CMOS input level pins with built-in pull-down resistor: NP1, HPOS1 to HPOS4, JUST, UONS, VPOS1 to VPOS3, ZOOM, QHSEL, CPHSEL, POSSET, QVDZMSEL						
High-level input voltage	V_{IH}		$V_{DD} \times 0.7$	—	V_{DD}	V
Low-level input voltage	V_{IL}		0	—	$V_{DD} \times 0.3$	V
Pull-down resistor	R_{IL}	$V_I = V_{DD}$	33	100	318	kΩ
Input leakage current	I_{LIL}	$V_I = V_{SS}$	—	—	±10	µA
4) Push-pull output pins: QH, CPV, OEH, OEV1 to OEV3, POL, HOUT, VOUT, BLACK						
High-level output voltage	V_{OH}	I_{OH} = –1.9 mA, $V_I = V_{DD}$ or V_{SS}	V_{DD} – 0.6	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1.9 mA, $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
5) Push-pull output pins: CPH1 to CPH3						
High-level output voltage	V_{OH}	I_{OH} = –3.8 mA, $V_I = V_{DD}$ or V_{SS}	V_{DD} – 0.6	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 3.8 mA, $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V

Note) *: The I_{DDS} associated with the V_{DD} applied to the oscillator pin XI shall be take from a power supply separate from the measured power supply.

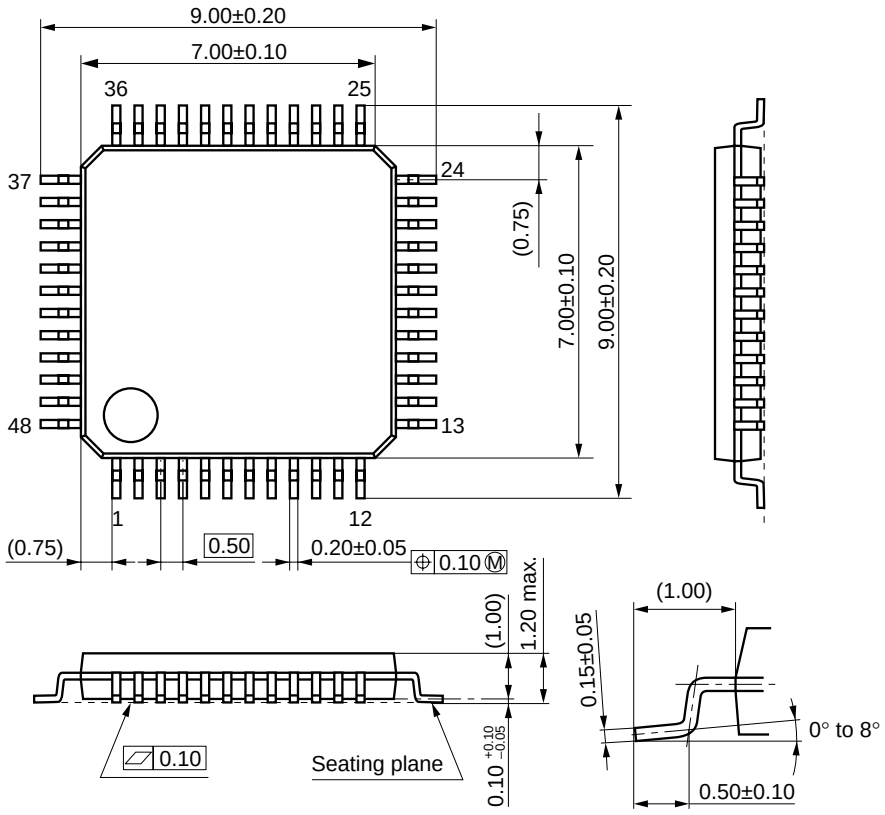
■ Electrical Characteristics (continued)

3. Electrical Characteristics at V_{DD} = 2.7 V to 3.6 V, V_{SS} = 0 V, f_{TEST} = 30 MHz, T_a = -40°C to +85°C (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
6) Tristate output pins: STH1, STH2, STV1, STV2						
High-level output voltage	V_{OH}	I_{OH} = –1.9 mA, $V_I = V_{DD}$ or V_{SS}	V_{DD} – 0.6	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1.9 mA, $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage current	I_{LO}	V_O = High-impedance state, $V_I = V_{DD}$ or V_{SS} , $V_O = V_{DD}$ or V_{SS}	—	—	±5	µA
7) Tristate output pins: PD						
High-level output voltage	V_{OH}	I_{OH} = –3.8 mA, $V_I = V_{DD}$ or V_{SS}	V_{DD} – 0.6	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 3.8 mA, $V_I = V_{DD}$ or V_{SS}	—	—	0.4	V
Output leakage current	I_{LO}	V_O = High-impedance state, $V_I = V_{DD}$ or V_{SS} , $V_O = V_{DD}$ or V_{SS}	—	—	±5	µA

■ Package Dimensions (Units: mm)

• TQFP048-P-0707B



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