CMOS 4-BIT MICROCONTROLLER

TMP47C407AN
TMP47C407AF

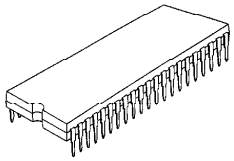
The 47C407A is a high performance 4-bit single chip microcomputer based on the TLCS-47 CMOS series with a DTMF generator and a large-capacity RAM for repertory dialing applications, and which is suitable for utilization in telephones.

PART No.	ROM	RAM	PACKAGE	OTP version
TMP47C407AN	4096 × 8-bit	768 × 4-bit	SDIP42-P-600-1.78	TMP47P407AN
TMP47C407AF			QFP44-P-1414-0.80D	TMP47P407AF

FEATURES

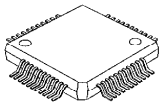
- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 2.1μs (at 3.84MHz)
- ◆Low voltage operation : 2.7V min.
- ◆90 basic instructions
- ◆Table look-up instructions
- ◆Subroutine nesting : 15 levels max.
- ◆5 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port (35 pins)
  - Input 2ports 5pins
  - Output 1port 3pins
  - I/O 7ports 27pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurment mode
- ◆Serial Interface with 4-bit buffer
  External/internal clock, leading/trailing edge shift mode
- ◆DTMF (Dual Tone Multi Frequency) Output
  - DTMF output with one instruction
  - Single tone output function
- ◆RAM for repertory dial : 768 × 4 bit max.
- ◆BEEP output function
- ◆Hold function
  - Battery/Capacitor back-up
  - Hold function controlled by port K0.
- ◆Real Time Emulator : BM47215B

SDIP42-P-600-1.78



TMP47C407AN
TMP47P407AN

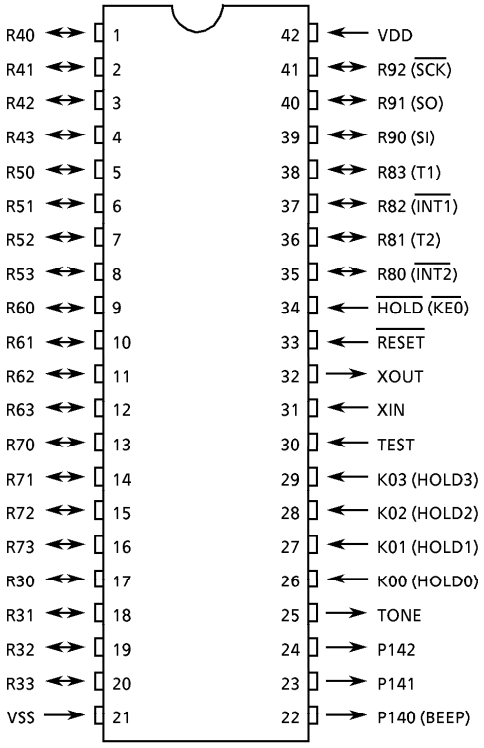
QFP44-P-1414-0.80D



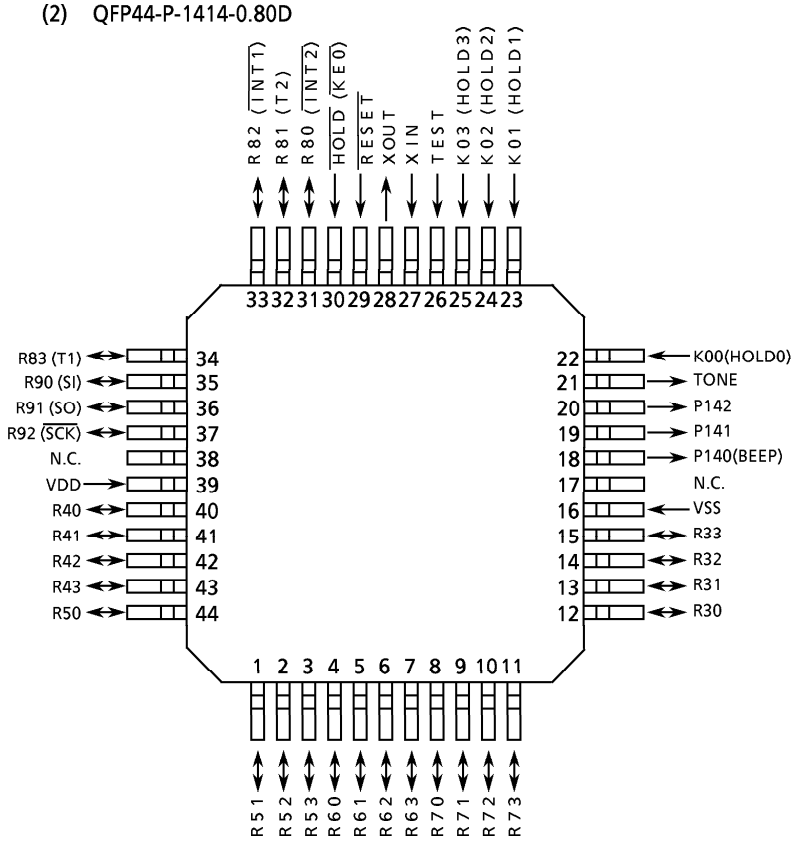
TMP47C407AF
TMP47P407AF

PIN ASSIGNMENT (TOP VIEW)

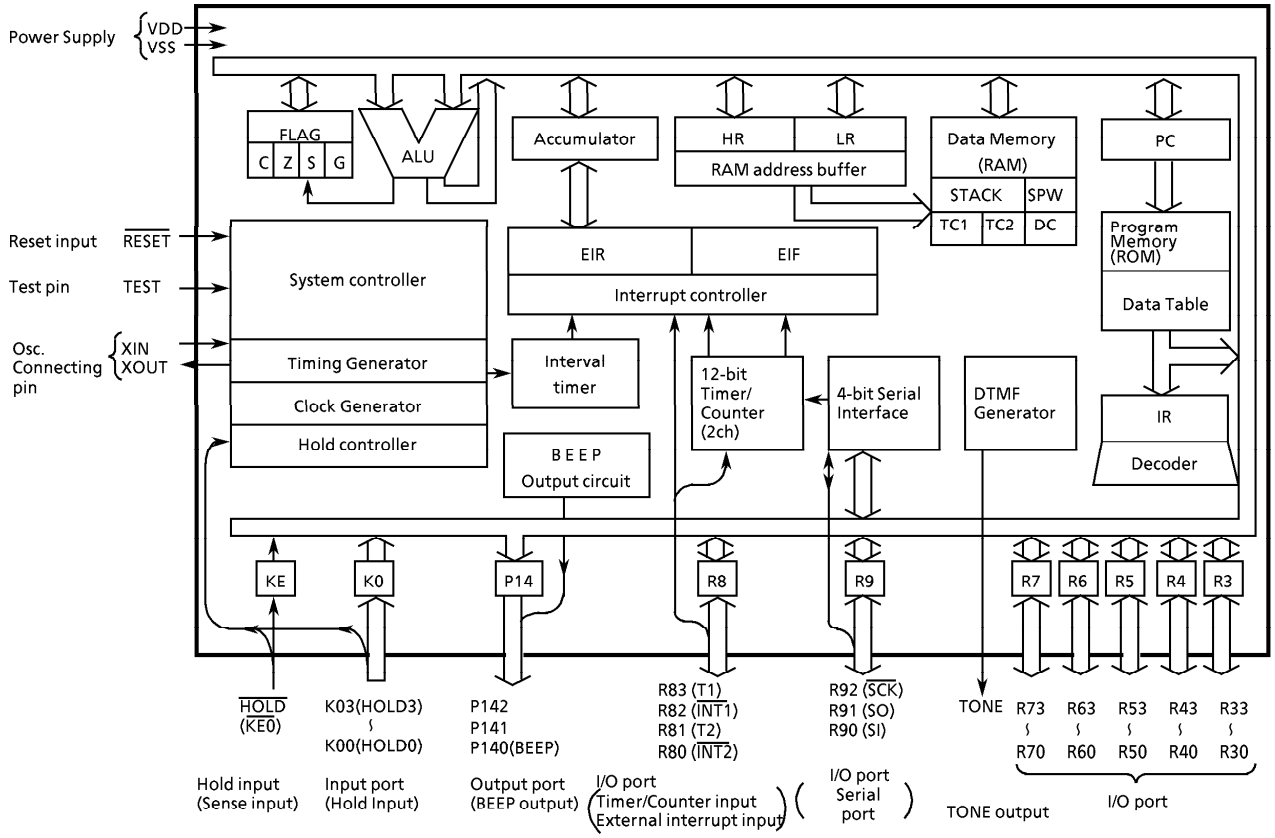
(1) SDIP42-P-600-1.78



(2) QFP44-P-1414-0.80D



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 (HOLD3) - K00 (HOLD0)	Input (Input)	4-bit input port	Hold request/release signal input (Active "H")
R33 - R30	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R43 - R40			
R53 - R50			
R63 - R60			
R73 - R70			
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/Counter 1 external input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
P142 - P141	Output	3-bit output port with latch	
P140 (BEEP)	Output (Output)		BEEP Output
TONE	Output	Tone output	
XIN	Input	Resonator connecting pins.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 2.7V to 6.0V	
VSS		0V(GND)	

OPERATIONAL DESCRIPTION

Concerning the 47C407A the configuration and functions of hardwares are described. As the description has been provided with priority on those parts differing from the 47C452B, the technical data sheets for the 47C452B shall also be referred to.

1. SYSTEM CONFIGURATION

(1) CPU Core Function

The functions are the same as those of the 47C452B.

(2) Peripheral Hardware Functions

① I/O Port
② Interval Timer
③ Timer/Counter
④ DTMF Generator
⑤ BEEP Output Circuit
⑥ Serial Interface

The following are explanations of functions ⑤ which have been added to the 47C454A or which are different from those of the 47C452B and DTMF Generator, I/O Port.

2. CPU CORE FUNCTIONS

2.1 DATA MEMORY

The 47C858 has a total of 768 × 4bits of data memory. This memory is same as the data memory built into the 47C407A, so refer to the technical data sheets for the 47C407A for an explanation of the operation.

2.2 Hold Operating Mode

The 47C407A has a $\overline{\text{HOLD}}$ pin and K0 port as hold control pins. Therefore, in the case of K0 port for Key inputs, the hold mode can be released by key inputs. Figure 4-1 shows the hold control circuit of the 47C407A. Hold operating mode of the 47C407A is same as the 47C452B, excepting those aforementioned. For details, refer to the technical data sheets for the 47C452B.

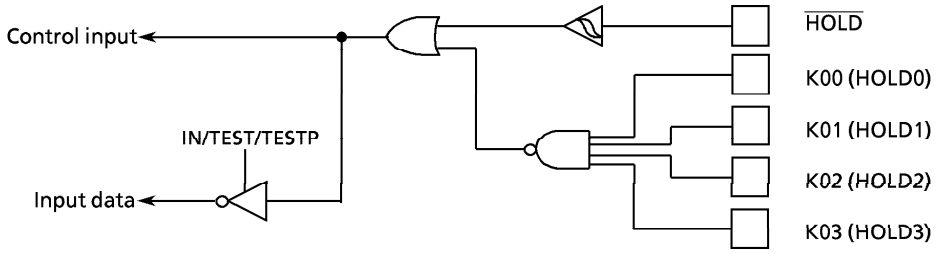


Figure 2-1. Hold control circuit

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O Ports

The 47C407A has 7 ports (27 pins) each as follows:

①	K0	;	4-bit input (shared with hold request/release signal input)
②	R3	;	4-bit input/output
③	R4, R5, R6, R7	;	4-bit input/output
④	R8	;	4-bit input/output (shared with external interrupt input and timer/counter input)
⑤	R9	;	3-bit input/output (shared with serial port)
⑥	P14	;	2-bit output (P140 is shared with BEEP output)
⑦	KE	;	1-bit sense input (shared with hold request/release signal input)

The 47C407A does not have the port P1 and P2.

Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port K0 (K03 - K00)

The 4-bit input port with pull-up resistors, shared by hold request/release signal input.

port K0 (Port address IP00)

3	2	1	0
K03 (HOLD3)	K02 (HOLD2)	K01 (HOLD1)	K00 (HOLD0)

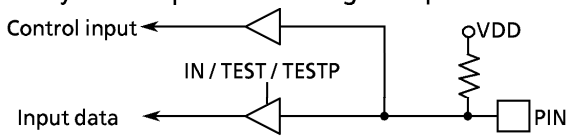


Figure 3-1. Port K0

(2) Port R3 (R33 - R30)

The 4-bit I/O port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset.

port R3 (Port address OP03/IP03)

3	2	1	0
R33	R32	R31	R30

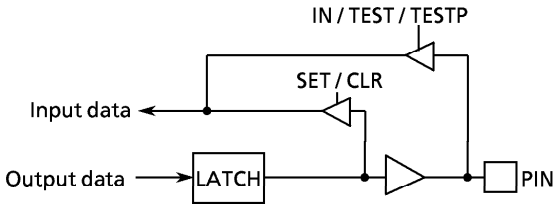


Figure 3-2. Port R3

(3) P14 (P142 - P140)

The 2-bit output port with latch. The latch is initialized to "1" during reset. The pin P140 is shared by the BEEP output. When used as the BEEP output, the latch must be set to "1".

port P14 (Port address OP14)

3	2	1	0
	P142	P141	P140 (BEEP)

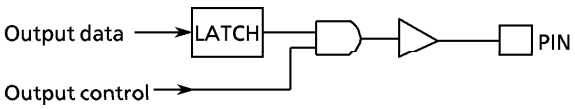


Figure 3-3. Port P14

Port address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	ROW register	ROW register	○	○	○	○ *Note2*	○	○	–
02	COLUMN register	COLUMN register	○	○	○	○	○	○	–
03	R3 input port	R3 output port	○	○	○	–	○	○	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	RAM address register	RAM address register	○	○	○	–	○	○	–
0B	RAM address register	RAM address register	○	○	○	–	○	○	–
0C	RAM data buffer register	RAM data buffer register	○	○	○	–	○	○	–
0D	RAM command register	RAM command register	○	○	○	–	–	○	–
0E	SIO, hold status	——	○	–	–	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operation mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	RAM address register	–	○	–	–	–	–	–
13	Undefined	BEEP output control	–	○	–	–	–	–	–
14	Undefined	P14 output port (BEEP output)	–	○	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	——	–	–	–	–	–	–	–
18	Undefined	——	–	–	–	–	–	–	–
19	Undefined	Interval timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer/counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/counter 2 control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	Serial interface control	–	○	–	–	–	–	–

Note 1. "——" means the reserved state. Unavailable for the user programs.

Note 2. The 5-bit to 8-bit data conversion instruction [OUTB @HL] , automatic access to ROW register and COLUMN register.

Table 3-1. Port Address Assignments and Available I/O Instructions

3.2 DTMF Generator

The 47C407A has built-in DTMF generator which generates dialing signals for tone dialing type telephones. There are two groups of tone dial signals, one group of 4 sine wave low frequencies and another group of 4 sine wave high frequencies. All of these frequencies can be selected individually and combined with a frequency from the other group for a total of 16 different DTMF composite waves.

(DTMF ; Dual Tone Multi Frequency)

3.2.1 Configuration of DTMF Generator

Figure 3-4 shows the DTMF generator configuration. The 47C407A generates two stepped, quasi sine waves for tone dial signals which can be combined and output. The high or low group of frequencies is selected by setting frequency selection codes into the ROW and COLUMN registers.

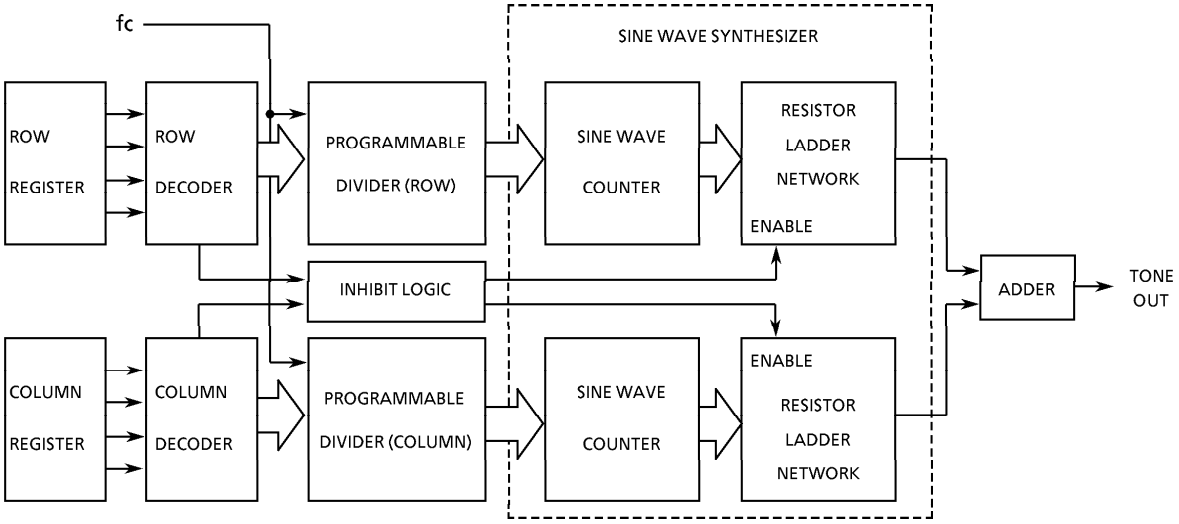


Figure 3-4. Configuration of DTMF Generator

3.2.2 Control of DTMF Generator

Tone output is controlled by ROW register (OP01/IP01) and COLUMN register (OP02/IP02). And single tone is controlled by TONE command register (OP0D/IP0D). ROW register, COLUMN register and TONE command register are initialized to "0" during the reset.

TONE command register (Port address OP0D/IP0D)

3	2	1	0
STE		(R / W)	(CE)

(Initial value 0*00)

STE	Controls single tone output

0 : Disable mode of single tone output

1 : Enable mode of single tone output

*Note 1. * ; don't care*

Note 2. When read STE bit, "1" is always read.

Figure 3-5. TONE Command Register

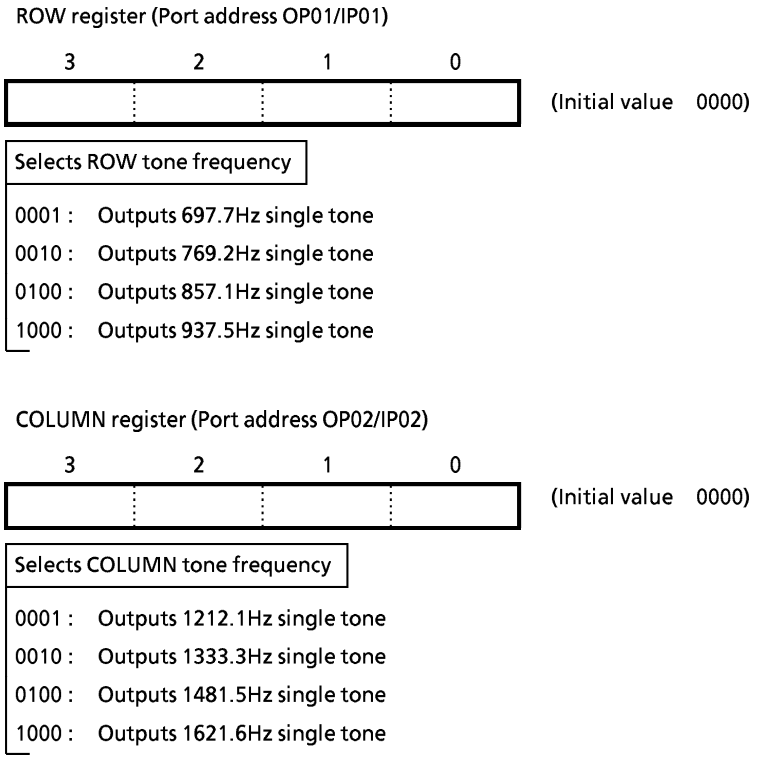


Figure 3-6. ROW, COLUMN Register

Tones are outputted by loading the frequency selection codes shown in Figure 3-6 into the ROW and COLUMN registers. In the enable mode of single tone output, either ROW or COLUMN register is disabled, another register remains to be enabled, and so single tone can be outputted, by loading an ineffective code into the register. When both the registers are enabled, dual tone can be outputted. In the disable mode of single tone output, effective codes are loaded into both ROW and COLUMN registers and then dual tone can be outputted. At this time, an ineffective code is loaded into ROW or COLUMN register and then the 47C407A has no tone output signal.
The [OUTB @HL] instruction can set 8-bit data into both registers (the upper 4 bits of the ROM data go to the COLUMN register and the lower 4 bits go to the ROW register) at the same time, and DTMF signal is outputted without single tone output.

Example 1: To output 1481. 5Hz single tone

```
OUT     #8, %OP0D       ; Sets the enable mode of single tone output
OUT     #0, %OP01       ; Sets an ineffective code into ROW register
OUT     #4, %OP02       ; Sets data "4" into COLUMN register
```

Example 2: 8 bits of data corresponding to the 5 bits of data linking the content of carry flag and the contents of data memory RAM address 90_H are read from the ROM, frequency selection codes are loaded into ROW and COLUMN registers, and dual tone is outputted.

```
LD      HL, #90H        ; HL←90H(Sets the address of the data memory)
OUTB    @HL             ; Sets the ROM data into the ROW and COLUMN
                          register
```

Table 3-2 shows the corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys. Table 3-3 shows the deviation between the 47C407A tone output frequency and standard frequency.

		COLUMN register (OP02 / IP02)		
	Frequency selection code	0001 (1209)	0010 (1336)	0100 (1477)
ROW register (OP01 / IP01)	0001 (697)	1	2	3
	0010 (770)	4	5	6
	0100 (852)	7	8	9
	1000 (941)	*	0	#
		Standard telephone dial key		

Contents of ( ) are standard frequencies, unit: Hz

Table 3-2. Corresponding frequency selection codes of the ROW and COLUMN registers for the telephone dial keys

ROW Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	697.7	697	+ 0.10
0	0	1	0	769.2	770	– 0.10
0	1	0	0	857.1	852	+ 0.60
1	0	0	0	937.5	941	– 0.37

COLUMN Tone						
Frequency selection code				Tone output frequency [Hz]	Standard frequency [Hz]	Deviation [%]
3	2	1	0			
0	0	0	1	1212.1	1209	+ 0.26
0	0	1	0	1333.3	1336	– 0.20
0	1	0	0	1481.5	1477	+ 0.30
1	0	0	0	1621.6	1633	– 0.70

Table 3-3. Tone output frequencies and Deviation from standard

3.2.3 Test mode for tone output

The 47C407A includes a test mode for checking tone output waveforms. Tones can be outputted by the circuit shown in figure 3-7. ROW data are inputted from the R6 port and COLUMN data are inputted from the R3 port, and any desired single or dual tones can be outputted by setting the selection codes shown in Figure 3-6. Figure 3-8 shows a single tone waveform and Figure 3-9 shows a dual tone waveform.

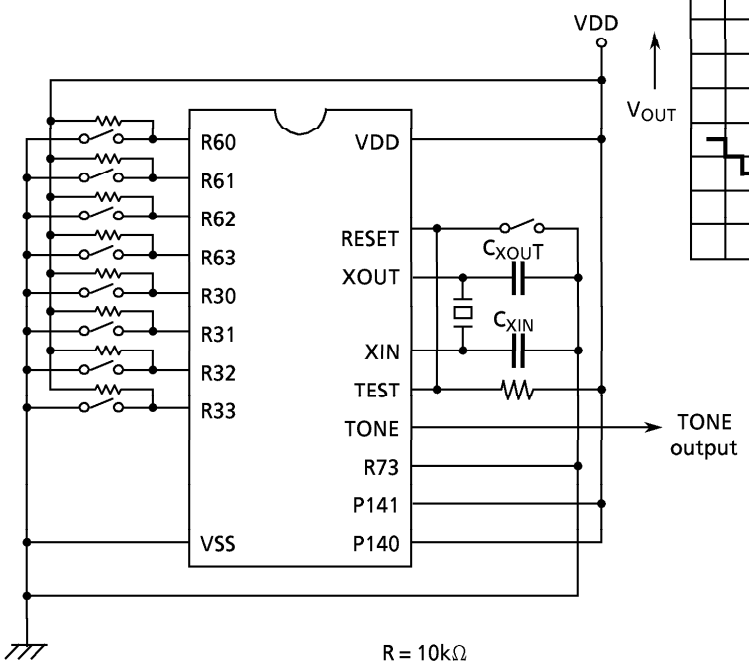


Figure 3-7. Tone test circuit

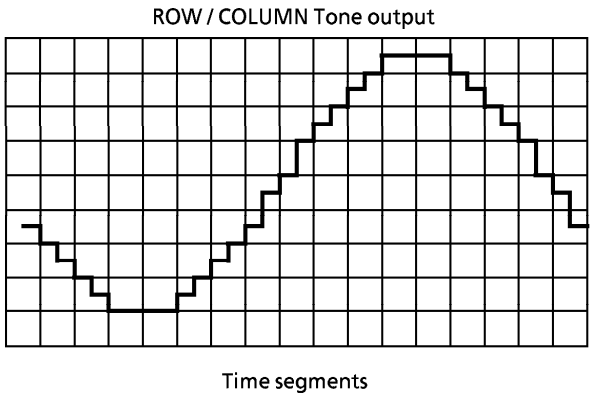


Figure 3-8. Single tone waveform

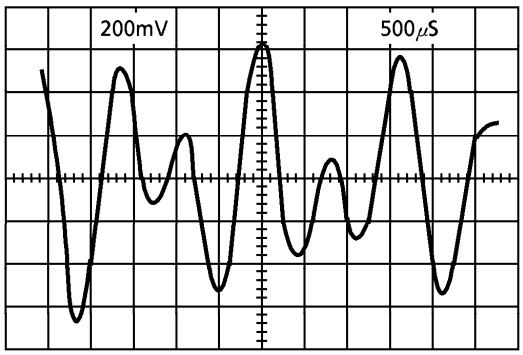


Figure 3-9. Dual tone waveform

3.3 BEEP Output Circuit

BEEP output circuit generates square wave in the audible frequency range. This circuit can drive the key input confirmation tone generator circuit for telephone applications.

BEEP output is from the P140 (BEEP) pin. This pin is for both P140 output and BEEP output. Set the P140 output latch to "1" for BEEP output.

3.3.1 BEEP Output Circuit Configuration

Figure 3-10 shows the BEEP output circuit configuration. The clock pulse of BEEP output circuit is supplied by an interval timer. BEEP output is controlled by frequency selection and output enable/disable setting.

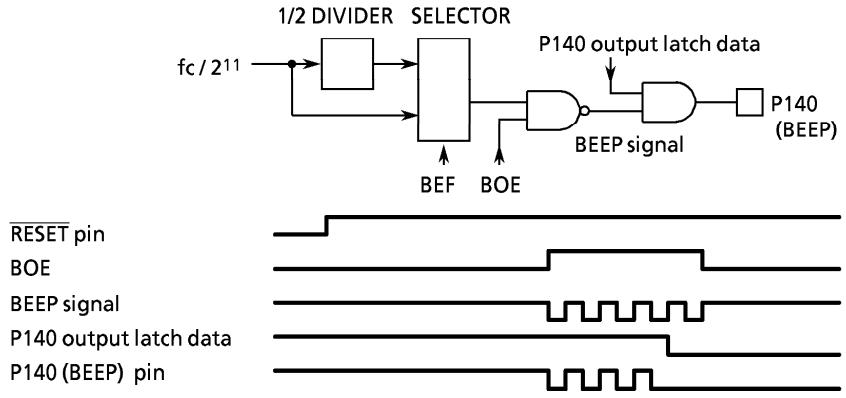


Figure 3-10. BEEP Output Circuit Configuration and Timing Chart

3.3.2 Control of BEEP Output

BEEP output is controlled with the BEEP output control command register (OP13).

BEEP Output Control command register (Port address OP13)

3	2	1	0
BOE			BEF

(Initial value 0**0)

BOE	Controls BEEP output
0 :	Disable output
1 :	Enable output

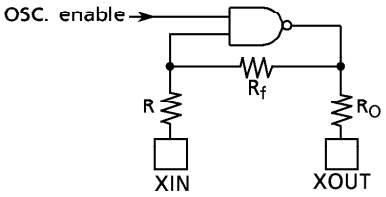
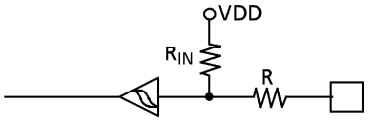
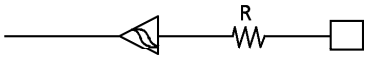
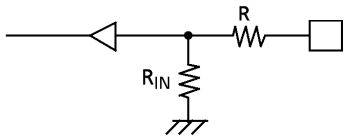
BEF	Selects BEEP output frequency	Example : At fc = 3.84MHz
0 : fc / 2^{11} [Hz]	·····	1875 [Hz]
1 : fc / 2^{12}	·····	937.5

Figure 3-11. BEEP Output Control command register

INPUT/OUTPUT CIRCUITRY

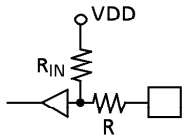
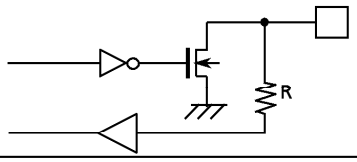
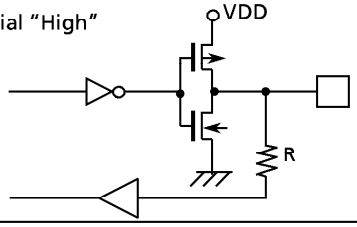
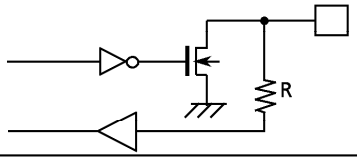
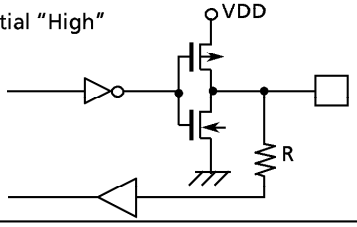
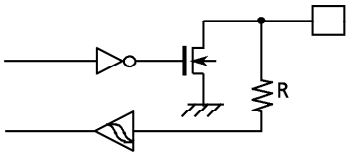
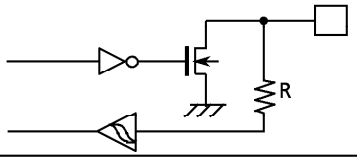
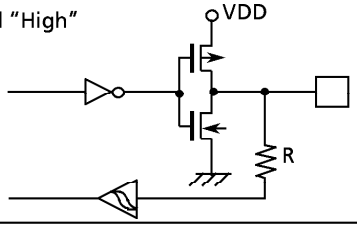
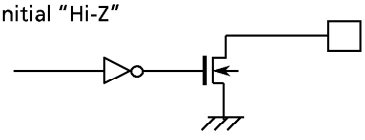
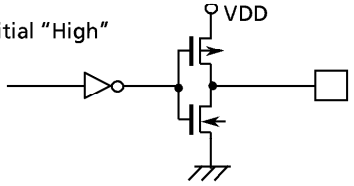
(1) Control pins

The input/output circuitries of the 47C407A control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins R = 1kΩ (typ.) R_f = 1.5MΩ (typ.) R_O = 2kΩ (typ.)
$\overline{\text{RESET}}$	Input		Hysteresis input Pull-up resistor R_{IN} = 220kΩ (typ.) R = 1kΩ (typ.)
$\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$)	Input (Input)		Hysteresis input (Sense input) R = 1kΩ (typ.)
TEST	Input		Pull-down resistor R_{IN} = 70kΩ (typ.) R = 1kΩ (typ.)

(2) I/O ports

The input/output circuitries of the 47C407A I/O ports are shown below, any one of the circuitries can be chosen by a code (WB, WE, WH) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input		Pull-up resistor R_{IN} = 70kΩ (typ.) R = 1kΩ (typ.)
R3 R4 R5 R6	I/O	WB: Initial "Hi-Z"  WE, WH: Initial "High" 	Sink open drain or push-pull output R = 1kΩ (typ.)
R7	I/O	WB, WE: Initial "Hi-Z"  WH: Initial "High" 	Sink open drain or push-pull output R = 1kΩ (typ.)
R8	I/O	Initial "Hi-Z" 	Sink open drain Hysteresis input R = 1kΩ (typ.)
R9	I/O	WB, WE: Initial "Hi-Z"  WH: Initial "High" 	Sink open drain or push-pull output Hysteresis input R = 1kΩ (typ.)
P14	Output	WB: Initial "Hi-Z"  WE, WH: Initial "High" 	Sink open drain or push-pull output

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin	– 0.3 to 10	
Output Current (per 1 pin)	I_{OUT}		3.2	mA
Power Dissipation (T_{opr} = 60°C)	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	T_{stg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 30 to 60	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	2.7	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc			3.84		MHz

D.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port, K0 TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Port R (open drain)					
Input Low Current	I_{IL}	Port R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Input Resistance	R_{IN1}	Port K0		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports P, R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output High Voltage	V_{OH}	Port R (push-pull)	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	V
Supply Current (in the Normal mode)	I_{DD}		Except TONE generating V_{DD} = 5.5V, fc = 3.84MHz	—	3	6	mA
	I_{DDT}		TONE generating V_{DD} = 5.5V, fc = 3.84MHz	—	5	10	
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V,	—	0.5	10	μA

Note 1. Typ values show those at T_{opr} = 25°C, V_{DD} = 5V

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the pull-up/pull-down resistor is contained.

Note 3. Supply Current ; V_{IN} = 5.3/0.2V
The K0 port is opened when the pull-up/pull-down resistor is contained.
The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

TONE OUTPUT CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 30 to 60°C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Tone Output Voltage (ROW)	V_{TONE}	RL ≧ 10kΩ, V_{DD} = 3.0V	135	200	260	mVrms
Tone Output Pre-Emphasis High Band	PEHB	PEHB = 20log (COL/ROW)	1	2	3	dB
Tone Output Distortion	DIS		—	—	10	%
Tone Output Frequency Stability	△f	Except error of osc. frequency	—	—	0.7	%

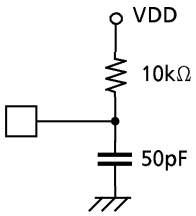
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 30 to 60°C)

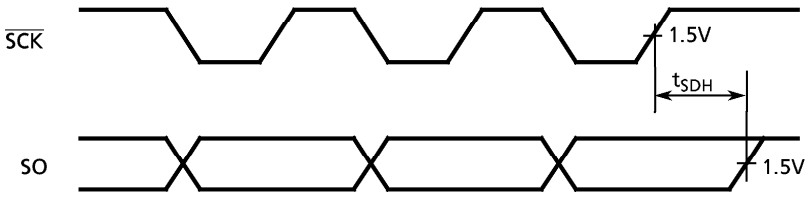
PARAMETER	SYMBO	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		2.1			μs
High level clock pulse width	t_{WCH}	For external clock operation	80	—	—	ns
Low level clock pulse width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$-300	—	—	ns

Note. Shift Data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)

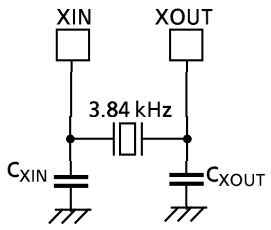


RECOMMENDED OSCILLATING CONDITION

(V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, Topr = – 30 to 60°C)

3.84kHz
Ceramic Resonator

CSB3.84MG901	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30pF
CST3.84MGW901	(KYOCERA)	C_{XIN}, C_{XOUT} built-in



TYPICAL CHARACTERISTICS