



8-Port Dual-Speed Ethernet Switch Controller

1. Features

- Provide single-chip controller of switching function among 8 10/100Mbps Full/Half-duplex Ethernet ports at wire speed.
- Support "Store-and-Forward" switching scheme.
- Support 2.0GBps (@66MHz) ring bus interface for inter-switch connection.
- Embedded local address table of 1K search entries.
- Support source/destination address lookup, learning, and aging.
- Support IEEE802.3x flow control for FDX and back-pressure flow control for HDX.
- Support up to 2MB SGRAM interface.
- Integrate 8 10/100Mbps MAC controllers.
- Cascade 4 switch controllers to construct 32 10/100Mbps switched Ethernet ports in a box easily without extra logic.
- 352-pin PQFP.

2. Description

The MX98206 is a 8-port 10/100Mbps single-chip shared-memory Ethernet switch controller. A desktop or departmental switched Ethernet solution can be achieved by combining MX98206, the necessary physical interfaces and low-cost memory. All 8 ports are full-duplex capable to provide private 20/200Mbps bandwidth connection to power users or servers through external physical (PHY) layers. System manufacturers can cascade 4 MX98206 switch controllers to build a 32-port 10/100Mbps switched Ethernet box without extra logic.

The operation of MX98206 is as following. Data frame received from MII interface is buffered in Rx FIFO before being transferred to external packet buffers under control of queue manager (QM). Priority-based arbitration is utilized in QM to maintain memory I/O bandwidth and fast data transfer without contention. The address information of incoming frame, namely source address (SA) and destination address (DA), is extracted for address self-learning and determining the forwarding port. MX98206 builds the filtering database (or called address table) of local host address information within embedded memory. Via hashing method, the new SA is verified and a new address entry of MAC and physical port I.D. mapping pair is recorded in address table. Same hash transformation is applied to DA to search the address table for determining forwarding port. If DAs of received frames are not recognized through address table, MX98206 issues command to locate destination stations on cascaded node through ring bus. Aging is provided to prevent address table from being overrid-

den. Aging mechanism checks entries in the database to discard the least used ones. When the forwarding port is found, received frames is relayed to destination host through Store-and-Forward switching scheme.

Contention occurs if frames from different source hosts are forwarded to the same destination host simultaneously. Contention makes multiple frames be queued in data buffers. The flow control mechanism is built to prevent buffer overflow which forces controller to lose packets. Controller sets some water marks on output/input queue per port to justify the fullness of data buffers. As soon as buffer fullness is over the warning threshold, flow control mechanism is triggered to stop the respondent host(s) to transmit frames for sometime. For half-duplex operation MII(s), the jam pattern is issued to host. For full-duplex operation MII(s), specific "pause" frame of IEEE Std. 802.3x is issued to host. After buffer fullness drops below the safe threshold, controller releases flow control status to allow hosts to work in norm condition.

System manufactures' design flexibility is our concern too. MX98206 provides ring bus interface for multiple MX98206s cascading. Up to 4 chip can be chained together for high-port-count, high-performance switched Ethernet solution. Simple protocol interpreter is built-in to locate destination on remote node, relay frames to remote node in shortest path. Via the robust ring structure system designer can utilize DRAM parts as data buffers, but still maintain high performance of frame switching.



MX98206

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