TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L Series

TMP93C071

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

****CAUTION****
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = (INT0, INT1), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of fc or fs) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontroller

TMP93C071F

1. Outline and Feature

TMP93C071F is a high-speed advanced 16-bit microcontroller developed for application with VCR system control, software servo motor control and timer control.

In addition to basics such as I/O ports, the TMP93C071F has high-speed/high-precision signal measuring circuit, PWM (Pulse-Width-Modulator) and high-precision real timing pulse generator.

The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)
- TLCS-90 instruction mnemonic upward compatible
- 16-Mbyte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication/division and bit transfer/arithmetic instructions
- High-speed micro DMA: 4 channels (1.6 μs/2 byte at 20 MHz)

(2) Minimum instruction execution time: 200 ns at 20 MHz

(3) Internal ROM: ROMless

(4) Internal RAM: 8 Kbytes

(5) External memory expansion
- Can be expanded up to 16 Mbytes (for both programs and data)
- AM 8/$\overline{16}$ pin (select the external data bus width)
- Can be mixed 8- and 16-bit external data buses.
  ··· Dynamic data bus sizing.

(6) 20-bit time-base-counter (TBC)
- Free running counter
- Accuracy: 100 ns (at 20 MHz)
- Overflow: 105 ms (at 20 MHz)

(7) 8-bit timer (TC0): 1 channel
- CTL linear time counter

(8) 16-bit timer (TC1 to 5): 5 channels
- C.sync count, capstan FG count, general: (3 channels)

(9) Timing pulse generator (TPG): 2 channels
- (16-bit timing data + 6-bit-output data) with 8-stages FIFO: 1 channel
- (16-bit timing data + 4-bit-output data): 1 channel
- Accuracy: 400 ns (at 20 MHz)

(10) Pulse width modulation outputs (PWM)
- 14-bit PWM: 3 channels (for controlling capstan, drum and tuner)
- 8-bit PWM: 9 channels (for controlling volume)
- Carrier frequency: 39.1 kHz (at 20 MHz)

(11) 24-bit time base counter capture circuit (Capture 0)
- (18-bit timing data + 6-bit trigger data) with 8-stages FIFO: 1 channel
- Capture input sources: Remote-control-input (RMTIN), V.sync, CTL, Drum-PG, general (1 channel)
- Accuracy: 400 ns (at 20 MHz)

(12) 17-bit time base counter capture circuit (Capture 1/2)
- (16-bit timing data + 1-bit trigger data): 2 channel
- Capture input sources: Drum-FG, Capstan-FG
- Accuracy: 100 ns (at 20 MHz)

(13) VISS/VASS detection circuit (VISS/VASS)
- CTL duty detection
- VASS data 16-bit latch

(14) Composite-sync-signal (C.sync) input (CSYNC)
- Vertical-sync-signal (V.sync) separation

(15) Head Amp switch/Color Rotary control (HA/CR)

(16) Pseudo-V/H generator (PV/PH)

(17) 8-bit AD converter (ADC): 16 channels
- Conversion speed: 95states (9.5 μs at 20 MHz)

(18) Serial bus I/F
- 8-bit synchronous (SIO0, 1) : 2 channels
- UART : 1 channel
- I^2C bus : 1 channel/2 ports

  ··· Multi - Master function/Master transfer with micro DMA.

(19) Watch dog timer (WDT)

(20) Interrupt controller (INTC)
- CPU: 8 sources ··· SWI instruction, and illegal instruction
- Internal: 21 sources
- External: 5 sources

  7-level priority can be set.

(21) I/O ports

- 57 I/O ports (multiplexed functional pins)
- 8 input ports (P40/AIN3 to P47/AIN10: These pins are also used as analog input for AD converter.)
- 4 output ports (P24/A20 to P27/A23: These pins are also used as address bus outputs.)

(22) Standby function: 4 halt modes (RUN, IDLE2, IDLE1, STOP)

(23) System clock function

- Dual clock operation 20 MHz (High-speed: normal)/32 kHz (Low-speed: slow)
  ⋯ 17-bit Real Time Counter built in

(24) Operating Voltage

- Vcc = 2.7 to 5.5 V (at 32 kHz)
- Vcc = 4.5 to 5.5 V (at 20 MHz)

(25) Package

- 120 pin QFP 28 mm × 28 mm (Pin pitch: 0.8 mm)
- Type name: P-QFP120-2828-0.80B

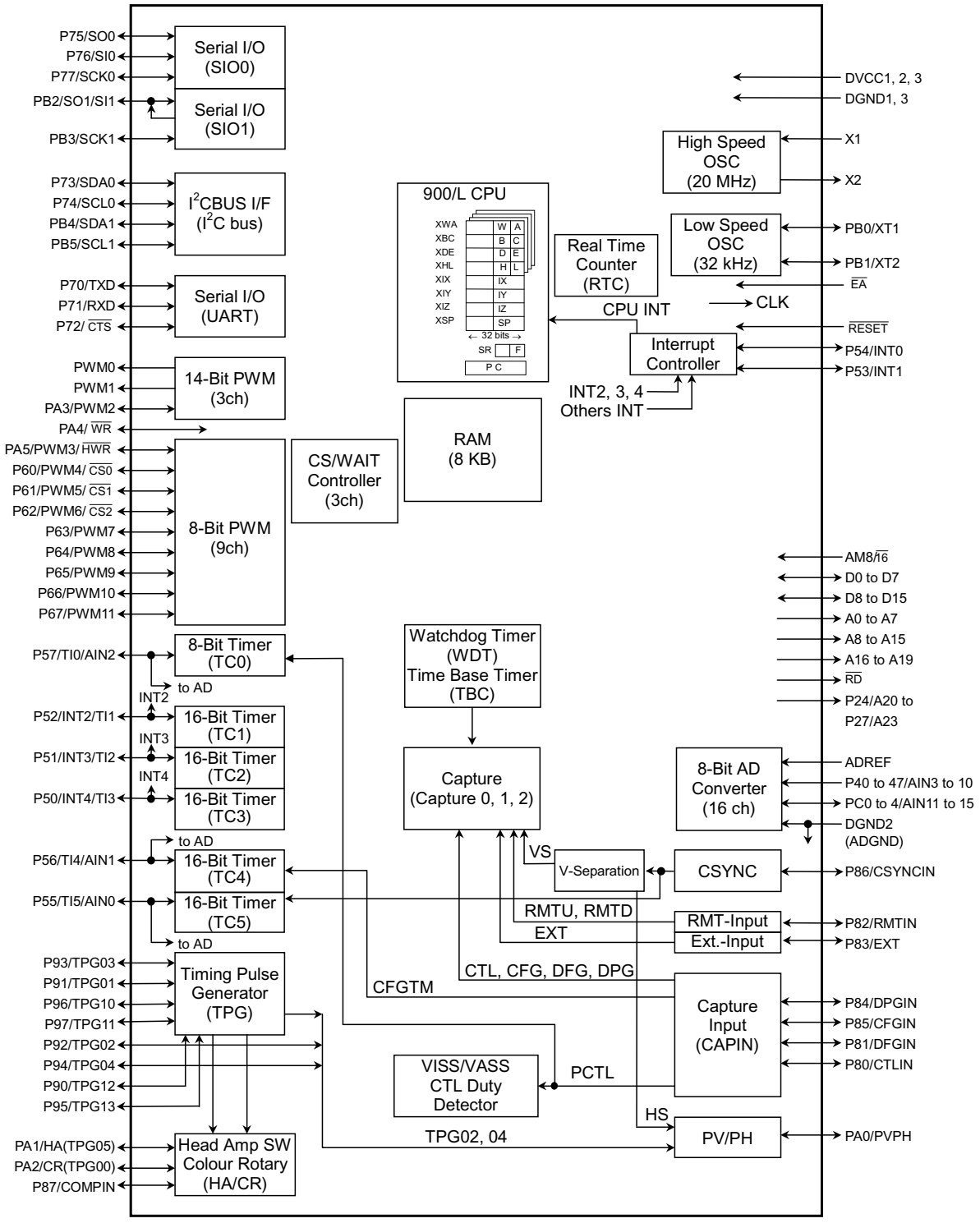


Figure 1.1 TMP93C071 block diagram

2. Pin Assignment And Functions

The assignment of input and output pins for the TMP93C071, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93C071.

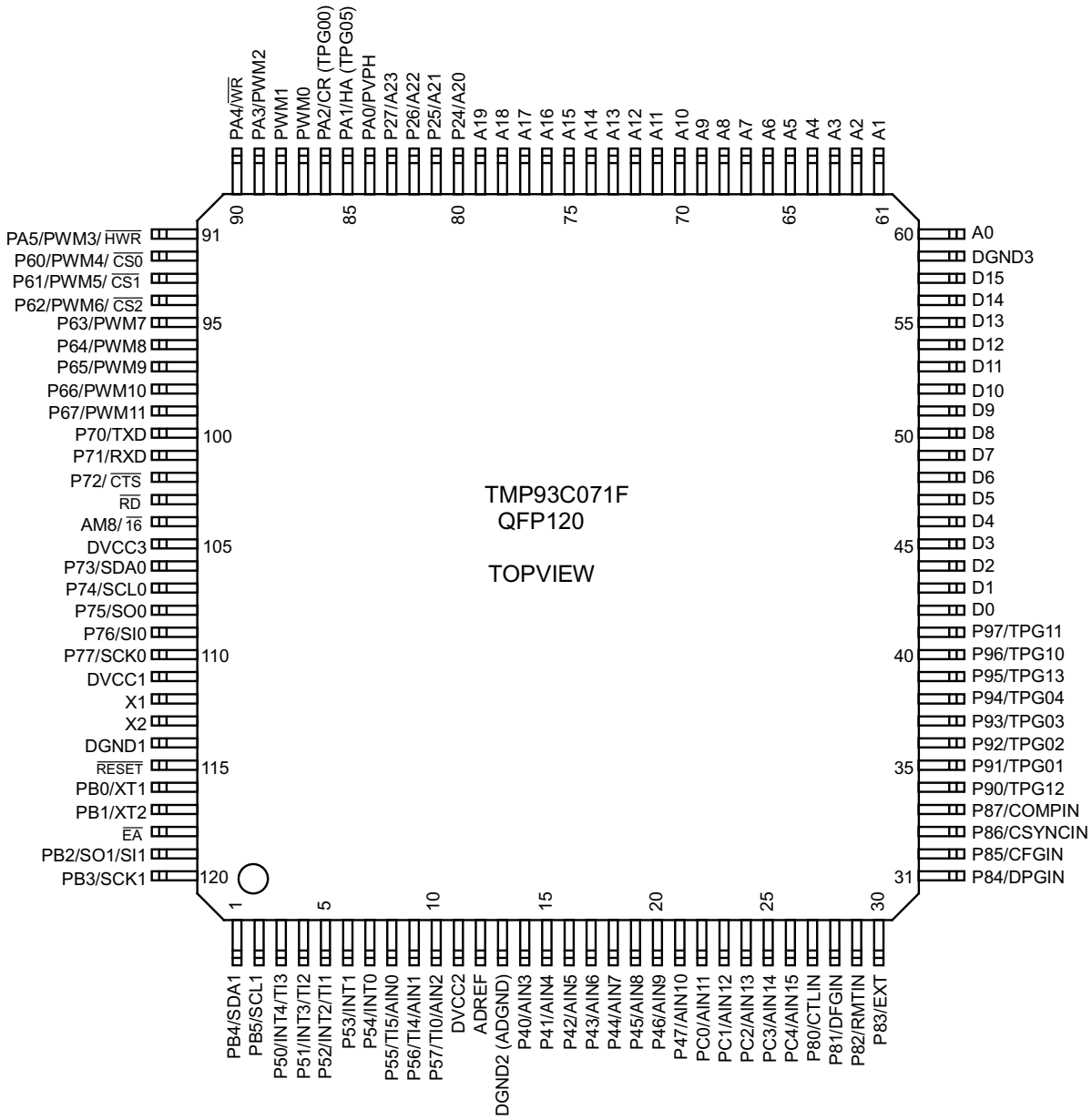


Figure 2.1.1 Pin assignment (120-pin QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 Pin names and function (1/4)

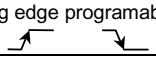
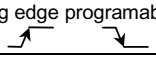
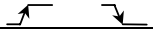
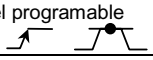
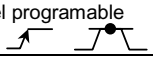
Pin Name	Number of Pins	I/O	Functions
D0 to D15	16	I/O (3-state)	Data: Bits 0 to 15 of data bus
A0 to A19	20	Output	Address: Bits 0 to 19 of address bus
A20 to A23	4	Output	Address: Bits 20 to 23 of address bus
P24 to P27		Output	Port 2: Output port
$\overline{RD}$	1	Output	Read: strobe signal for reading external memory
AM8/ $\overline{16}$	1	Input	Data bus width select input (only 8 bits or 8 bits/16 bits)
$\overline{EA}$	1	Input	External access: Always set to “0”
$\overline{RESET}$	1	Input	Reset: Initializes LSI.(with pull-up R)
X1/X2	2	I/O	High Frequency Oscillator connecting pins (20 MHz)
PB0	1	I/O	Port B0: I/O port (Open-drain output)
XT1		Input	Low Frequency Oscillator connecting pin (32 kHz)
PB1	1	I/O	Port B1: I/O port (Open-drain output)
XT2		Output	Low Frequency Oscillator connecting pin (32 kHz)
ADREF	1	Input	AD reference Voltage input
P40 to P47	8	Input	Port 4: Input ports
AIN3 to AIN10		Input	Analog input: Analog input signal for AD converter
PC0 to PC4	5	I/O	Port C: PC0 to PC4 I/O port that allows selection of I/O on a bit basis.
AIN11 to AIN15		Input	Analog input: Analog input signal for AD converter
P50	1	I/O	Port 50: I/O port (Schmitt input)
INT4		Input	External Interrupt request input 4 Rising edge/Falling edge programable
TI3		Input	16-bit timer3 (TC3) Input 3 
P51	1	I/O	Port 51: I/O port (Schmitt input)
INT3		Input	External Interrupt request input 3 Rising edge/Falling edge programable
TI2		Input	16-bit timer2 (TC2) Input 2 
P52	1	I/O	Port 52: I/O port (Schmitt input)
INT2		Input	External Interrupt request input 2 Rising edge/Falling edge programable
TI1		Input	16-bit timer1(TC1) Input 1 
P53	1	I/O	Port 53: I/O port (Schmitt input)
INT1		Input	External Interrupt request input 1: Rising edge/ Level programable 
P54	1	I/O	Port 54: I/O port (Schmitt input)
INT0		Input	External Interrupt request input 0: Rising edge/ Level programable 
P55	1	I/O	Port 55: I/O port (Schmitt input)
TI5		Input	16-bit timer5 (TC5) Input 5
AIN0		Input	Analog input: Analog input signal for AD converter
P56	1	I/O	Port 56: I/O port (Schmitt input)
TI4		Input	16-bit timer4 (TC4) Input 4
AIN1		Input	Analog input: Analog input signal for AD converter
P57	1	I/O	Port 57: I/O port (Schmitt input)
TI0		Input	8-bit timer0 (TC0) Input 0
AIN2		Input	Analog input: Analog input signal for AD converter

Table 2.2.1 Pin names and function (2/4)

Pin Name	Number of Pins	I/O	Functions
PWM0	1	Output	PWM (14-bit) output 0: PWM0 output Push-pull or open-drain output selectable
PWM1	1	Output	PWM (14-bit) output 1: PWM1 output Push-pull or open-drain output selectable
P60 PWM4 $\overline{CS0}$	1	I/O Output Output	Port 60: I/O port, Push-pull or open-drain output selectable 8-bit PWM output 4: PWM4 output Chip select 0: Output 0 when address is within specified address area.
P61 PWM5 $\overline{CS1}$	1	I/O Output Output	Port 61: I/O port, Push-pull or open-drain output selectable 8-bit PWM output 5: PWM5 output Chip select 1: Output 0 when address is within specified address area.
P62 PWM6 $\overline{CS2}$	1	I/O Output Output	Port 62: I/O port, Push-pull or open-drain output selectable 8-bit PWM output 6: PWM6 output Chip select 2: Output 0 when address is within specified address area.
P63 PWM7	1	I/O Output	Port 63: I/O port, Push-pull or open-drain output selectable 8-bit PWM output 7: PWM7 output
P64 PWM8	1	I/O Output	Port 64: I/O port, Push-pull or open-drain output selectable 8-bit PWM output 8: PWM8 output
P65 PWM9	1	I/O Output	Port 65: I/O port, Push-pull or open-drain output selectable 8-bit PWM output 9: PWM9 output
P66 PWM10	1	I/O Output	Port 66: I/O port, Push-pull or open-drain output selectable 8-bit PWM output 10: PWM10 output
P67 PWM11	1	I/O Output	Port 67: I/O port, Push-pull or open-drain output selectable 8-bit PWM output 11: PWM11 output
P70 TXD	1	I/O Output	Port 70: I/O port (Schmitt input), Push-pull or open-drain output selectable UART send data
P71 RXD	1	I/O Input	Port 71: I/O port (Schmitt input) UART receive data
P72 $\overline{CTS}$	1	I/O Input	Port 72: I/O port (Schmitt input) UART clear to send
P73 SDA0	1	I/O I/O	Port 73: I/O port (Schmitt input), Push-pull or open-drain output selectable I^2C bus SDA line 0
P74 SCL0	1	I/O I/O	Port 74: I/O port (Schmitt input), Push-pull or open-drain output selectable I^2C bus SCL line 0
P75 SO0	1	I/O Output	Port 75: I/O port (Schmitt input), Push-pull or open-drain output selectable SIO0 send data 0
P76 SI0	1	I/O Input	Port 76: I/O port (Schmitt input) SIO0 receive data 0
P77 SCK0	1	I/O I/O	Port 77: I/O port (Schmitt input), Push-pull or open-drain output selectable SIO0 transfer clock input/output 0
P80 CTLIN	1	I/O Input	Port 80: I/O port (Schmitt input) Capture input for Control signal (CTL)
P81 DFGIN	1	I/O Input	Port 81: I/O port (Schmitt input) Capture input for Drum-FG signal (DFG)
P82 RMTIN	1	I/O Input	Port 82: I/O port (Schmitt input) Capture input for Remote Control Input signal

Table 2.2.1 Pin names and function (3/4)

Pin Name	Number of Pins	I/O	Functions
P83 EXT	1	I/O Input	Port 83: I/O port (Schmitt input) External Capture input (Rising edge only)
P84 DPGIN	1	I/O Input	Port 84: I/O port (Schmitt input) Capture input for Drum-PG signal (DPG)
P85 CFGIN	1	I/O Input	Port 85: I/O port (Schmitt input) Capture input for Capstan-FG signal (CFG)
P86 CSYNCIN	1	I/O Input	Port 86: I/O port (Schmitt input) Capture input for C.sync
P87 COMPIN	1	I/O Input	Port 87: I/O port (Schmitt input) Envelope Comparator Input (to HA/CR)
P90 TPG12	1	I/O Output	Port 90: I/O port, Push-pull or open-drain output selectable TPG12: TPG output 12
P91 TPG01	1	I/O Output	Port 91: I/O port, Push-pull or open-drain output selectable TPG01: TPG output 01
P92 TPG02	1	I/O Output	Port 92: I/O port, Push-pull or open-drain output selectable TPG02: TPG output 02 (Internally connected to PV/PH Logic)
P93 TPG03	1	I/O Output	Port 93: I/O port, Push-pull or open-drain output selectable TPG03: TPG output 03
P94 TPG04	1	I/O Output	Port 93: I/O port, Push-pull or open-drain output selectable TPG04: TPG output 04 (Internally connected to PV/PH Logic)
P95 TPG13	1	I/O Output	Port 95: I/O port, Push-pull or open-drain output selectable TPG13: TPG output 13
P96 TPG10	1	I/O Output	Port 96: I/O port, Push-pull or open-drain output selectable TPG10: TPG output 10
P97 TPG11	1	I/O Output	Port 97: I/O port, Push-pull or open-drain output selectable TPG11: TPG output 11
PA0 PVPH	1	I/O Output 3-state	Port PA0: I/O port Pseudo-V.sync, Pseudo-H.sync output (controlled by TPG02/04.)
PA1 HA (TPG05)	1	I/O Output	Port PA1: I/O port HA: Head amp switch output or TPG05 output
PA2 CR (TPG00)	1	I/O Output	Port PA2: I/O port schmitt CR: Colour Rotary output or TPG00 output
PA3 PWM2	1	I/O Output	Port A3: I/O port, PWM (14-bit) output 2: PWM2 output Push-pull or open-drain output selectable
PA4 $\overline{WR}$	1	I/O Output	Port A4: I/O port, Push-pull or open-drain output selectable Write: Strobe signal for writing data on pins D0 to D7
PA5 PWM3 $\overline{HWR}$	1	I/O Output Output	Port A5: I/O port, Push-pull or open-drain output selectable 8-bit PWM output 3: PWM3 output High write: Strobe signal for writing data on pins D8 to D15
PB2 SO1/SI1	1	I/O I/O	Port PB2: I/O port (Schmitt input), Push-pull or open-drain output selectable SIO1 send data 1 and receive data 1 (Internally connected)
PB3 SCK1	1	I/O I/O	Port PB3: I/O port (Schmitt input), Push-pull or open-drain output selectable SIO1 transfer clock input/output 1

Table 2.2.1 Pin names and function (4/4)

Pin Name	Number of Pins	I/O	Functions
PB4 SDA1	1	I/O I/O	Port PB4: I/O port (Schmitt input), Push-pull or open-drain output selectable I^2C bus SDA line 1
PB5 SCL1	1	I/O I/O	Port PB5: I/O port (Schmitt input), Push-pull or open-drain output selectable I^2C bus SCL line 1
DVCC1, 2, 3	3		Power supply pins All of these pins should be connected to power source.
DGND1, DGND2 (ADGND), DGND3	3		GND pins (0 V) All of these pins should be connected to GND (0 V) line. DGND2 are also used as ADGND for AD converter.

3. Operation

This section describes the functions and basic operational blocks of TMP93C071 devices.

See the "7. Points of Concern and Restrictions" for the using notice and restrictions for each block.

3.1 CPU

TMP93C071 devices have a built-in high-performance 16-bit CPU (900/L CPU). (For CPU operation, see TLCS-900/L CPU in the previous section).

This section describes CPU functions unique to the TMP93C071 that are not described in the previous section.

3.1.1 Reset

To reset the TMP93C071, the RESET input must be kept at 0 for at least 10 system clocks. (1 μs at 20 MHz) within the operating voltage range and with a stable oscillation.

When reset is accepted, the CPU sets as follows:

- Program Counter (PC) according to Reset Vector that is stored FFFF00H to FFFF02H.

  PC (7 to 0) ← stored data in location FFFF00H

  PC (15 to 8) ← stored data in location FFFF01H

  PC (23 to 16) ← stored data in location FFFF02H
- Stack pointer (XSP) for system mode to 100H.
- IFF2 to 0 bits of status register to 111. (Sets mask register to interrupt level 7.)
- MAX bit of status register to 1. (Sets to maximum mode)
- Bits RFP2 to 0 of status register to 000. (Sets register banks to 0.)

When reset is released, instruction execution starts from PC (reset vector). CPU internal registers other than the above are not changed.

When reset is accepted, processing for built-in I/Os, ports, and other pins is as follows:

- Initializes built-in I/O registers as per specifications.
- Sets port pins (including pins also used as built-in I/Os) to general-purpose input/output port mode.

Note: By resetting, register in the CPU except program counter (PC), status register (SR) and stack pointer (XSP) and the data in internal RAM are not changed.

Figure 3.1.1 show the reset timing chart of TMP93C071.

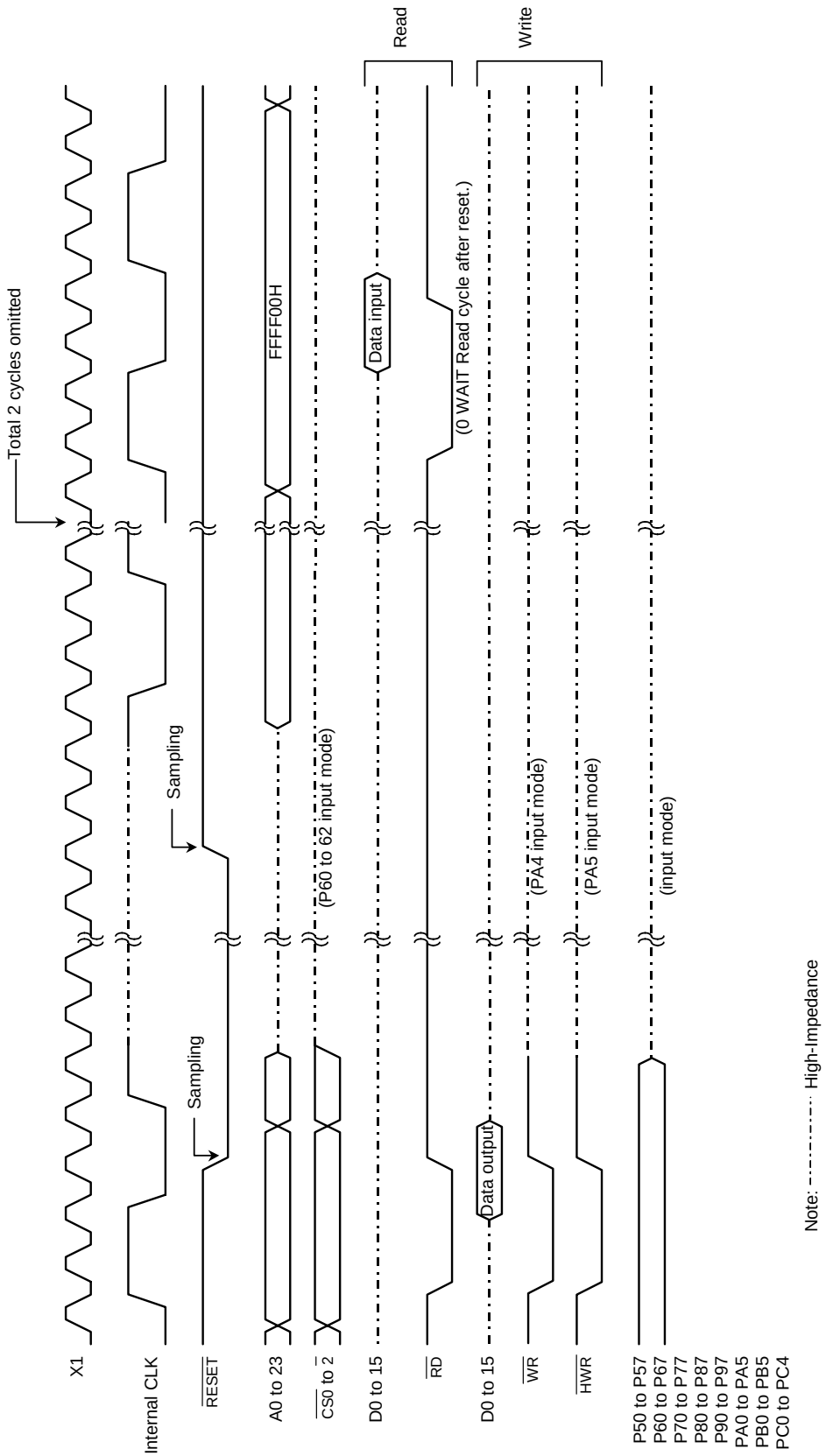


Figure 3.1.1 TMP93C071 reset timing chart

3.1.2 AM8/$\overline{16}$ pin

a. With fixed 16-bit data bus, external 16-bit data bus or 8-bit data bus is selectable
Set this pin to L.
The external data bus width is set by the chip select/wait control register which is described in section 3.6.3.
It is necessary to set the program memory to be accessed to 16-bit data bus after reset.

b. With fixed external 8-bit data bus
Set this pin to H.
The values of bit 4 <B0BUS>, <B1BUS> and <B2BUS> in the chip select/wait control register described in section 3.6.3 are invalid. The external 8-bit data bus is fixed.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93C071.

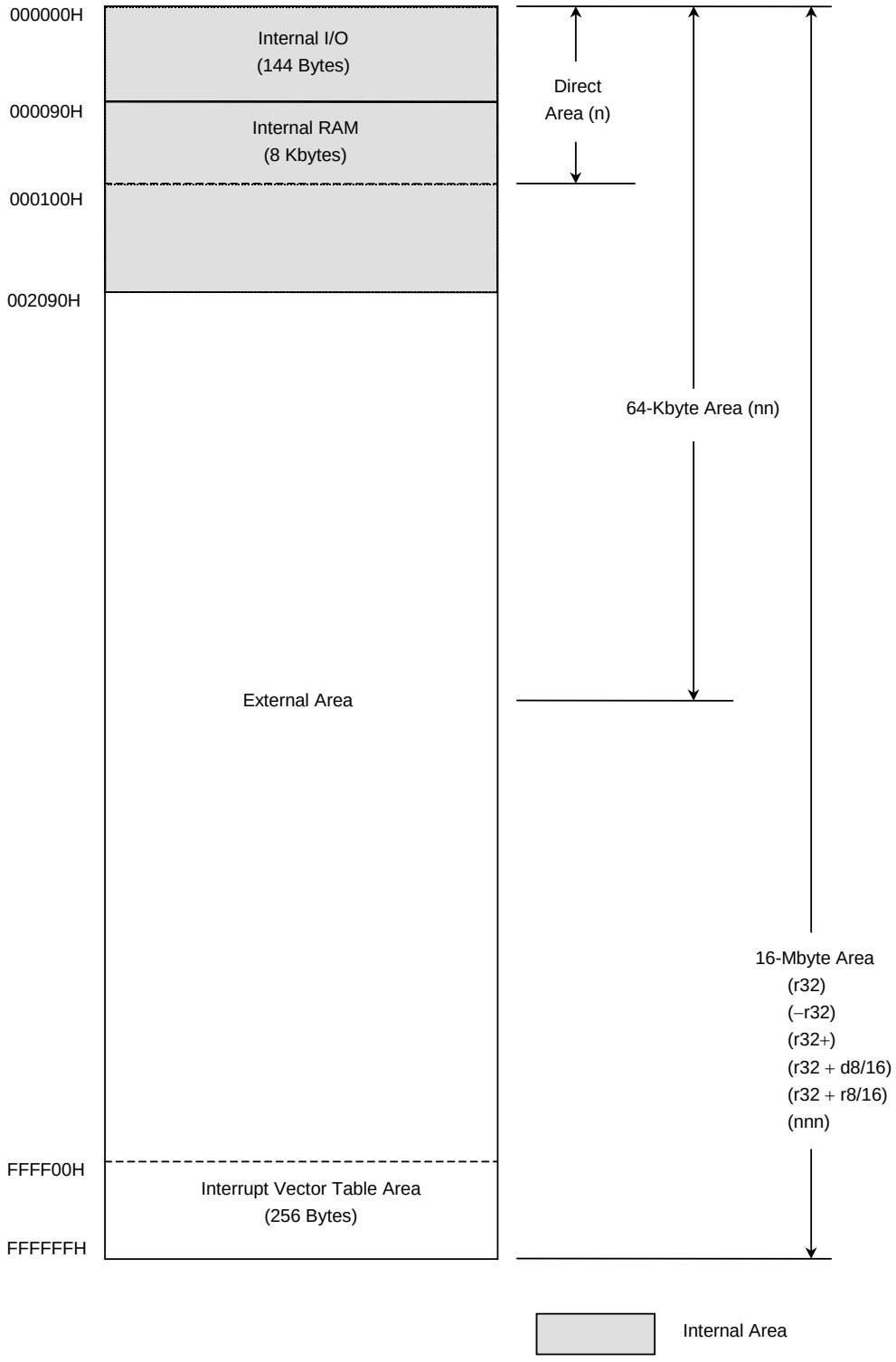


Figure 3.2.1 Memory map

4. Electrical Characteristics(Preliminary)

4.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	−0.5 to 6.5	V
Input Voltage	V_{IN}	−0.5 to Vcc + 0.5	V
(Including Open-drain ports)	V_{OUT}	−0.5 to Vcc + 0.5	V
Output Current (Per 1 pin)	I_{OL}	3.2	mA
Output Current (Per 1 pin)	I_{OH}	−3.2	mA
Output Current (total)	ΣI_{OL}	120	mA
Output Current (total)	ΣI_{OH}	−120	mA
Power Dissipation (Ta = 70°C)	PD	600	mW
Soldering Temperature (10sec)	T_{SOLDER}	260	°C
Storage Temperature	T_{STG}	−65 to 150	°C
Operating Temperature	T_{OPR}	−20 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Ta = −20 to 70°C

Parameter		Symbol	Condition	Min	Typ.	Max	Unit
Power Supply Voltage		Vcc	fc = 4 to 20 MHz	4.5		5.5	V
			fs = 30 to 34 kHz	2.7			
Input Low Voltage	D0 to D15	V_{IL} (TTL)	Vcc ≧ 4 .5 V	−0.3		0.8	V
			Vcc < 4.5 V			0.6	
	P4, P6, P9, PA, PB0, 1, PC	V_{IL1} (CMOS)	Vcc = 2.7 to 5.5 V			0.3 Vcc	
	$\overline{RESET}$, INT0 to 4, P5, P7, P8, PB2 to 5	V_{IL2} (Schmitt)				0.25 Vcc	
	$\overline{EA}$, AM8/$\overline{16}$	V_{IL3} (Fixed)				0.3	
	X1	V_{IL4} (Xtal)				0.2 Vcc	
Input High Voltage	D0 to D15	V_{IH} (TTL)	Vcc ≧ 4.5 V	2.2		Vcc + 0.3	V
			Vcc < 4.5 V	2.0			
	P4, P6, P9, PA, PB0, 1, PC	V_{IH1} (CMOS)	Vcc = 2.7 to 5.5 V	0.7 Vcc			
	$\overline{RESET}$, INT0 to 4, P5, P7, P8, PB2 to 5	V_{IH2} (Schmitt)		0.75 Vcc			
	$\overline{EA}$, AM8/$\overline{16}$	V_{IH3} (Fixed)		Vcc − 0.3			
	X1	V_{IH4} (Xtal)		0.8 Vcc			

DC Characteristics (2/2)

Ta = −20 to 70°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Output Low Voltage	V_{OL}	IOL = 1.6 mA (Vcc = 2.7 to 5.5 V)			0.45	V
Output High Voltage	V_{OH}	IOH = −400 μA (Vcc = 2.7 to 5.5 V)	2.4			V
	V_{OH1}	IOH = −700 μA (Vcc = 4.5 to 5.5V)	4.1			
Input Leakage Current	I_{LI}	0.0 ≦ Vin ≦ Vcc		0.02	±5	μA
Output Leakage Current	I_{LO}	0.2 ≦ Vin ≦ Vcc − 0.2		0.05	±10	
Power Down Voltage	V_{STOP}	VIL2 = 0.2 Vcc, VIH2 = 0.8 Vcc	2.0		6.0	V
$\overline{RESET}$ Pull Up Resistor	R_{RST}	Vcc = 5 V ± 10%	50		150	Ω
		Vcc = 3 V ± 10%	80		200	
Pin Capacitance	CIO	osc = 1 MHz/100 mVpp			10	pF
Schmitt Width $\overline{RESET}$, INT0 to 4, P5, P7, P8, PB2 to 5	V_{TH}			1.0		V
NORMAL	I_{CC}	Vcc = 5 V ± 10% fc = 20 MHz		28	45	mA
RUN				22	35	
IDLE2				16	25	
IDLE1				3.5	8	
SLOW		Vcc = 3 V ± 10% fs = 32.768 kHz (Typ: Vcc = 3.0 V)		40	70	μA
RUN				32	45	
IDLE2				27	40	
IDLE1				17	30	
STOP		Vcc = 2.7 to 5.5 V		0.2	10	μA

Note 1: Typical value are for Ta = 25°C and Vcc = 5 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL, SLOW).
Only CPU is operational; output pins are open and input pins are fixed.

Note 3: P55, P56 and P57 have a hysteresis when TI5, TI4 and TI0 is enabled.

4.3 AD Conversion Characteristics

Ta = −20 to 70°C, Vcc = 4.5 to 5.5 V

Parameter	Symbol	Min	Typ.	Max	Unit
Analog Reference Voltage Supply	ADREF	Vcc−1.5	Vcc	Vcc	V
	ADGND	Vss	Vss	Vss	V
Analog Input Voltage Range	V_{AIN}	ADGND	—	ADREF	V
Analog Current for ADREF	I_{REF}	—	1.0	1.5	mA
Total tolerance (excludes quantization error) (Ta=25°C, Vcc=ADREF=5V)	E_T	—	—	±3	LSB

4.4 AC Electrical Characteristics(Preliminary) (Separated Bus)

(1) Vcc = 5 V ± 10% Ta = −20 to 70°C

Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
OSC.Period (= X)	t_{OSC}	50	250	50		ns
A0 to 23 Valid → $\overline{RD}$ / $\overline{WR}$ / $\overline{HWR}$ Fall	t_{AC}	1.0X − 25		25		ns
$\overline{RD}$ / $\overline{WR}$ / $\overline{HWR}$ Rise → A0 to 23 Hold	t_{CA}	0.5X − 25		0		ns
A0 to 23 Valid → D0 to 15 input	t_{AD}		3.5X − 65		110	ns
$\overline{RD}$ fall → D0 to 15 input	t_{RD}		2.5X − 60		65	ns
$\overline{RD}$ Low width	t_{RR}	2.5X − 40		85		ns
$\overline{RD}$ rise → D0 to 15 Hold	t_{HR}	0		0		ns
$\overline{WR}$ / $\overline{HWR}$ Low Pulse Width	t_{WW}	2.5X − 40		85		ns
D0 to 15 Valid → $\overline{WR}$ / $\overline{HWR}$ Rise	t_{DW}	2.0X − 55		45		ns
$\overline{WR}$ / $\overline{HWR}$ Rise → D0 to 15 Hold	t_{WD}	0.5X − 15		10		ns
A0 to 23 Valid → Port Input	t_{APH}		2.5X − 120		5	ns
A0 to 23 Valid → Port Hold	t_{APH2}	2.5X + 50		175		ns
$\overline{WR}$ / $\overline{HWR}$ Rise → Port Valid	t_{CP}		200		200	ns

AC Test Condition:

- Output Level: High = 2.2 V, Low = 0.8 V, CL = 50pF
  (D0 to D15, A0 to 23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, $\overline{CS0}$ to $\overline{CS2}$: CL = 100pF)
- Input Level: High = 2.4 V/Low = 0.45 V (D0 to D15)
  High = 0.8 Vcc/Low = 0.2 Vcc (except D0 to D15)

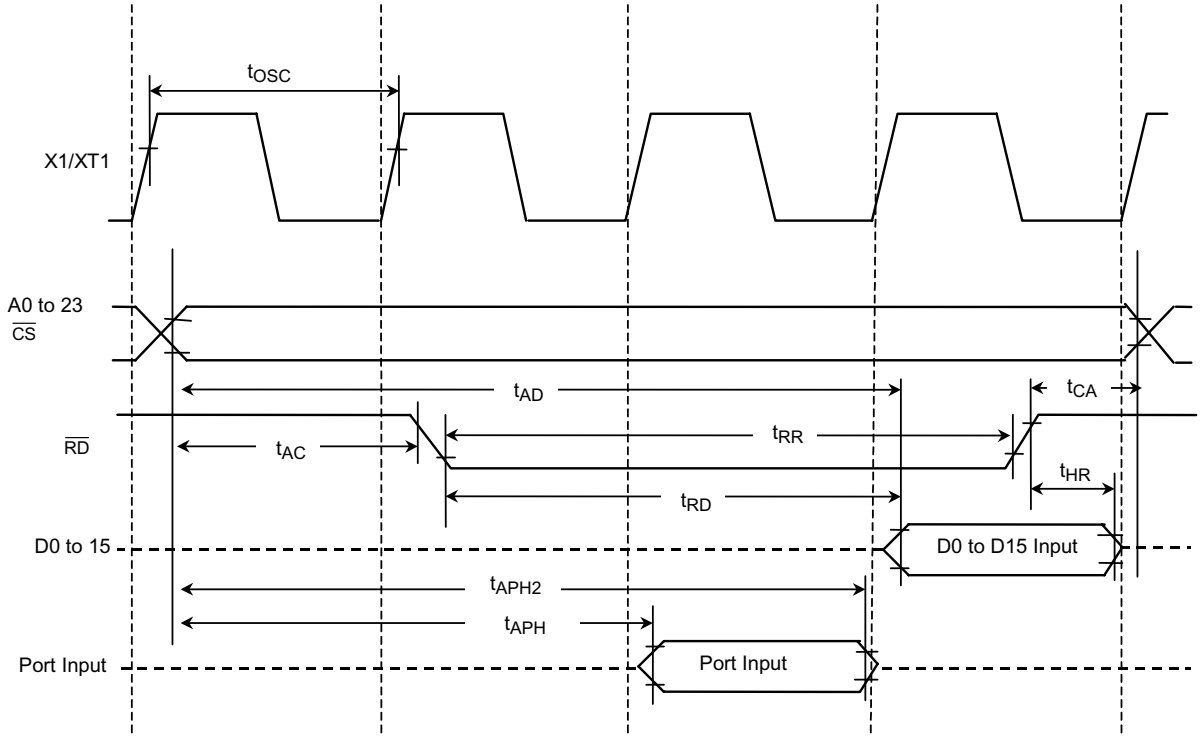
(2) Vcc = 3V ± 10% Ta = −20 to 70°C

Parameter	Symbol	Variable		Unit
		Min	Max	
OSC.Period(= X)	t_{OSC}	29400	33300	ns
A0 to 23 Valid → $\overline{RD}$ / $\overline{WR}$ / $\overline{HWR}$ Fall	t_{AC}	1.0X − 50		ns
$\overline{RD}$ / $\overline{WR}$ / $\overline{HWR}$ Rise → A0 to 23 Hold	t_{CA}	0.5X − 40		ns
A0 to 23 Valid → D0 to 15 input	t_{AD}		3.5X − 125	ns
$\overline{RD}$ fall → D0 to 15 input	t_{RD}		2.5X − 115	ns
$\overline{RD}$ Low width	t_{RR}	2.5X − 40		ns
$\overline{RD}$ rise → D0 to 15 Hold	t_{HR}	0		ns
$\overline{WR}$ / $\overline{HWR}$ Low Pulse Width	t_{WW}	2.5X − 40		ns
D0 to 15 Valid → $\overline{WR}$ / $\overline{HWR}$ Rise	t_{DW}	2.0X − 120		ns
$\overline{WR}$ / $\overline{HWR}$ Rise → D0 to 15 Hold	t_{WD}	0.5X − 40		ns
A0 to 23 Valid → Port Input	t_{APH}		2.5X − 120	ns
A0 to 23 Valid → Port Hold	t_{APH2}	2.5X + 50		ns
$\overline{WR}$ / $\overline{HWR}$ Rise → Port Valid	t_{CP}		200	ns

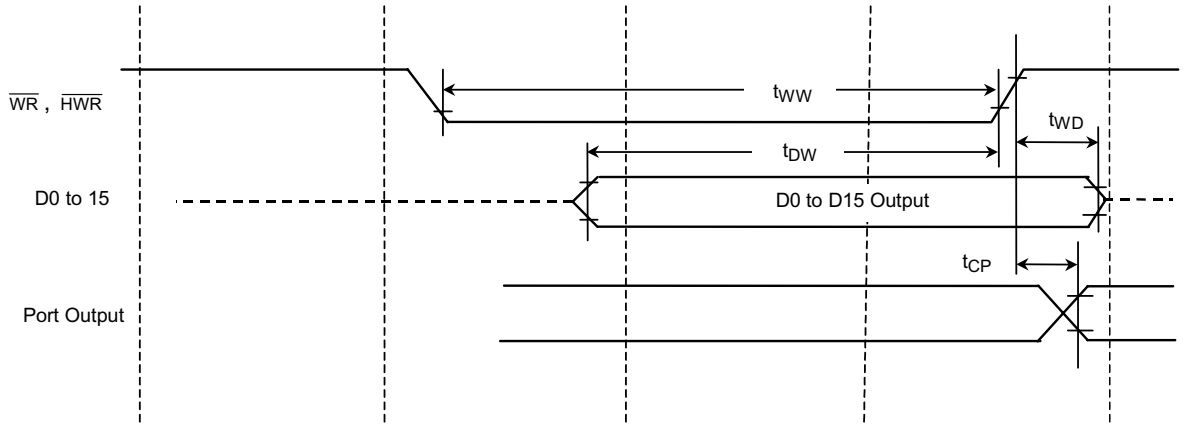
AC Test Condition:

- Output Level: High = 0.7 × Vcc, Low = 0.3 × Vcc, CL = 50pF
- Input Level: High = 0.9 × Vcc, Low = 0.1 × Vcc

(1) Read cycle timing chart

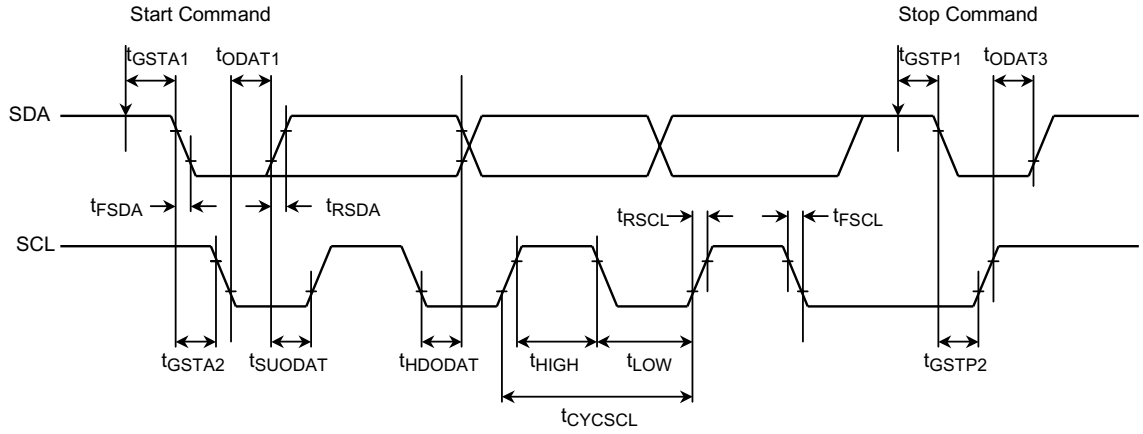


(2) Write cycle timing chart



4.5 Serial Channel Timing Chart

(1) I²C bus



Parameter		Symbol	Min	Typ.	Max	Unit
SCL cycle		t_{CYCSCL}	16N/f + 12/f	—	—	s
SCL low pulse width		t_{LOW}	—	8N/f	—	s
SCL High pulse width		t_{HIGH}	8N/f + 10/f	—	—	s
SDA Rising Time	(Note 1)	t_{RSDA}	—	—	—	s
SDA Falling Time	(Note 1)	t_{FSDA}	—	—	—	s
SCL Rising Time	(Note 1)	t_{RSCL}	—	—		s
SCL Falling Time	(Note 1)	t_{FSCL}	—	—		s
The time from start command write to start sheecense		t_{GSTA1}	—	6/f		s
Start condition hold time, start generation of the first clock after this		t_{GSTA2}	—	8N/f + 4/f		s
Delay time from SCL rising to data output	(Note 2)	T_{ODAT1}	—	—	10/f	s
Set up time of data output SCL rising	(Note 2)	t_{SUODAT}	8N/f −(10/f + t_{FSCL})	—	—	s
The time of holding data for SCL rising	(Note 3)	t_{HODAT}	3/f	—	—	s
The time from stop command write to starting stop sheecense		t_{GSTP1}	—	6/f	—	s
The time from SDA falling to SCL rising (during stop sheecense)		t_{GSTP2}	—	8N/f + 14/f	—	s
Stop condition set up time		t_{GSTP3}	8N/f + 14/f	—	—	s

Note 1: The time of rising/falling depend on the feature of bus interface.

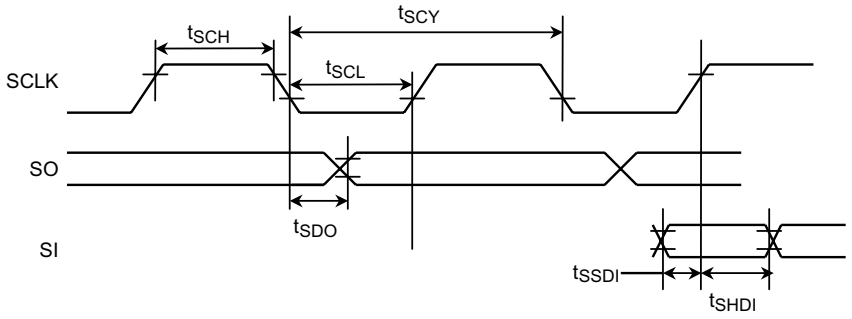
Note 2: The worst case is at the first bit of slave address.

Note 3: The worst case is at the acknowledge bit.

Frequency divisor set in N: I2CCR3<DV4 to 0>

Internal system clock (fsys) = f/2 (f = fc or fs)

(2) SIO0, 1



SIO AC Electrical Characteristics

(SCLK external input)

Ta = −20 to 70°C Vcc = 5 V ± 10%

Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
SCLK cycle	t_{SCY}	2^5X (2^4X)		1.6 (0.8)		us
SCLK High pulse width	t_{SCH}	tSCY/2 − 50 (t_{SYC}/2)		750 (400)		ns
SCLK Low pulse width	t_{SCL}	tSCY/2−50 (t_{SYC}/2)		750 (400)		ns
SCLK shift edge → SO delay	t_{SDO}		6X + 50		350	ns
SCLK shift edge → SI setup	t_{SSDI}	−X + 50		0		ns
SCLK shift edge → SI hold	t_{SHDI}	6X + 50		350		ns

Note: These are value when SCxMOD<SIOxE> don't be disabled under transferring.

(SCLK internal output)

Ta = −20 to 70°C Vcc = 5 V ± 10%

Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
SCLK cycle	t_{SCY}	2^4X	2^7X	0.8	6.4	us
SCLK High pulse width	t_{SCH}	t_{SCY}/2 − 50	t_{SCY}/2	350	3200	ns
SCLK Low pulse width	t_{SCL}	t_{SCY}/2 − 50	t_{SCY}/2	350	3200	ns
SCLK shift edge → SO delay	t_{SDO}		X + 50		100	ns
SCLK shift edge → SI setup	t_{SSDI}	X + 50		100		ns
SCLK shift edge → SI hold	t_{SHDI}	0		0		ns