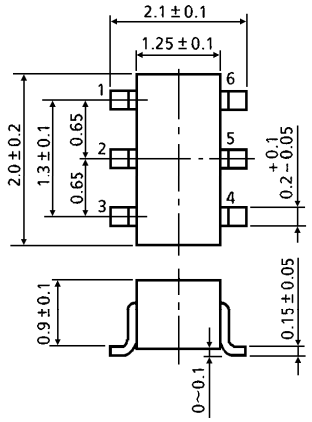
TOSHIBA FIELD EFFECT TRANSISTOR SILICON N CHANNEL MOS TYPE

SSM6N04FU

HIGH SPEED SWITCH APPLICATIONS

- With Built-in Gate-Source Resistor : R_{GS} = 1 MΩ (Typ.)
- 2.5 V Gate Drive
- Low Gate Threshold Voltage : V_{th} = 0.7~1.3 V
- Small Package

Unit in mm



1. SOURCE 1 4. SOURCE 2
2. GATE 1 5. GATE 2
3. DRAIN 2 6. DRAIN 1

US6	
JEDEC	—
EIAJ	—
TOSHIBA	2-2J1C

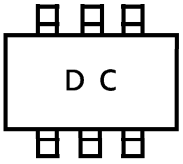
Weight : 6.8 mg

MAXIMUM RATINGS (Ta = 25°C) (Q1, Q2 COMMON)

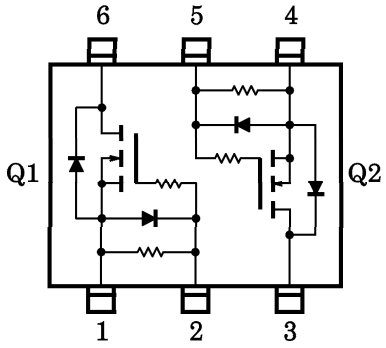
CHARACTERISTIC	SYMBOL	RATING	UNIT
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GSS}	10	V
DC Drain Current	I_D	100	mA
Drain Power Dissipation	P_D*	200	mW
Channel Temperature	T_{ch}	150	°C
Storage Temperature Range	T_{stg}	−55~150	°C

* Total Rating

MARKING



PIN ASSIGNMENT (TOP VIEW)



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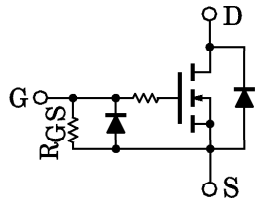
ELECTRICAL CHARACTERISTICS (Ta = 25°C) (Q1, Q2 COMMON)

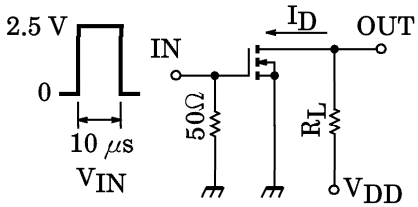
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	V_{GS} = 10 V, V_{DS} = 0	—	—	15	μA
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	I_D = 100 μA, V_{GS} = 0	20	—	—	V
Drain Cut-off Current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0	—	—	1	μA
Gate Threshold Voltage		V_{th}	V_{DS} = 3 V, I_D = 0.1 mA	0.7	—	1.3	V
Forward Transfer Admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 10 mA	25	50	—	mS
Drain-Source ON Resistance		$R_{DS(ON)}$	I_D = 10 mA, V_{GS} = 2.5 V	—	4	12	Ω
Input Capacitance		C_{iss}	V_{DS} = 3 V, V_{GS} = 0, f = 1 MHz	—	11.0	—	pF
Reverse Transfer Capacitance		C_{rss}	V_{DS} = 3 V, V_{GS} = 0, f = 1 MHz	—	3.3	—	pF
Output Capacitance		C_{oss}	V_{DS} = 3 V, V_{GS} = 0, f = 1 MHz	—	9.3	—	pF
Switching Time	Turn-on Time	t_{on}	V_{DD} = 3 V, I_D = 10 mA, V_{GS} = 0~2.5 V	—	0.16	—	μs
	Turn-off Time	t_{off}	V_{DD} = 3 V, I_D = 10 mA, V_{GS} = 0~2.5 V	—	0.19	—	
Gate-Source Resistor		R_{GS}	V_{GS} = 0~10 V	0.7	1.0	1.3	MΩ

(Q1, Q2 COMMON)
EQUIVALENT CIRCUIT



SWITCHING TIME TEST CIRCUIT

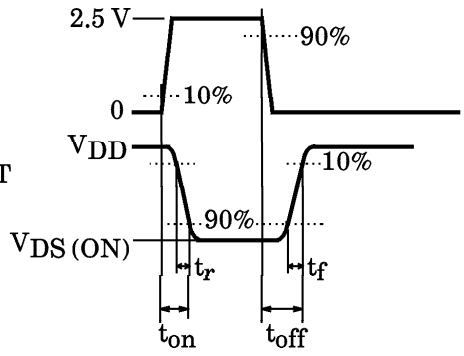
(a) TEST CIRCUIT



V_{DD} = 3 V
D.U. ≦ 1%
V_{IN} : t_r, t_f < 5 ns
(Z_{out} = 50 Ω)
COMMON SOURCE
Ta = 25°C

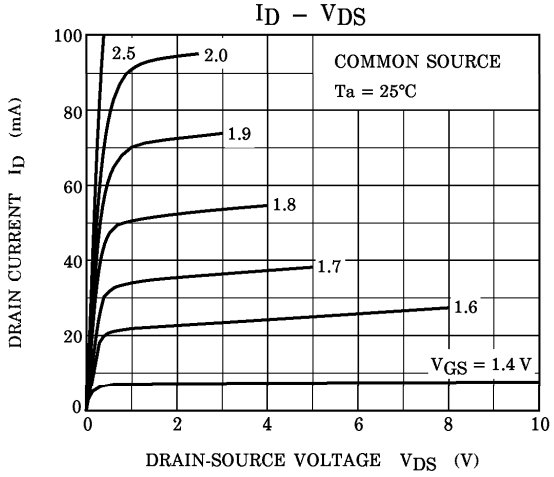
(b) V_{IN}
V_{GS}

(c) V_{OUT}
V_{DS}

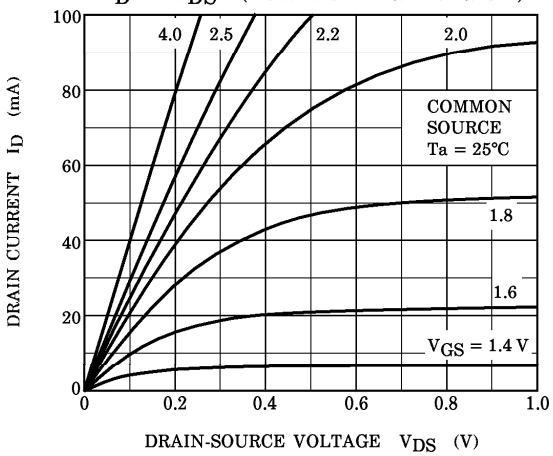


(Q1, Q2 COMMON)

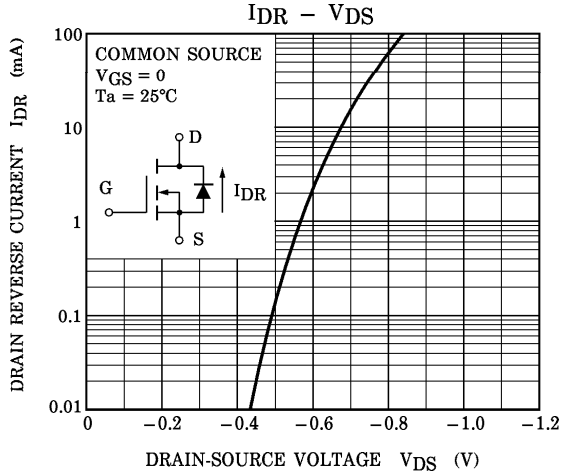
I_D – V_{DS}



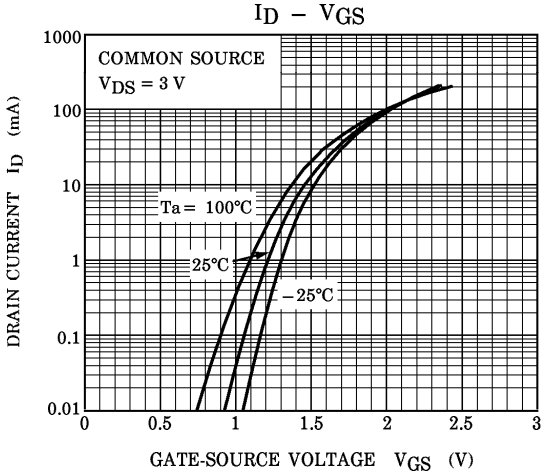
I_D – V_{DS} (LOW VOLTAGE REGION)



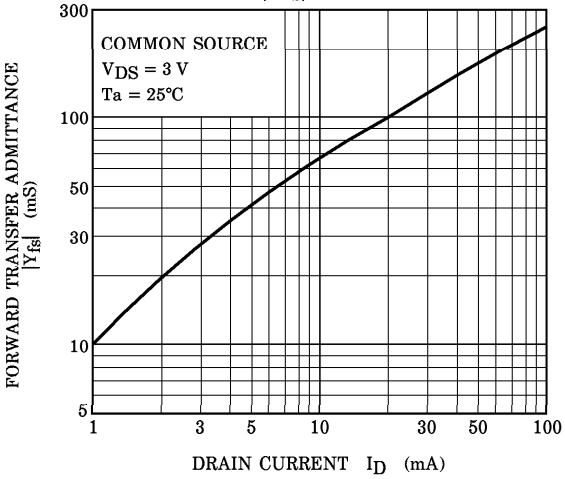
I_{DR} – V_{DS}



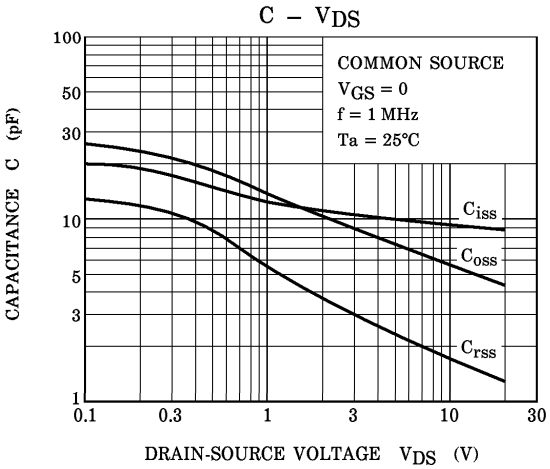
I_D – V_{GS}



$|Y_{fs}|$ – I_D

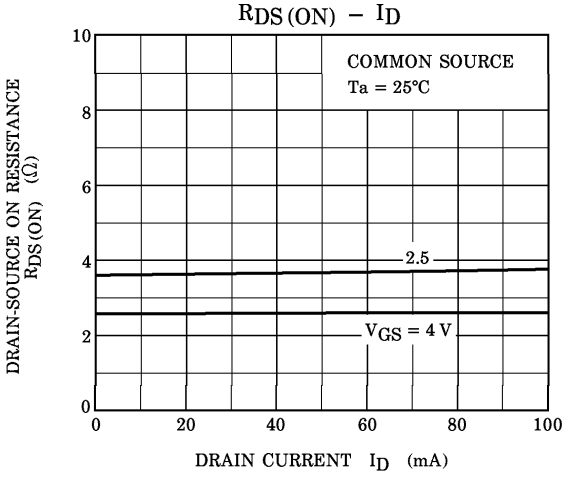


C – V_{DS}

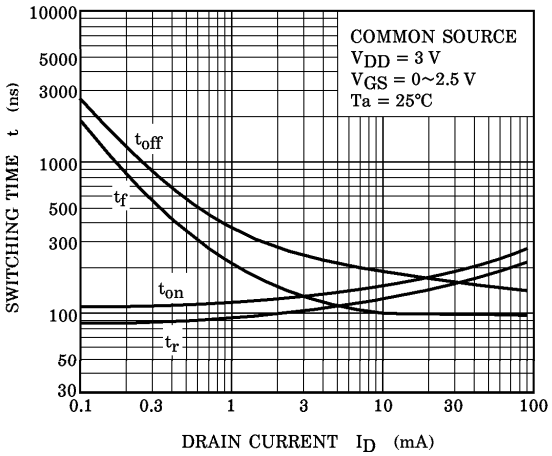


(Q1, Q2 COMMON)

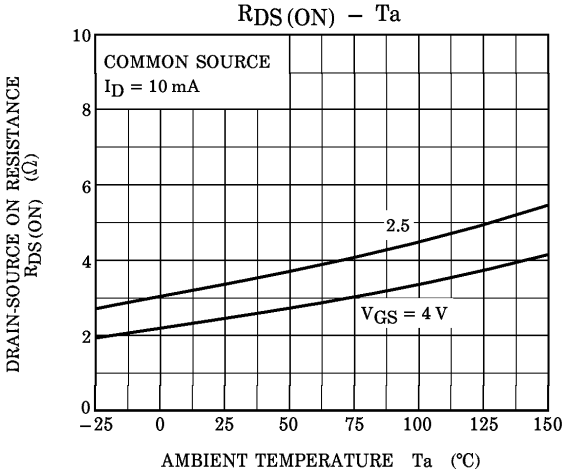
$R_{DS\,(ON)}$ – I_D



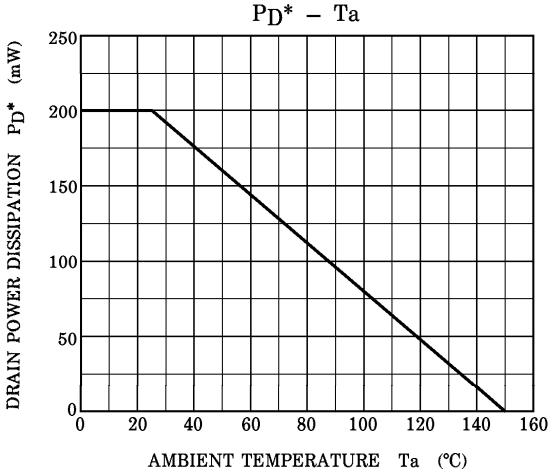
t – I_D



$R_{DS\,(ON)}$ – Ta



P_D* – Ta



*: Total Rating