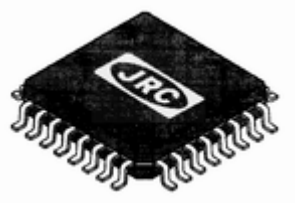
General Purpose Digital Signal Processor

■Package

■ General Description

The NJU26150 is a high performance 24-bit general purpose digital signal processor. The NJU26150 has an internal program memory to download outside EEPROM program. After download, the NJU26150 starts automatically.
The NJU26150 is suitable for any kind of audio products, such as AV Receiver, Car Audio.



NJU26150

■ FEATURES

- Pin assignment is same as the NJU26100 Series. The common PCB is available for the NJU26150.
- After being ROMed (NJU26100 Series), no change is necessary for PCB and host processor program.
- The NJU26150 is useful for reducing time-to-market and a product with specification-change possibility.
- 2K words Delay Memory (word=16bits)
- 4K words Program Memory (word=16bits)

■ Digital Signal Processor Specification

- 24bit Fixed-point Digital Signal Processing
- Maximum Clock Frequency : 38MHz
- Digital Audio Interface : 3 Input ports / 3 Output ports
- Power Supply : DSP Core : 2.5V, I/O interface: 2.5V (+3.3V tolerant)
- Package : QFP 32pin

The detail hardware specification of the NJU26150 is described in the " NJU26100 Series Hardware Data Sheet". In respect to software commands, request NJR.

■ Function Block Diagram

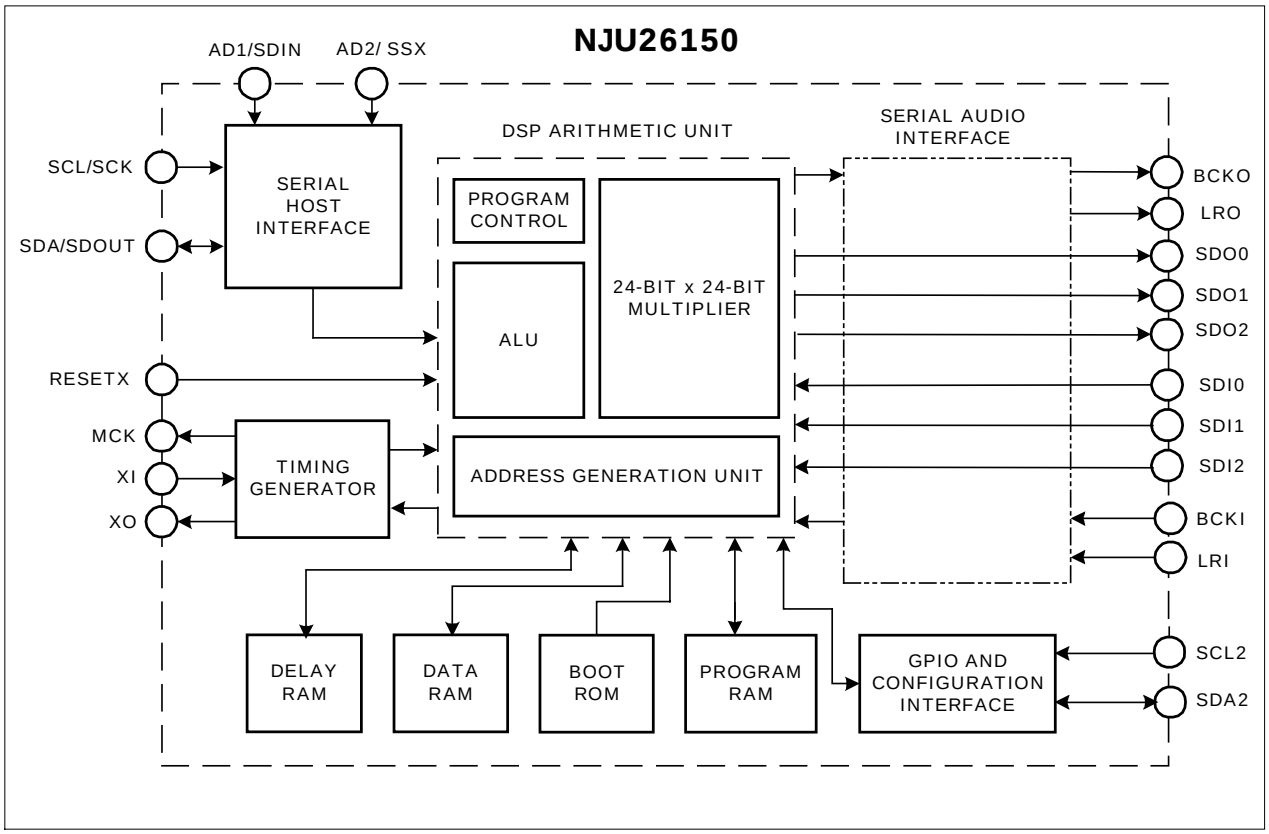


Fig. 1 NJU26150 Block Diagram

■ Pin Configuration

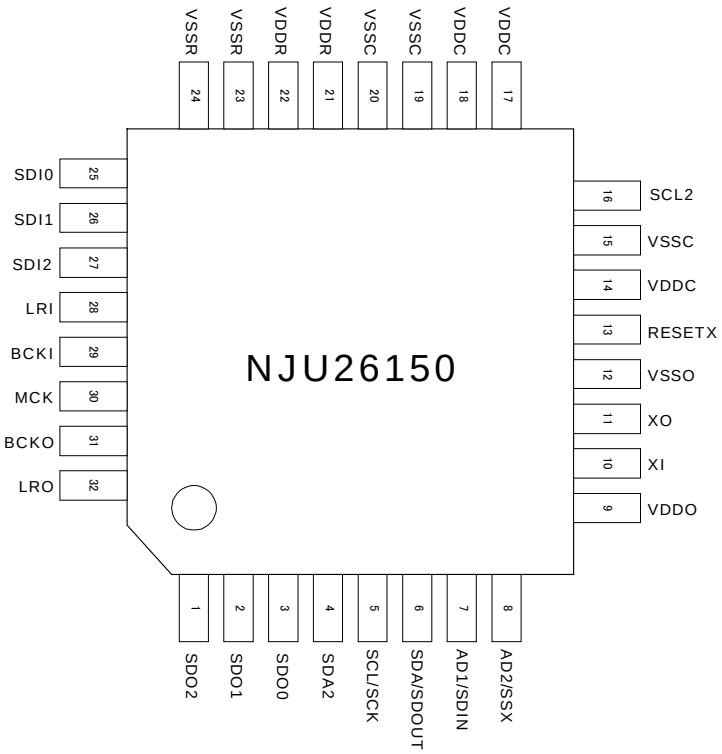


Fig. 2 NJU26150 Pin Configuration

■ Pin Description

Table 1 Pin Description

No.	Pin Name	I/O	Pin Description	No.	Pin Name	I/O	Pin Description
1	SDO2	O	Audio Data Output 2	17	VDDC	P	DSP Core Power Supply +2.5V
2	SDO1	O	Audio Data Output 1	18	VDDC	P	DSP Core Power Supply +2.5V
3	SDO0	O	Audio Data Output 0	19	VSSC	G	DSP Core Power Supply GND
4	SDA2	IO	I/O Data, Pull-up	20	VSSC	G	DSP Core Power Supply GND
5	SCL/SCK	I	I^2C clock / Serial clock	21	VDDR	P	I/O Power Supply +2.5V
6	SDA/SDOUT	IO	I^2C I/O / Serial Out	22	VDDR	P	I/O Power Supply +2.5V
7	AD1/SDIN	I	I^2C Address / Serial In	23	VSSR	G	I/O Power Supply GND
8	AD2/SSX	I	I^2C Address/Serial enable	24	VSSR	G	I/O Power Supply GND
9	VDDO	P	OSC Power Supply +2.5V	25	SDI0	I	Audio Data Input 0
10	XI	I	OSC Clock Input	26	SDI1	I	Audio Data Input 1
11	XO	O	OSC Clock Output	27	SDI2	I	Audio Data Input 2
12	VSSO	G	OSC Power Supply GND	28	LRI	I	LR Clock Input
13	RESETX	I	Reset	29	BCKI	I	Bit Clock Input
14	VDDC	P	DSP Core Power Supply +2.5V	30	MCK	O	A/D,D/A Clock Output
15	VSSC	G	DSP Core Power Supply GND	31	BCKO	O	Bit Clock Output
16	SCL2	IO	Clock Output	32	LRO	O	LR Clock Output

* I : Input, O : Output, IO : Bi-directional, P : +Power, G : GND * Package is shown in fig. 3.

■ Audio Data Output

The NJU26150 audio interface provides industry standard serial data formats of I^2S, MSB-first left-justified or MSB-first right-justified. The NJU26150 audio interface provides three data inputs, SDI0, SDI1,SDI2 and three data outputs, SDO0, SDO1, SDO2 as shown in table 2 and 3.

Table 2 Serial Audio Input Pin

Symbol	Pin No.	Description
SDI0	25	Audio Data Input 0
SDI1	26	Audio Data Input 1
SDI2	27	Audio Data Input 2

Table 3 Serial Audio Output Pin

Symbol	Pin No.	Description
SDO0	3	Audio Data Output 0
SDO1	2	Audio Data Output 1
SDO2	1	Audio Data Output 2

■ I^2C address

AD1 and AD2 pins are used to configure the seven-bit SLAVE address of the serial host interface. These pins offer additional flexibility to SLAVE address. 4 addresses could be chosen by AD1 and AD2-pin. The AD1 and AD2-pin addresses are decided by the connections of AD1 and AD2-pin. The AD1 and AD2 addresses should be the same level as AD1 and AD2-pin connections.

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Table 4 I^2C Bus SLAVE Address

bit7	bit6	bit5	bit4	Bit3	bit2	bit1	bit0
0	0	1	1	1	AD2*[1]	AD1*[1]	R/$\overline{W}$

*1 AD1 or AD2 address is 0 when AD1 or AD2-pin is “L”. AD1 or AD2 address is 1 when AD1 or AD2-pin is “H”.

The detail **I^2C** bus timing of the NJU26150 is described in the “ NJU26100 Series Hardware Data Sheet”.

■ Application

The application circuit diagram of the NJU26150 is shown in Fig.3a and Fig.3b.

- The NJU26150 and EEPROM realize the function of the NJU261xx shown in Fig.3a. The program exists in EEPROM. The program is downloaded into the NJU26150. The NJU26150 pin 4 (SDA2) should be connected to VDD through a 4.7K-ohm resister.
- The NJU261xx pin connections are shown in Fig.3b. The EEPROM is deleted. In case of selecting **I²C**, the NJU261xx pin 4(SEL1) should be connected to GND through a 4.7K ohm resister.
  *Notice: In case of selecting Serial bus, the NJU261xx pin 4 (SEL1) should be connected to VDD through a 4.7K ohm resister.

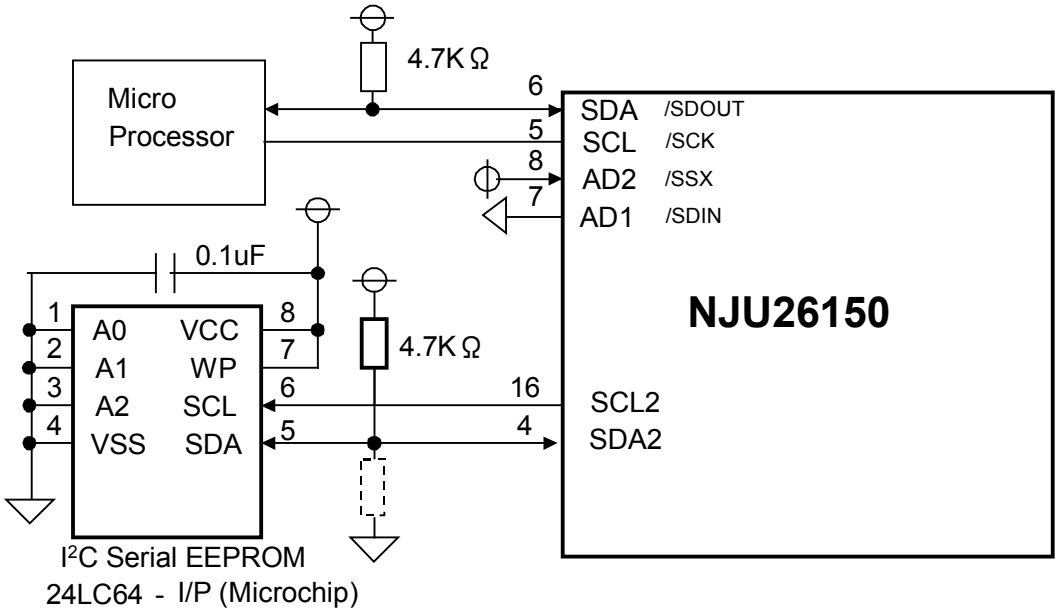

Fig. 3a NJU26150 application on circuit diagram

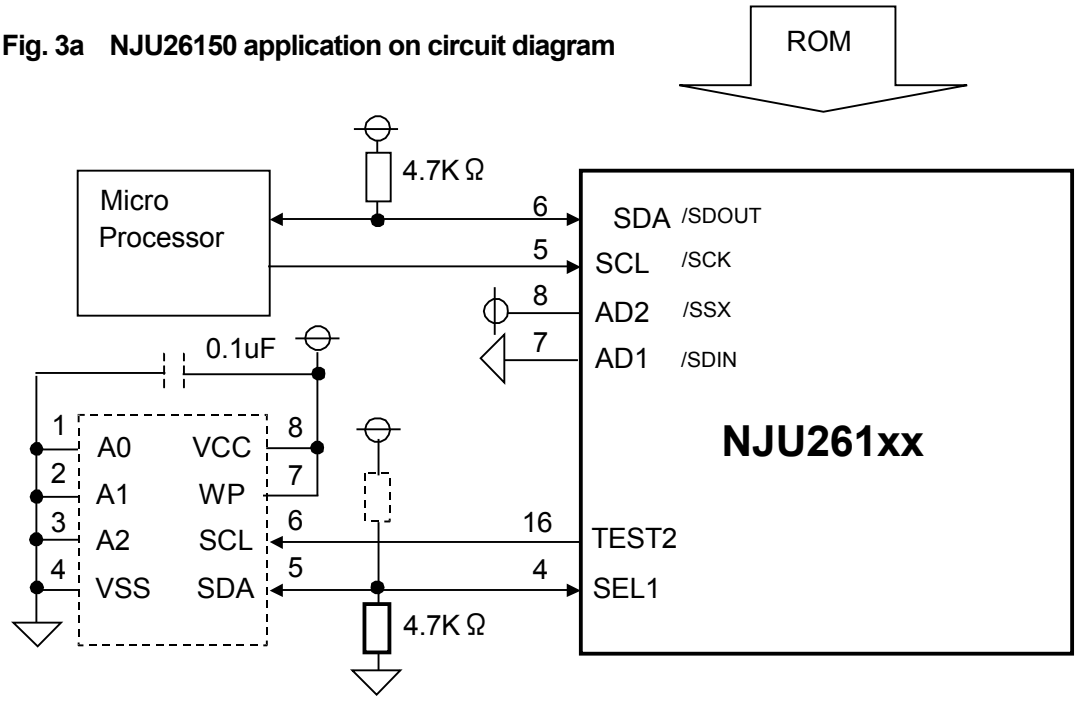

Fig. 3b NJU261xx application on circuit diagram

■ Download Procedure

The procedure of the download to the NJU26150 is described as follows.

1) Micro Processor releases RESET.
2) The NJU26150 starts download procedure from EEPROM automatically.
3) Send NOP command (0xff) and read the NJU26150 in order to check download procedure. When the reply status is 0x83, the download procedure is under running. When the reply status is 0x80, the download procedure is finished.

* In download procedure, the NJU26150 does not accept the command. The unacceptable command period is shown in table 5.

Table 5 Unacceptable command time after RESET

System Clock	Fs	Unacceptable command time after RESET
36.864MHz	48KHz	1sec
33.868MHz	44.1KHz	1sec
24.576MHz	32KHz	1.5sec

Table 6 EEPROM List (Reference Data)

Maker	**Part Number**	**VDD**	**Package**
ATMEL	AT24C64	1.8 - 5.5V	PDIP, SOIC, TSSOP
Micro Chip	24AA64 24LC64	1.8 - 5.5V 2.5 - 5.5V	PDIP, SOIC, TSSOP, MSOP
SAMSUNG	KS24L641	2.0 - 5.5V	DIP, SOP
SII	S-24CV64A	1.8 - 5.5V	DIP, SOP, TSSOP
AKM	AK6012AF	1.8 - 5.5V	SOP
ST-Micro	M24C64-R	1.8 - 5.5V	PDIP, SO, TSSOP
Rohm	BR24C64/F	2.7 - 5.5V	DIP, SOP
Hitachi	HN58X2464	1.8 - 5.5V	SOP, TSSOP

■ License Information

1. Purchase of **I²C** components of New Japan Radio Co. ,Ltd or one of sublicensed Associated Companies conveys a license under the Philips **I²C** Patent Rights to use these components in an **I²C** system, provided that the system conforms to the **I²C** Standard specification as defined by Philips.

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