MX97102

ISDN S/T CONTROLLER

FEATURES

- Pin-to-Pin and Register-to-Register compatible with Siemens 2186
- Full duplex 2B+D ISDN S/T Transceiver according to CCITT I.430
- GCI digital interface
- 3 types of 8-bit CPU interface
- Receive timing recovery with adaptively switched thresholds
- D-channel access control
- LAPD(HDLC) support with FIFO(2x64) buffers
- Activation/Deactivation
- Multiframing with S and Q bit access
- CPU access to B and IC channels
- Watchdog timer
- Package types : P-LCC-44, P-LQFP-64

GENERAL DESCRIPTIONS

MX97102 implements the 4-wire S/T interface used to link voice/data terminals to an ISDN. It is designed for the user site of the ISDN-basic access, two 64kbit/s B channels and a 16kbit/s D channel.

MX97102 can be mainly divided into three portions according to their interfaces. Except these three interface functions, it also provides the LAPD controller which handles the HDLC packets of the ISDN D-channel for the associated microprocessor.

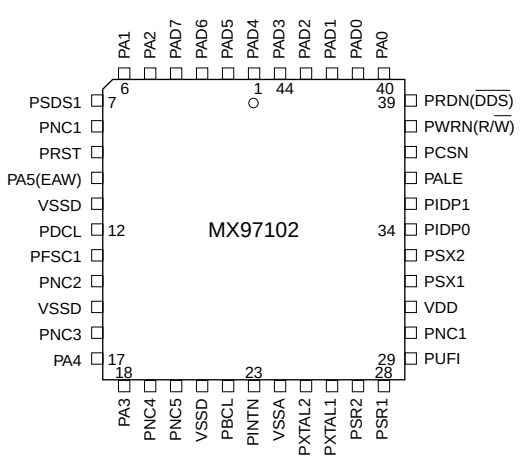
The first, S/T interface controller, provides all electrical and logical functions of the S/T interface, such as S/T transceiver, activation/deactivation, timing recovery, multiframe S and Q channels, and D-channel access and priority control for communicating with remote equipments.

The Second is the microprocessor interface controller which offers the registers compatible with Siemens PSB2186, provides three types of microprocessor interface, such as Motorola bus mode, Intel multiplexed mode and Intel non-multiplexed mode.

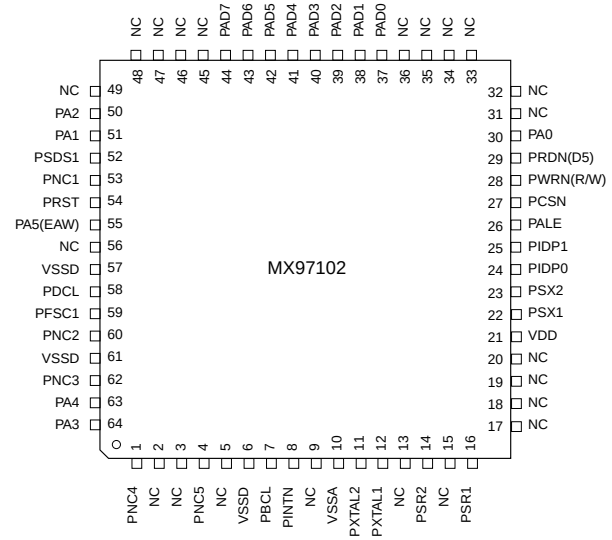
The last portion is the GCI interface controller which is used to connect different voice/data application modules for local digital data exchangements.

PIN CONFIGURATION

44-PLCC



64-PLQFP



BLOCK DIAGRAM

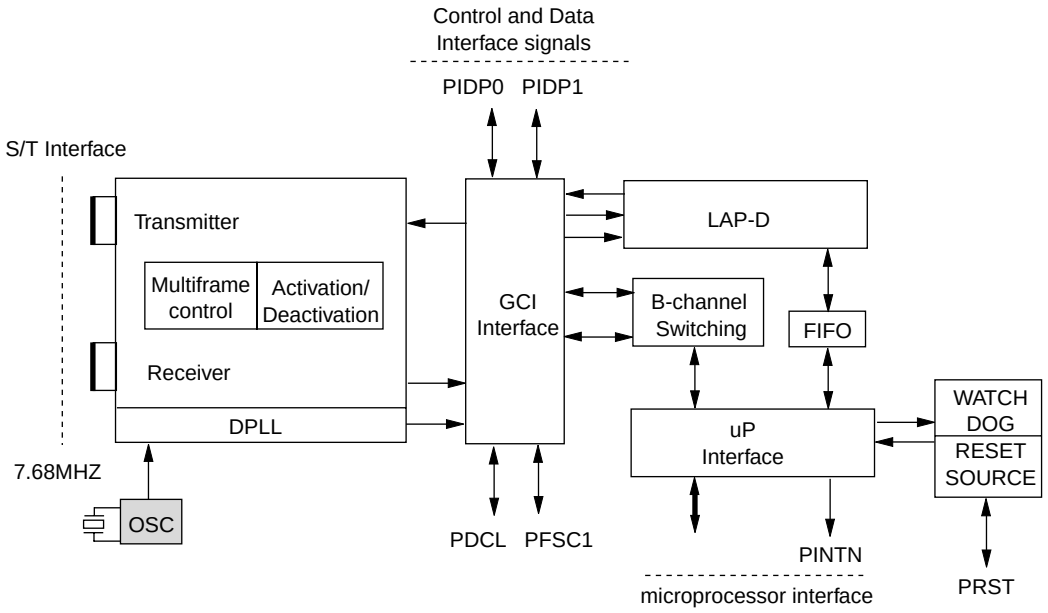


FIGURE 2: FUCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION (44-PIN)

TABLE 1: MX97102 PIN DESCRIPTIONS

PAD#	PIN NAME	I/O	DESCRIPTION
41	PAD0(D0)		Multiplexed Bus Mode:Address/data bus from the CPU system to this device
42	PAD1(D1)		and data between the CPU system and this device,
43	PAD2(D2)		Non-Multiplexed Bus Mode:Data bus between the CPU system and this
44	PAD3(D3)	I/O	device.
1	PAD4(D4)		
2	PAD5(D5)		
3	PAD6(D6)		
4	PAD7(D7)		
37	PCSN	I	ChipSelect:A logic "LOW" enable this device for a read/write operation.
38	PWRN(R/$\overline{W}$)	I	Read/Write:A logic "HIGH" indicates a valid read operation by CPU. A logic "LOW" indicates a valid write operation by CPU.(Motorola bus mode) Write:A logic "LOW" indicates a write operation.(Intel bus mode)
39	PRDN($\overline{DS}$)	I	Data Strobe: The rising edge marks the end of a valid read or write operation (Motorola bus mode). Read:A logic "LOW" indicates a read operation.(Intel bus mode)
23	PINTN	Open Drain	Interrupt Request:The signal is a logic "LOW" when this device requests an interrupt. It is an open drain output.
8, 4 16, 19 20,30	PNC1~PNC5 PUFI		No used.
36	PALE	I	Address Latch Enable:A logic "HIGH" indicates an address on the address/ data bus(Multiplexed bus type only). ALE also selects the micro-processor interface type (multiplexed or non-multiplexed).
9	PRST	I/O	Reset:A logic "HIGH" on this input forces this device into reset state. The minimum pulse length is four DCL-clock periods or four ms. If the terminal specific functions are enabled,this device may also output a reset signal.
13	PFSC1	O(I)	Frame Sync 1:Frame sync output. Logic "HIGH" during channel 0 on the GCI interface. This pin becomes Input if Test Mode is programmed (register ADF1).
12	PDCL	O(I)	Data Clock:Clock of frequency, 1536kHz output, equals to twice the GCI data rate. This pin becomes Input if Test Mode is programmed (register ADF1)

TABLE 1: MX97102 PIN DESCRIPTIONS(Continued)

PAD#	PIN NAME	I/O	DESCRIPTION
			(non-multiplexed bus mode)
40	PA0		Address Bit 0
6	PA1		Address Bit 1
5	PA2		Address Bit 2
18	PA3		Address Bit 3
17	PA4		Address Bit 4
10	PA5(EAW)		Address Bit 5; External Awake, when terminal specific function enabled, this pin is used as an external awake line. If a falling edge on this input is detected, it generates an interrupt and a reset pulse.
22	PBCL	O	Bit Clock:Clock of frequency 768kHz equal to the GCI data rate.
7	PSDS1	O	Serial Data Strobe 1:A programmable strobe signal, selecting either one or two B or IC channels on GCI interface, is supplied via this line. (register ADF2)
11, 15			
21	VSSD	-	Digital ground
24	VSSA	-	Analog ground
31	VDD	-	Power supply (5V±5%)
26	PXTAL1	I	Connection for crystal or external clock input.
25	PXTAL2	O	Connection for external crystal. Left unconnected if external clock is used.
27	PSR2		
28	PSR1	I	S-Bus Receiver Input
32	PSX1		S-Bus Transmitter Output(positive)
33	PSX2	O	S-Bus Transmitter Output(negative)
34	PIDP0(DD)		GCI-Data Port 0 (DD)
35	PIDP1(DU)	I/O	GCI-Data Port 1 (DU)
			Open drain without internal pull-up resister or push-pull.

ABSOLUTE MAXIMUM RATINGS

TABLE 2: ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Maximum Supply Voltage (VDD)	6V
DC Input Voltage on any pin	-0.4Vto VDD+0.4V
Storage Temperature Range	-55℃ to 150℃
Operating Free Air Temperature Range	0℃ to 70℃

DC CHARACTERISTICS

TABLE 3: DC CHARACTERISTICS

Temperature from 0 to 70℃; VDD = 5V±5%, VSSA = 0V, VSSD = 0V

Symbol	Parameter	Conditions	Min. Value	Max. Value	Unit	Remarks
VIL	L-input voltage		-0.4	0.8	V	
VIH	H-input voltage		2.0	VDD+0.4	V	All pins except
VOL	L-output voltage	IOL= 2mA		0.45	V	PSX1, PSX2,
VOL1	L-output voltage (IDP0)	IOL= 7mA		0.45	V	PSR1, PSR2
VOH	H-output voltage	IOH= -400uA	2.4		V	
VOH	H-output voltage	IOH= -100uA				
			VDD-0.5		V	
ILI	Input leakage current	0<VIN<VDD to 0V		±10		All pins except
ILO	Output leakage current	0<VOUT<VDD to 0V		±10	uA	BCL, PSX1,2, PSR1,2, PA0, PA1, PA3, PA4
ILIPD	Input leakage current, internal pull-down	0<VIN<VDD to 0V		120	uA	PA0, PA1, PA3, PA4, BCL
VX	Absolute value of output pulse amplitude (VSX2 - VSX1)	RL = 50W RL = 50W	2.03 2.10	2.31 2.39	V	PSX1, PSX2
IX	Transmitter output current	RL = 5.6W	7.5	13.4	mA	
RX	Transmitter output impedance	Inactive or during binary one during binary zero RL = 50W	10 0	kW W		
VSR1	Receiver output voltage	IO < 5uA	2.35	2.6	V	PSR1, PSR2
VTR	Receiver threshold voltage (VSR2 - VSR1)	Dependent on peak level	225	375	mV	

AC CHARACTERICS

TABLE 4: CRYSTAL SPECIFICATION

PARAMETER	SYMBOL	Limit values	UNIT
Frequency	f	7.680	MHz
Frequency calibration tolerance		max. 100	ppm
Load capacitance	CL	max. 50	pF
Oscillator mode		fundamental	

XTAL1 Clock Characteristics (external oscillator input)

TABLE 5: CLOCK CHARACTERISTICS

Parameter	Limit values	
	min.	max.
Duty cycle	1:2	2:1

Temperature from 0 to 70℃, VDD = 5V±5%
Inputs are driven to 2.4V for a logical "1" and to 0.4V for a logical "0" . Timing measurements are made at 2.0V for a logical "1" and 0.8V for a logical "0". The AC-testing output is loaded with a 150pF capacitor.

TIMING WAVE FORM

MICROPROCESSOR INTERFACE TIMING----INTERL BUS MODE

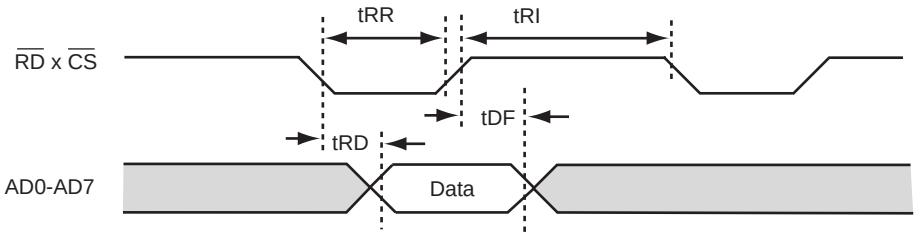


FIGURE 3(a) MICROPRCESSOR READ CYCLE IN INTEL BUS MODE

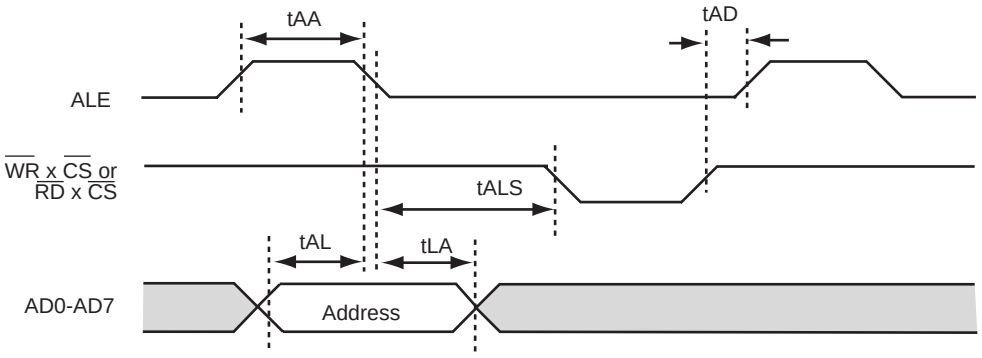


FIGURE 3(b) MICROPROCESSOR WRITE CYCLE IN INTEL BUS MODE

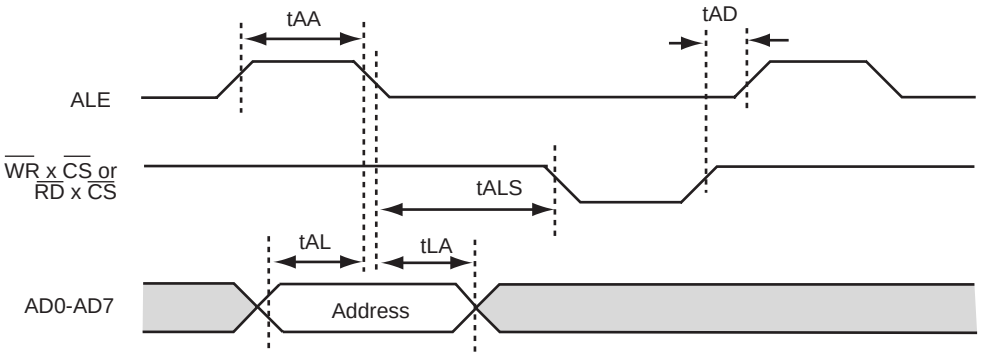


FIGURE 3(c) MULTIPLEXED ADDRESS TIMING IN INTEL BUS MODE

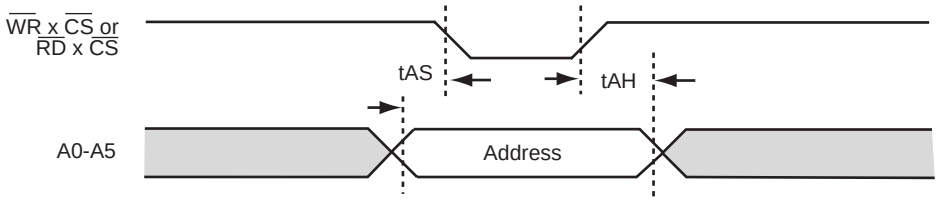


FIGURE 3(d) NON-MULTIPLEXED ADDRESS TIMING IN INTEL BUS MODE

MOTOROLA BUS MODE

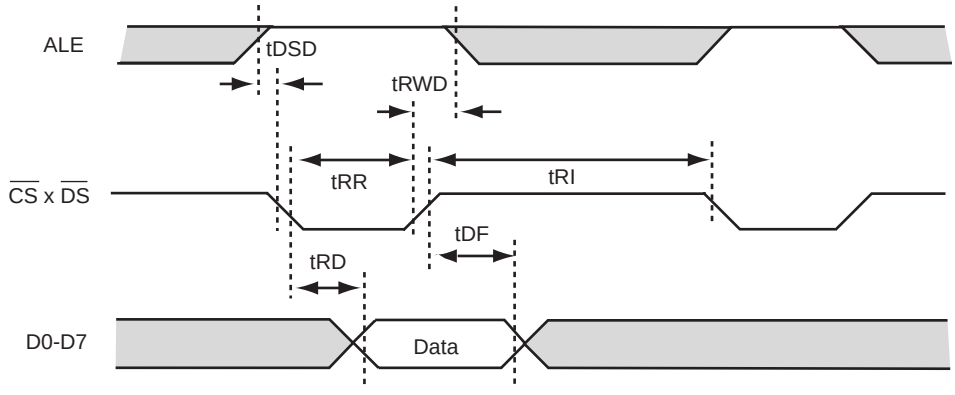


FIGURE 4(a) MICROPROCESSOR READ TIMING IN MOTOROLA BUS MODE

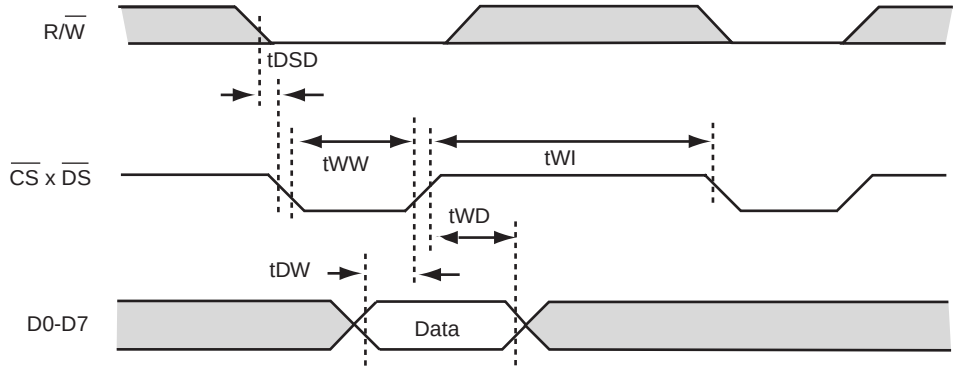


FIGURE 4(b) MICROPROCESSOR WRITE TIMING IN MOTOROLA BUS MODE

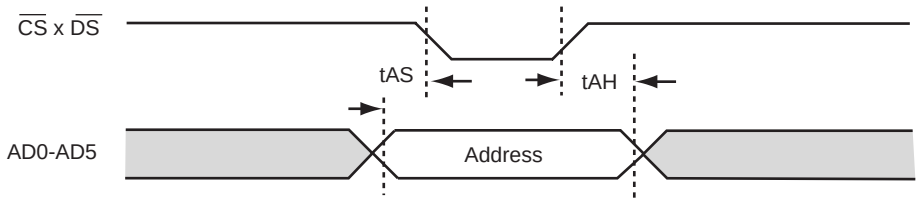


FIGURE 4(c) NON-MULTIPLEXED ADDRESS TIMING IN MOTOROLA BUS MODE

TABLE 6: PARAMETERS FOR MICROPROCESSOR INTERFACE TIMING

PARAMETER	SYMBOL	Limit Value		UNIT
		min.	max.	
ALE pulse witdh	tAA	50		ns
Address setup time to ALE	tAL	15		ns
Address hold time to ALE	tLA	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	tALS	0		ns
Address setup time	tAS	25		ns
Address hold time	tAH	10		ns
ALE guard time	tAD	15		ns
$\overline{DS}$ delay after $\overline{RW}$ setup	tDSD	0		ns
$\overline{RD}$ pulse width	tRR	110		ns
Data ouput delay from $\overline{RD}$	tRD		110	ns
Data float from $\overline{RD}$	tDF		25	ns
$\overline{RD}$ control interval	tRI	70		ns
$\overline{W}$ pulse width	tWW	60		ns
Data setup time to $\overline{W}$, CS	tDW	35		ns
Data hold time from $\overline{W}$, CS	tWD	10		ns
$\overline{W}$ control interval	tWI	70		ns

APPLICATIONS

ISDN ACCESS ARCHITECTURE

MX97102 is designed especially for subscriber terminal equipment with S/T interfaces, Four wire, two pairs for transmission and receiption separately, are connected to the NT equipment at the user site. Via the NT equipment, subscribers could dial up to the wide-area network with the traditional telephone line. The NT serves a converter between the U interface at the exchange and the S interface at the user premises. The NT may be either an NT1 only or an NT1 together with an NT2 connected via the T interface which is physically identical to the S interface. NT2 may include higher level functions like multiplexing and switching as in a PBX. Figure 5 illustrates the connections between the user site to the public domain of central office.

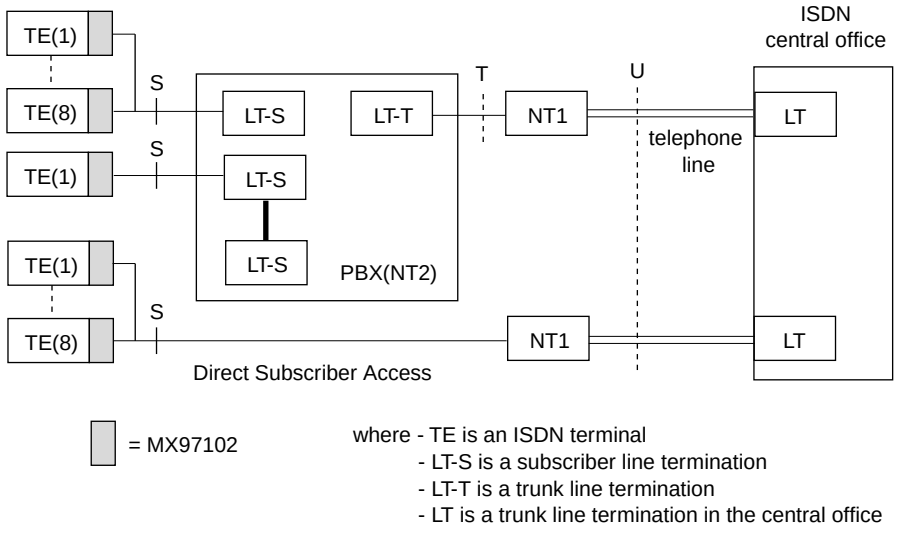


FIGURE 5 : ISDN - BASIC SUBSCRIBER ACCESS ACHITECTURE

MX97102 is based on the ISDN basic access, 192kbit/s, which consists of two circuit-switched 64 kbit/s B channels and a message oriented 16kbit/s D channel for packetized data, signaling and telemetry information. The D channel is processed by the LAPD controller contained in the MX97102 and routed via a parallel CPU interface to the terminal processor. The high level support of the LAPD protocol which is implemented by the MX97102 allows the use of a low cost processor in cost sensitive applications.

GCI CONNECTION

With the GCI interface, MX97102 could connect different voice/data (V/D) application modules. Up to eight D-channel components may be connected to the D and C/I (Command/Indication) channels (TIC-bus). TIC-bus arbitration is also implemented in MX97102.

Data transfers between the MX97102 and the V/D modules are done with the help of the GCI MONITOR channel protocol. Each V/D module can be accessed by an individual address. Two intercommunication channels IC1 and IC2 allow a 2*64kbit/s transfer rate between voice/data modules. Figure 6 shows one GCI connection, data module A uses D-channel for data transfer, a voice processor is connected to a programmable digital processing codec filter via IC1 and a data encryption module to a data device via IC2. Meanwhile, B1 is used for voice communication, B2 for data communication.

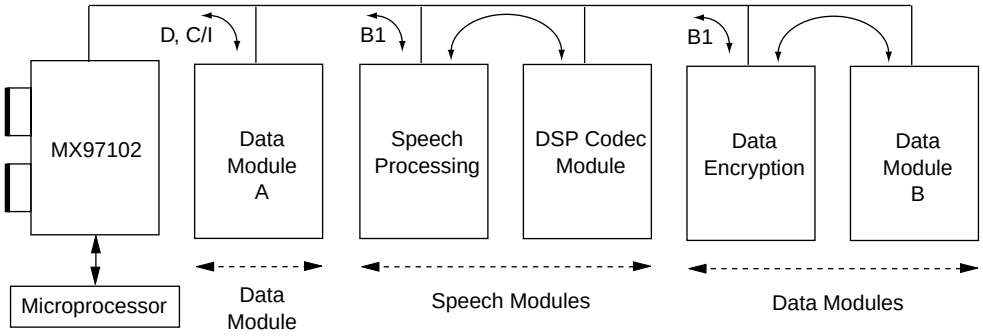


FIGURE 6: EXAMPLES OF GCI CONNECTION

MICROPROCESSOR INTERFACE CONNECTION

Single-chip microcontroller, such as 8048, 8031 or 8051, can meet the need of MX97102. MX97102 is built in various microprocessor interface, it fits perfectly into almost any 8-bit microprocessor system environment. The microprocessor interface can be selected to be either of the Motorola type (with control signals CS, R/W, DS) of the Siemens/Intel non-multiplexed bus type (with control signals CS, WR, RD) or of the Siemens/Intel multiplexed address/data bus type (with WR, RD, ALE).

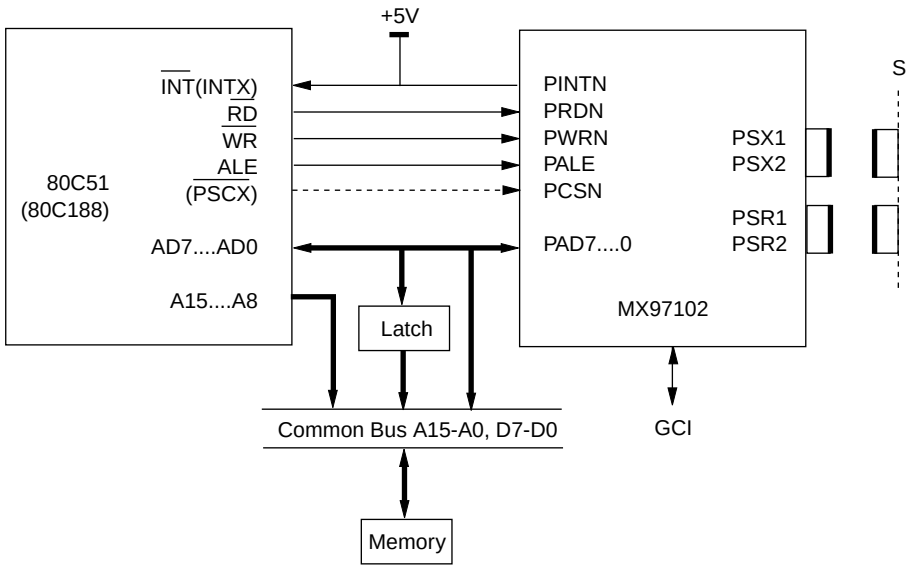
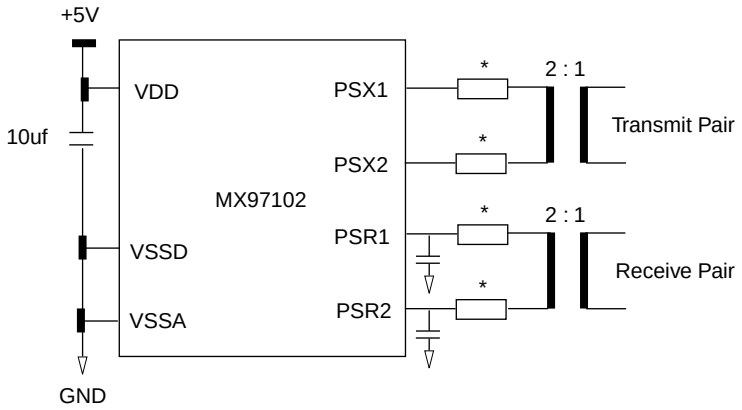


FIGURE 7: CONNECTING THE MX97102 TO INTEL MICROCONTROLLER

S/T INTERFACE

Line transceiver functions for the S/T interface follows the electrical specifications of CCITTI.430. According to this standard, pseudo-ternary encoding with 100% pulse width is used on the S/T interface. For both receive and transmit direction, a 2:1 transformer is used to connect the MX97102 transceiver to the 4 wire S/T interface.



Note : * ----- See MXIC design spec. document 8012-0530

FIGURE 8: MX97102 EXTERNAL S-INTERFACE CIRCUITRY

The receiver is changed as a threshold detector with adaptively switched threshold levels. Pin PSR1 delivers 2.5V as an output, which is the virtual ground of the input signal on pin PSR2.

INTERNAL REGISTER

TABLE 7: HDLC OPERATION AND STATUS REGISTERS

Addr. (hex)	Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
00-1F	FIFO	R/W									Tx/Rx FIFO address
20	ISTA	R	RME	RPF	RSC	XPR	TIN	CISQ	SIN	EXI	Interrupt Status Register
20	MASK	W	RME	RPF	RSC	XPR	TIN	CISQ	SIN	EXI	Mask Register
21	STAR	R	XDOV	XFW	XRNR	RRNR	MBR	MAC1	X	MAC0	Status Register
21	CMDR	W	RMC	RRES	RNR	STI	XTF	XIF	XME	XRES	Command Register
22	MODE	R/W	MDS2	MDS1	MDS0	TMD	RAC	DIM2	DIM1	DIM0	Mode Register
23	TIMR	R/W	CNT	CNT	CNT	V	A	L	U	E	Timer Register
24	EXIR	R	XMR	XDU	PCE	RFO	SOV	MOS	SAW	WOV	Extended Interrupt Register
24	XAD1	W									Transmit Address 1
25	RBCL	R	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0	Receive Frame Byte Count Low
25	XAD2	W									Transmit Address 2
26	SAPR	R									Received SAPI
26	SAP1	W	SAPI1	SAPI1	SAPI1	SAPI1	SAPI1	SAPI1	CRI	0	Individual SAPI 1
27	RSTA	R	RDA	RDO	CRC	RAB	SA1	SA0	C/R	TA	Receive Status Register
27	SAP2	W	SAPI2	SAPI2	SAPI2	SAPI2	SAPI2	SAPI2	MCS	0	Individual SAPI 2
28	TEI1	W	TEI1	TEI1	TEI1	TEI1	TEI1	TEI1	TEI1	EA	Individual TEI 1
29	RHCR	R									Receive HDLC Control
29	TEI2	W	TEI2	TEI2	TEI2	TEI2	TEI2	TEI2	TEI2	EA	Individual TEI 2
2A	RBCH	R	XAC	VN1	VN0	OV	RBC11	RBC10	RBC9	RBC8	Receive Fram Byte Count High
2B	STAR2	R	0	0	0	0	WFA	MULT	TREC	SDET	Status Register 2
2B	STAR2	W	0	0	0	0	0	MULT	0	0	Status Register 2

TABLE 8: SPECIAL PURPOSE REGISTERS

Addr. (hex)	Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Description
30	SPCR	R/W	SPU	0	0	TLP	C1C1	C1C0	C2C1	C2C0	Serial Port Control Reg.
31	CIR0	R	SQC	BAS	CODR0	CODR0	CODR0	CODR0	CIC0	CIC1	Command/Indication Receive 0
31	CIX0	W	RSS	BAC	CODX0	CODX0	CODX0	CODX0	1	1	Command/Indication Transmit 0
32	MOR0	R									MONITOR Receive 0
32	MOX0	W									MONITOR Transmit 0
33	CIR1	R	CODR1	CODR1	CODR1	CODR1	CODR1	CODR1	MR1	MX1	Command/Indication Receive 1
33	CIX1	W	CODX1	CODX1	CODX1	CODX1	CODX1	CODX1	1	1	Command/Indication Transmit 1
34	MOR1	R									MONITOR Receive 1
34	MOX1	W									MONITOR Transmit 1
35	C1R	R/W									Channel Register 1
36	C2R	R/W									Channel Register 2
37	B1CR	R									B1-Channel Register
37	STCR	W	TSF	TBA2	TBA1	TBA0	ST1	ST0	SC1	SC0	Sync Transfer Control Register
38	B2CR	R									B2-Channel Register
38	ADF1	W	WTC1	WTC2	TEM	PFS	IOF	0	0	ITF	Additional Feature Reg.1
39	ADF2	R/W	IMS	0	0	0	ODS	D1C2	D1C1	D1C0	Additional Feature Reg.2
3A	MOSR	R	MDR1	MER1	MDA1	MAB1	MDR0	MER0	MDA0	MAB0	MONITOR Status Reg.
3A	MOCR	W	MRE1	MRC1	MXE1	MXC1	MRE0	MRC0	MXE0	MXC0	MONITOR Control Reg.
3B	SQRR	R	IDC	CFS	CI1E	SYN	SQR1	SQR2	SQR3	SQR4	S-,Q-Channel Receive Register
3B	SQXR	W	IDC	CFS	CI1E	SQIE	SQX1	SQX2	SQX3	SQX4	S-,Q-Channel Transmit Register
3C	ADF3	R/W	0	0	0	0	STM1	STM0	MAX1	MAX0	Additional Feature Reg.3

ORDERING INFORMATION

PART NO.	PACKAGE
MX97102QC	44 PIN PLCC
MX97102UC	64 PIN LQFP

REVISION HISTORY

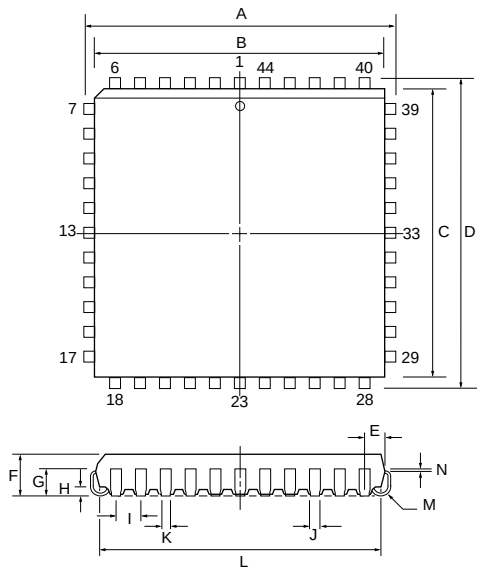
Rev. No.	Description	Page	Date
1.1	Preliminary release		JULY/28/1997
1.2	Change editing Add ordering information and revision history Change words in drawings Add "not used" pins in pin descriptions		NOV/1997
1.3	Page6, Table 3 changed		NOV/1997
1.4	Wording errors		APR/14/1998
1.5	Change feature description		MAY/21/1998
1.6	Storage Temperature Range " -65℃ to 125℃" replaced by "-55℃ to 150℃"	P4	JUN./15/1998
1.7	Add 64-pin package		AUG/21/1998
1.8	Made for CD-ROM release		SEP/15/1998
1.9	Modify 64-pin package outline data		OCT/20/1998
2.0	64 PIN P-LQFP PACKAGE INFORMATION content changed	P16	OCT/27/1998

PACKAGE INFORMATION

44-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

ITEM	MILLIMETERS	INCHES
A	17.53 ± .12	.699 ± .005
B	16.59 ± .12	.653 ± .12
C	16.59 ± .12	.653 ± .12
D	17.53 ± .12	.690 ± .12
E	1.95	.077
F	4.70 max.	.185 max.
G	2.55 ± .25	.100 ± .010
H	.51 min.	.020 min.
I	1.27 [Typ.]	.050 [Typ.]
J	.71 ± .10	.028 ± .004
K	.46 ± .10	.018± .004
L	15.50 ± .51	.610 ± .020
M	.53 R	.025 R
N	.25 [Typ.]	.010 [Typ.]

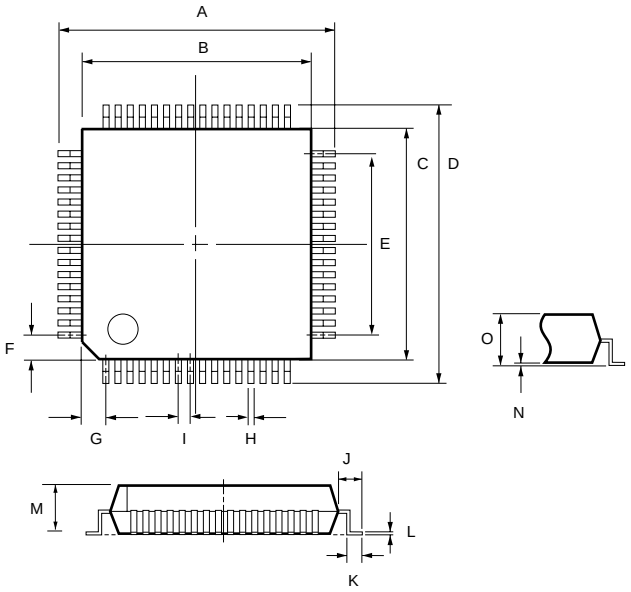
NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



64-PIN PLASTIC LOW-PROFILE QUAD FLAT PACKAGE (P-LQFP)

ITEM	MILLIMETERS	INCHES
A	16	.63
B	14	.55
C	14	.55
D	16	.63
E	12 [Typ.]	.47 [Typ.]
F	1 [Typ.]	.039 [Typ.]
G	1 [Typ.]	.039 [Typ.]
H	.35 ± .05	.014 ± .002
I	0.8	.031
J	1	.039
K	.6 ± .15	.024± .006
L	.15 ± .05	.006 ± .002
M	1.45 ± .05	.057 ± .002
N	.1 ± .05	.004 ± .002
O	1.6 [max.]	.063 [max.]

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-8888
FAX:+886-3-578-8887

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-747-2309
FAX:+65-748-4090

TAIPEI OFFICE:
TEL:+886-3-509-3300
FAX:+886-3-509-2200

MACRONIX AMERICA, INC.

TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com