AN1672/D

The ECL Translator Guide

PECL • LVPECL • NECL • TTL • LVTTL/LVCMOS • CMOS

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APPLICATION NOTE

Objective

This application note is intended to provide the basic device selection and connection information to enable signal translation interface between ON Semiconductor's ECL logic operating in various supply modes This document also provides information regarding translation between our ECL devices and TTL (5 V), CMOS (5 V), or LVTTL/LVCMOS (3.3 V) devices. For translation interface with LVDS, see AN1568.

Translation to and from ECL technology is discussed in three section divisions:

Section 1. Translation between differently supplied ECL drivers and receivers

Section 2. Translation from different ECL operating mode drivers to non ECL receivers

Section 3. Translation from non ECL drivers to different ECL operating mode receivers

Proper translation occurs when the driver's output logic levels are within the spec limits of the receiver and are recognized. Specific device data sheets should be consulted for exact specifications and parameter limits.

Resources

IBIS and SPICE models may be found at www.onsemi.com for most devices. General ECL information, also online, may be consulted such as AND8020, AND8066, and AND8072.

General Background

TTL and CMOS drivers generally source current (to the receiver) in the HIGH state and sink current (from the receiver) in the LOW state. In contrast, ECL drivers source current in both HIGH and LOW states (to the receiver). Receiver inputs do not require any "termination" although any driver may or may not require termination considerations. The driver termination considerations may be located physically near or internal to a receiver.

TTL and CMOS devices will usually be operated across a single positive power supply (V_{CC} or V_{DD}) and ground. ECL devices may operate similarly across a single Positive supply and V_{EE} (Ground) as Positive ECL (PECL) or Low Voltage Positive ECL (LVPECL). Or traditionally, ECL devices may span across Ground and a single negative power supply, V_{EE}, as Negative ECL (NECL) or Low Voltage Negative ECL (LVNECL). Any device may be operated with all pins offset by a fixed voltage, but interface with standard levels may require a translation device. A pure ECL device might be operated in NECL, PECL, or LVPECL mode by simply shifting all voltage levels. Of course, a translator dedicated to a specific technology will expect only fixed voltages and can't usually operate in different, or shifted voltage modes.

Different ECL operating supply modes are generally considered to be as presented below in Table 1.

Table 1. ECL Operating Supply Modes

PECL	V_{CC} = 5.0, V_{EE} = 0.0
LVPECL	V_{CC} = 3.3, V_{EE} = 0.0
2.5VPECL	V_{CC} = 2.5, V_{EE} = 0.0
2.5VNECL	V_{CC} = 0.0, V_{EE} = −2.5
LVNECL	V_{CC} = 0.0, V_{EE} = −3.3
NECL	V_{CC} = 0.0, V_{EE} = −5.0

Some devices may span one or more operating modes and each mode will allow supply tolerances. ECL signal levels (V_{OL}, V_{OH}, V_{IL}, and V_{IH}) are referenced from the V_{CC} pin or positive rail. Therefore, when ECL devices are operated from different negative power supplies, no translation is required for interconnects. When operated in a single ended configuration, the critical Input parameters are V_{IL} and V_{IH} limits (V_{IHCMR} and V_{pp} are ignored). When operation differentially, critical limit Input parameters are V_{IHCMR} and V_{pp} (V_{IL} and V_{IH} are ignored). See AND8066 for interconnect details. All supply pins, V_{CC}, LVCC, and GND, must be connected for proper operation. A 0.1 μF to 0.01 μF decoupling cap is recommended from V_{CC} to GND. V_{CC} ripple should be minimized and may require additional filter networks.

Standard non ECL operating modes are generally considered (with certain supply tolerances) to be as presented below in Table 2.

Table 2. Non ECL Operating Supply Modes

V_{CC} = 5.0, V_{EE} = 0.0
V_{CC} = 3.3, V_{EE} = 0.0
V_{CC} = 2.5, V_{EE} = 0.0

Most translation interface between technologies will require a separate, dedicated translator IC device, but some newer ECL devices offer a translation feature integrated into certain mode control pins. Several of the GigaComm™ devices offer a programmable mode pins for selecting the control pins translation levels. MC10EP195 offers Delay Select pins with user programmable TTL, CMOS, or ECL threshold levels.

An alternative translation technique, cap coupling, is discussed in Application Note AND8020, Section 5. Cap coupling may accommodate level shifting when the signal's "edge density" is sufficient. Otherwise, coding may be required to increase "edge density". Certainly the risk of erroneous levels, due to the coupling cap leakage, may not be acceptable and system requirements may demand the hard levels found with active device translation.

Section 1: Translation Between Differently Supplied ECL Drivers and Receivers

Table 3. Translation Between Differently Supplied ECL Drivers and Receivers

To: From:	PECL V_{CC} = +5 V	LVPECL V_{CC} = +3.3 V	LVNECL V_{EE} = −3.3 V	NECL V_{EE} = −4.5 to −5.2 V
PECL V_{CC} = +5 V	Standard Connection	LVEL92	LVEL91	EL91
LVPECL V_{CC} = +3.3 V	EL17 EP17 LVEL16 LVEL17	Direct Connection	LVEL91 LVEP91	LVEP91
LVNECL V_{EE} = −3.3 V	EL90	LVEL90	Standard Connection	Direct Connection
NECL V_{EE} = −4.5 V to −5.2 V	EL90	LVEL90	Standard Connection	Standard Connection

From PECL to LVPECL

The MC100LVEL92 translates signals from a PECL (V_{CC} = 5.0, V_{EE} = 0.0) operating mode driver to a LVPECL V_{CC} = 3.3, V_{EE} = 0.0 operating mode receiver.

From PECL to NECL

The MC100EL91 translates signals from a PECL (V_{CC} = 5.0, V_{EE} = 0.0) operating mode driver to a NECL (V_{CC} = 0.0, V_{EE} = −5.0) operating mode receiver.

From PECL to LVNECL

The MC100LVEL91 translates signals from a PECL (V_{CC} = 5.0, V_{EE} = 0.0) operating mode driver to a LVNECL (V_{CC} = 0.0, V_{EE} = −3.3) operating mode receiver.

From LVPECL to PECL

The critical parameter for differential PECL receiver to properly interface with a differential LVPECL driver is $V_{IHCMRmin}$ (or V_{CMRmin}). V_{IH} and V_{IL} limits may be disregarded for differential receiving. Assuming no tangent loss from traces, if the LVPECL driver V_{OHmin} level is more positive (higher) than the $V_{IHCMRmin}$ spec of the differential PECL receiver, the device will properly translate or level shift from LVPECL to PECL. For example, suppose a MC100EP16 operating differentially in LVPECL mode (V_{CC} = 3.3, V_{EE} = 0.0) with a worst case V_{OHmin} of 2.155 V, drives a MC100EP17 receiver differentially operating in PECL mode (V_{CC} = 5.0, V_{EE} = 0.0). The MC100EP17 receiver spec $V_{IHCMRmin}$ is 2.0 V and will always properly recognize the drivers HIGH level 2.155 V (or higher). The MC100EL13, MC100EL14, MC100EL29, MC100EL56 are also acceptable as LVPECL receivers differentially.

Most of the “E” (ECLinPS), “EL” (ECLinPS Lite), 10H/100H, or 10xxx series devices do not have a sufficiently low $V_{IHCMRmin}$ to receive LVPECL.

When a receiver in LVPECL mode is driven single ended, the critical parameters will be V_{IL} and V_{IH}. $V_{IHCMRmin}$ (or V_{CMRmin}) may be ignored. A PECL receiver V_{ILmin}, typically >3.0 V, will be insufficiently low to recognize the drivers HIGH level and will not permit proper interconnect.

From LVPECL to LVNECL

The MC100LVEL91 translates signals from a PECL (V_{CC} = 5.0, V_{EE} = 0.0) operating mode driver to a LVNECL (V_{CC} = 0.0, V_{EE} = −3.3) operating mode receiver.

From LVPECL to NECL

The MC100EL91 translates signals from a LVPECL (V_{CC} = 3.3, V_{EE} = 0.0) operating mode driver to a NECL (V_{CC} = 0.0, V_{EE} = −5.0) operating mode receiver.

From LVNECL to PECL

The MC100EL90 translates signals from a LVNECL (V_{CC} = 0.0, V_{EE} = −3.3) operating mode driver to a PECL (V_{CC} = 5.0, V_{EE} = 0.0) operating mode receiver.

From LVNECL to LVPECL

The MC100LVEL90 translates signals from a LVNECL (V_{CC} = 0.0, V_{EE} = −3.3) operating mode driver to a PECL (V_{CC} = 3.3, V_{EE} = 0.0) operating mode receiver.

Section 2: Translation from Different ECL Operating Mode Drivers to Non ECL Receivers

The following table indicates the options available for translation from different ECL operating drivers to non ECL receivers.

Table 4. Translation from Different ECL Operating Mode Drivers to Non ECL Receivers

To: From:	TTL V_{CC} = +5 V	LVTTL/LVCMOS V_{CC} = 3.3 V	CMOS V_{DD} = 5 V
PECL V_{CC} = +5 V	H350 H607 ELT21 ELT23 ELT28*	LVEL92 + LVELT23 or EPT21 or EPT23 or LVELT23 or EPT26	PECL to TTL or PECL to LVTTL/LVCMOS Translator and HCT or ACT
LVPECL V_{CC} = +3.3 V	ELT21 ELT23	EPT21 EPT23 LVELT23 EPT26	LVPECL to LVTTL Translator and HCT or ACT Input
LVNECL V_{EE} = −3.3 V	ELT25 EPT25*	EPT25	LVNECL/TTL Translator to HCT or ACT Input
NECL V_{EE} = −4.5 to −5.2 V	H125 H601 H603 H605 H680* H681* ELT25 EPT25*	EPT25	NECL/TTL Translator to HCT or ACT Input

*See text segment for details

From PECL to TTL

MC10H350 as PECL to TTL

Several devices are offered for translation signals from PECL mode drivers to 5 V supplied TTL receivers. The MC10H350 operates over the frequency range from DC to about 50 MHz. Although operation is possible to 80 MHz, the output will not sustain full spec V_{OH} levels rolling off with higher frequency.

Open, floating differential inputs on a gate will force the TTL output to default LOW. By adding a pullup resistor of 1 kΩ to 4 kΩ, a device's output will directly interface with CMOS (5 V) inputs. The device input pin "common mode range", V_{IHCMR} min to max, is insufficient to allow recognition of LVPECL levels. Single ended operation of the MC10H350 will require an input signal swing of 700 mV peak−to−peak or greater.

Outputs are Enabled by Pin 9, $\overline{OE}$, going LOW. If left floating open, MC10H350 Pin 9 will default LOW. Worst case skew from Output to Output within a device occurs from Input falling edge to Output falling edge at 125°C at 1.4 ns. For the Input rising edge to Output rising edge, the worst case skew is about 1 ns (at −55°C). Device to Device slew is less than 800 ps skew from part to part. Output drive will come out of saturation with 80 mA − 100 mA, lowering V_{OH} levels.

MC10H607 / MC100H607 as PECL to TTL

The MC10H607 and MC100H607 are Registered PECL to TTL translators. A standard output test condition load is 50 pF and 500 Ω to GND. MR, Pin 19, will default LOW when floating open, allowing operation. The input pin "common mode" range is insufficient to allow recognition of LVPECL levels.

ELT21/23/28 as PECL to TTL

ECL inputs for ELT21/23/28 have 50 kΩ internal pulldown resistors. If both ECL ELT21/23 inputs are pulled below 1.3 V, an override circuit will force the output Q to HIGH, Qb LOW. By adding an output pullup resistor of 1 to 4 kΩ, a device will interface with CMOS (5 V) inputs. The input common mode range for ELT21 / ELT23 is generally considered to be sufficient (2.2 V) to allow recognition of PECL HIGH levels (>4 V) allowing translation. Single ended operation may be accomplished with a V_{BB} reference voltage placed on the nondriven differential input. If a V_{BB} pin is present, then it should be bypassed when used or left floating open when unused. A simple V_{BB} supply may be created by a resistor divider providing the proper switch point voltage to preserve duty cycle (see AND8066). A High Current may be created from a simple buffer gate as shown in AND8020, Figure 22.

These ELT TTL devices typically display >2X the required data sheet drive. For example, at V_{OLmax} (0.5 V) the required sinking drive current is 24 mA and actual drive >>50 mA. At V_{OHmin} (2.4 V), the spec sourcing drive current is 3.0 mA and the typical device will source >>8 mA. The unloaded V_{OH} max may reach as positive as 4.0 V.

Typical drive current strength of the TTL output is shown in the following two tables, Table 5 and Table 6, and their graphs, Figure 1 and Figure 2.

Table 5. ELT TTL Series Drive LOW Current (I_{OL}) vs Voltage (V_{OL})

I_{OL}	V_{OL}
0.010	0.162
0.020	0.209
0.030	0.256
0.040	0.303
0.079	0.465
0.118	0.628

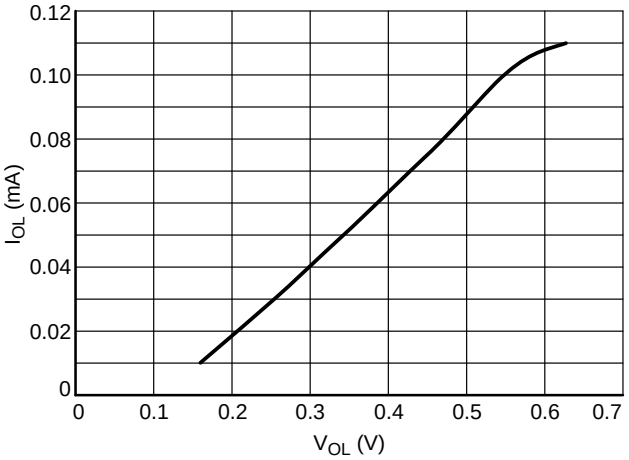

Figure 1. ELT TTL Series Drive LOW Current (I_{OL}) versus Voltage (V_{OL})

Table 6. ELT Series TTL Drive HIGH Current (I_{OH}) vs Voltage (V_{OH})

I_{OH}	V_{OH}
−0.0379	2
−0.0316	2.26
−0.0249	2.508
−0.0164	2.9
−0.0091	3.167
−0.0031	3.339
−0.001	3.4

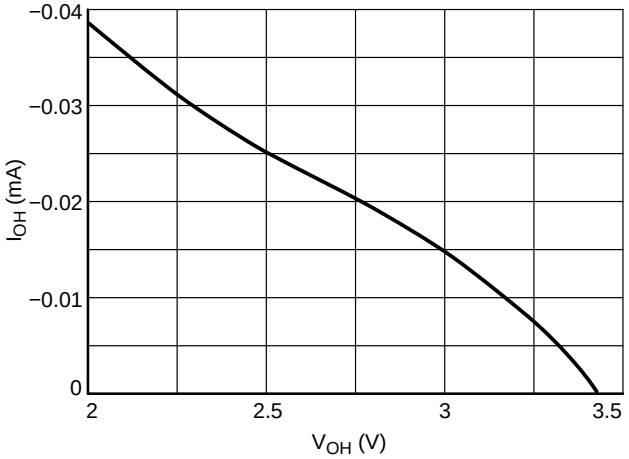

Figure 2. ELT Series TTL Drive HIGH Current (I_{OH}) versus Voltage (V_{OL})

Typical ELT TTL series output impedance in the HIGH state is about 43 Ω. In the LOW state output impedance is about 42 Ω.

Typical t_{PLH} and t_{PHL} may differ as much as 0.5 ns. At higher frequencies, the output swing will decrease. Gain is typically about five and inputs require a minimum of 200 mVpp swing. Jitter is typically 500 ps. Measurements are made at 1.5 V for AC characteristics such as t_{pd} and skew.

From PECL to LVTTL

This translation requires two devices for a direct, active connection. First, a level shift from PECL to LVPECL is done with the MC100LVEL92. Then, a translation from LVPECL to LVTTL is done with either the LVELT23, EPT21, EPT23, LVELT23, or EPT26 (see segment below).

No sequencing is needed in powering up the MC100LVEL92, although both Positive supply levels, V_{CC} and LVCC, must be connected for proper operation.

From PECL to CMOS

The translation from PECL to CMOS is accomplished through two stages, from PECL to an intermediary stage (such as either TTL or LVTTL), then from the intermediary stage to CMOS. When the intermediary stage is through TTL, then the final stage will be from TTL to CMOS using any of the HCT type devices (i.e., MC74HCT245A), or ACT (i.e., MC74ACT244).

From LVPECL to TTL

Translation from LVPECL to TTL will be similar to “PECL to LVTTL” and the prior segment should be reviewed. The input common mode range maximum (2.2 V) for ELT21 / ELT23 is generally considered to be sufficient to allow recognition of LVPECL HIGH levels (>2.2 V), thus allowing proper translation.

From LVPECL to LVTTL/LVCMOS

Devices MC100EPT21, MC100EPT23, MC100LVELT23, and MC100EPT26 translate LVPECL signals to LVTTL/LVCMOS. Standard levels for the LVTTL and LVCMOS are the same.

There are no “open input” default circuits to force the outputs to a determined state. Provisions should be taken to prevent auto−oscillation. If the inputs are permitted to converged on the same voltage (within the V_{IHCMR} range), or merely left floating, auto−oscillation will initiate.

There are no powerup sequence requirements or power sequence restrictions. If either V_{CC} or V_{EE} supplies are not present, such as during an open pin condition, the output falls to near zero without harm or damage to the device.

Outputs of these devices typically display about 2X the required data sheet drive. For example, at V_{OLmin} the drive is required to sink 24 mA and will typically sink >50 mA. At V_{OH}, the spec drive is −3.0 mA and will typically source >8 mA.

Typical drive current strength of the TTL output is shown in the following two tables, Table 7 and Table 8, and their graphs, Figure 3 and Figure 4.

Typical EPT TTL series output impedance in the HIGH state is about 5 Ω. In the LOW state output impedance is about 15 Ω.AC measurements are made to the 1.5 V point for the AC characteristics such as t_{pd} and skew.

Table 7. EPT TTL Series Drive LOW Current (I_{OL}) vs Voltage (V_{OL}) at 25°C

I_{out}	V_{out}
0.004	0.022
0.020	0.104
0.039	0.200
0.058	0.295
0.082	0.415
0.118	0.596
0.158	0.800
0.1963	1.000

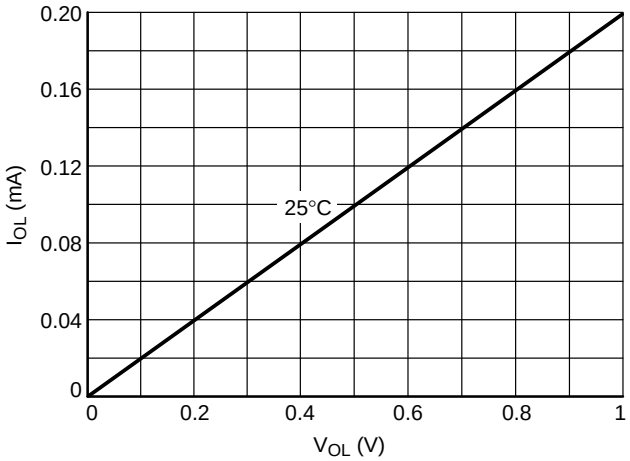

Figure 3. EPT TTL Series Drive LOW Current (I_{OL}) versus Voltage (V_{OL}) at 25°C

Table 8. EPT Series TTL Drive HIGH Current (I_{OH}) vs Voltage (V_{OH}) at 25°C

I_{out}	V_{out}
−0.0146	2.32
−0.0112	2.36
−0.0081	2.40
−0.0052	2.44
−0.0028	2.48
−0.0011	2.52
−0.0003	2.56

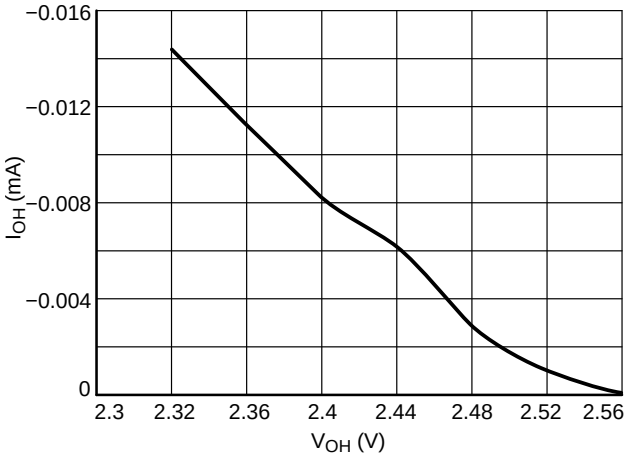

Figure 4. EPT Series TTL Drive HIGH Current (I_{OH}) versus Voltage (V_{OH})

From LVPECL to CMOS

Translation from LVPECL to CMOS will be similar to “PECL to CMOS” and that prior segment should be reviewed. The receiver input common mode range maximum must be sufficient to allow proper recognition of LVPECL HIGH levels (>2.2 V), thus allowing proper translation.

The LVPECL to CMOS translation is accomplished through two stages, first LVPECL to LVTTL, then from LVTTL to CMOS. Final stage devices may any of the HCT type devices (i.e., MC74HCT245A), or ACT (i.e., MC74ACT244).

From LVNECL to TTL

MC100ELT25 will translate from LVNECL to TTL. Note the V_{IHCMR} minimum is V_{EE} + 2.2 V. If a 3.3 V supply is available for the MC100EPT25, this device will translate LVNECL to TTL, reaching a V_{OH} of greater than 2.4 V up to 250 MHz.

From LVNECL to LVTTL/LVCMOS

MC100EPT25 will translate from LVNECL to LVTTL/LVCMOS.

From LVNECL to CMOS

Use a first stage of MC100ELT25 (or MC100EPT23 if a 3.3 V supply is available) and then use a final stage device of an appropriate HCT (i.e., MC74HCT245A) or ACT (i.e., MC74ACT244).

From NECL to TTL

Several devices are offered for translation signals from NECL mode drivers to 5 V supplied TTL receivers, but the MC10H125 is the standard translator. Special advantages may be realized with the MC10H6xx series devices. Review the device data sheets for specific devices features.

The MC10H125 operates over the frequency range from DC to about 50 MHz, although operation is possible >80 MHz with diminished output swing (reduced V_{OH} levels) with higher frequency. Open, floating differential inputs on a gate may allow the device to spontaneously auto oscillate unless provisions are taken to prevent the inputs from converging. An external network may be used to force a default state on the outputs when the inputs are open. Use a 50 kΩ pulldown on the noninverting input, then a 50 kΩ pullup and a 50 kΩ pulldown on the inverting input.

If a 3.3 V V_{CC} is available, the MC100EPT25 may be used on this supply to receive NECL and drive a TTL receiver. The MC100EPT25 V_{OH} will be limited to about 2.6 V at lower frequencies, decreasing at higher frequencies to 1.6 V V_{OH}, at 550 MHz (see data sheet). These may be sufficient levels for a TTL receiver.

From NECL to LVTTL/LVCMOS

MC100EPT25 will translate from NECL to LVTTL/LVCMOS.

From NECL to CMOS

Use a MC100EPT25 to translate from NECL to LVTTL/LVCMOS, and then any of the HCT type devices (i.e., MC74HCT245A), or ACT (i.e., MC74ACT244) to boost the levels to CMOS.

Section 3: Translation from Non ECL Drivers to Different ECL Operating Mode Receivers

Table 9. Translation from Non ECL Drivers to Different ECL Operating Mode Receivers

To: / From:	PECL V_{CC} = +5 V	LVPECL V_{CC} = +2.5 V	LVPECL V_{CC} = +3.3 V	LVNECL V_{EE} = −3.3 V	NECL V_{EE} = −4.5 to −5.2 V
TTL	H351 H606 ELT20 ELT22 ELT28*		ELT20, or ELT22, + LVEL92; if V_{IH} is limited to V_{CC} = 3.3 V use EPT20, EPT22, or LVELT22	ELT20 or ELT22 + LVEL91	H424 H124 H600 H602 H604 ELT24
LVTTL/LVCMOS/ HSTL/CML/LVDS V_{CC} = 2.5 V		NB100LVEP91		NB100LVEP91	NB100LVEP91
LVTTL/LVCMOS V_{CC} = 3.3 V	H351 H606 ELT20 ELT22 ELT28* OR: (EPT20 or EPT22 or EP24 or LVELT22) + 5 V PECL line receiver		EPT20 EPT22 LVELT22 MC100EPT622	EPT24 or NB100LVEP91	NB100LVEP91 or EPT24 + EL91
CMOS V_{DD} = +5 V	H352 ELT20 ELT22 ELT28		H352 + LVEL92	H352 + LVEL91	H352 + EL91

*Bidirectional

From TTL to PECL

An open, floating TTL input will drift to near V_{CC} and may inject noise into the device under this condition. It is recommended to tie any unused TTL input to V_{CC}.

MC10H351 as TTL to PECL

The MC10H351 operates over the frequency range from DC to >200 MHz. Although operation to higher frequencies is possible, the output V_{OH} levels will decrease, rolling off as frequency increases. TTL V_{CC} (Pin 11) would best be connected to the TTL logic devices positive supply, while ECL V_{CC} is recommended to be isolated to a separate PECL logic plane, if possible. V_{EE}, Pin 8, may be connected to the common ground plane.

An open, floating TTL input (Pins 7, 8, 9, 12, 14) will drift to near V_{CC} and considerations must be taken to reduce noise injected into the device under this condition, such as connecting unused inputs to V_{CC}. The Common Strobe pin is TTL type input.

Output to output skew is 150 ps worst case (at +70°C). Device to Device slew is less than 300 ps skew. Jitter is 40 to 60 ps.

MC10H606 / MC100H606 as TTL to PECL

This device offers translation and registration (reclocking) of TTL signals to PECL. Special advantages may be realized with this device, consult the device data sheets for specific features.

MC10ELT20 / MC100ELT20 and MC10ELT22 / MC100ELT22 as TTL to PECL

These devices do not sport any internal input resistor network to force a default level on an open floating pin. An open, floating TTL input (Pins 7, 8, 9, 12, 14) will drift to near V_{CC} and considerations must be taken to reduce noise injected into the device under this condition, such as connecting unused inputs to V_{CC}.

Higher operating frequency range will be affected by input swing; a higher input swing will allow a higher operating range.

From TTL to LVPECL

Translation from TTL to LVPECL requires a two−stage process: first TTL to PECL (with a 5 V supply) second PECL to LVPECL. The first may be accomplished per the segment above on TTL to PECL. The second stage is done with MC100LVEL92 (see also PECL to LVPECL segment).

Under the condition where the TTL signal is confined to not exceed 3.3 V, a MC10EPT20 / MC100EPT20, MC10EPT22 / MC100EPT22, or MC100LVELT22 may be used. The MC100LVELT22 has operation frequency band range from <1 Hz (with sufficiently sharp edges) to 600 MHz. Diode clamping may be used to prevent input signals from exceeding 3.3 V_{CC}.

From TTL to LVNECL

Translation from TTL to LVNECL is done in two stages:

1. Use TTL to PECL (ELT20 or ELT22)
2. Then use PECL to LVNECL Translation (LVEL91).

Both are described above. Alternatively, the first translation may be TTL to LVPECL and the second

translation would then be LVPECL to LVNECL Translation, still using the LVEL91.

If a −5 V supply is available, signals may be translated to NECL (see next segment) then ported to any LVNECL input.

From TTL to NECL

Several devices are available to accomplish TTL to NECL translation in a single package: the −H424, −H124, and the ELT24. Alternatively, translation from TTL to NECL could be done in two stages: first TTL to PECL (ELT20 or ELT22), second by passing though a PECL to NECL Translation (EL91). The NECL or LVNECL output levels could then be ported to any NECL or LVNECL receiver, since the levels are the same. No power supply sequencing is needed, but all supply connections are required for proper operation.

H424 as TTL to NECL

An “open”, floating TTL input will drift to near V_{CC} and considerations and may inject noise into the device under this condition. It is recommended to tie any unused TTL input to V_{CC}.

H124 as TTL to NECL

Although no supply sequencing is required, if the V_{EE} and GND are powered up prior to the V_{CC} connected, about 5 to 10 mA may be drawn from a “off” V_{CC} supply. This could draw the off V_{CC} supply to −0.25 V, depending in the internal “off” impedance.

H600 as TTL to NECL

This device boasts a 9 bit wide capability with a bandwidth from <1 Hz (with sufficiently sharp edges) to 250 MHz. The ECL Enable input has an internal 50 kΩ pulldown resistor to force an input default (LOW) state when floating open. When both the TTL and ECL Enable pins are forced LOW, the outputs will default to LOW.

H602 as TTL to NECL

This device has similarities to the −H600 with pulldown resistors on the ENECL, LEN, and MR inputs.

ELT24 as TTL to NECL

Use the MC100EPT24D with a V_{EE} “stand−off” resistor of about 61 Ω to drop the 1.7 V difference between V_{EE} of LVPECL and PECL (mean I_{EE} = 28 mA, sigma = 0.2 mA). This reduces the operating voltage across the device from 5.0 V V_{EE} supply to 3.3 V.

This device does not have an internal input resistor network to force a default level on an open, floating input pin. If floated open, the TTL input, Pin 2, will drift to near V_{CC} and may inject noise into the device. A 10 kΩ pullup resistor may be connected from Pin 2 to V_{CC} forcing a default state (Q HIGH) under open or floating input conditions.

From LVTTL/LVCMOS to PECL

Translation from LVTTL to PECL may be done in a single device such as the H351, H606, ELT20, ELT22, or through half of the ELT28.

For higher frequency operation, translation is done in two stages:

1. LVTTL to LVPECL using EPT20, EPT22, LVELT22, or EPT24
2. LVPECL signals into any PECL line receiver with a $V_{IHCMRmin}$ able to recognize a LVPECL HIGH level (such as EL17, EL14, EL13, etc.).

From LVTTL/LVCMOS to LVPECL

Use EPT20, EPT22, or LVELT22 to translate from LVTTL/LVCMOS to LVPECL

From LVTTL to LVNECL

Use the MC100EPT24D

From LVTTL to NECL

Translation from LVTTL/LVCMOS to NECL is done in two stages:

1. Use LVTTL/LVCMOS to LVPECL (EPT20, EPT22, LVELT22)
2. Then use LVPECL to NECL (EL91).

From CMOS to PECL

The MC10H352 offers inputs with proper CMOS detect levels for translating 5.0 V CMOS signals to PECL levels.

Non CMOS detect level devices may be used such as ELT20, ELT22, and ELT28 for expended frequency range with some small loss in duty cycle.

From CMOS to LVPECL

Translation from CMOS to LVPECL is done in two stages:

1. CMOS to PECL using a MC10H352 (or similar)
2. Then use a PECL to LVPECL translator, MC100LVEL92.

From CMOS to LVNECL

Translation from CMOS to LVNECL is done in two stages:

1. CMOS to PECL using a MC10H352 (or similar)
2. Then use PECL to LVNECL via MC100LVEL91.

From CMOS to NECL

Translation from CMOS to NECL is done in two stages:

1. CMOS to PECL using a MC10H352 (or similar);
2. Then use PECL to NECL translator, MC100EL91.

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