



HyperTransport™ to PCI Bridge

SP1011

Product Brief

Overview

The SP1011 is the first HyperTransport™-to-PCI Bridge that interfaces the new generation of HT based microprocessors (μP) and micro-controllers (μC) to PCI based peripherals. It also connects HT based hosts (μP and μC) to HT based peripherals. The SP1011 expands the possibilities for today system architects and designers by providing design options based on HyperTransport never possible before.

The SP1011 supports 64-bit, 66-MHz PCI operations and implements two bidirectional 8-bit HyperTransport™ interfaces that provide 800 MByte per second of bandwidth in each direction. Up to 31 devices

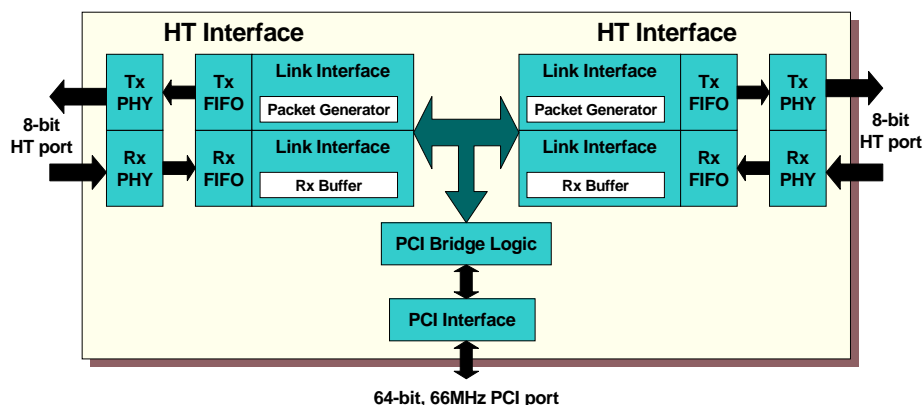
can be daisy-chained to build higher capacity systems with multiple PCI busses and HT based peripherals. A fairness algorithm allocates bandwidth among devices, thereby eliminating starvation of bridges at the end of the chain.

The SP1011 breathes new life into systems which are encumbered by the limits of traditional PCI fabrics. It reduces the time to market, design complexity and system costs of PCI and HT based systems.

Key Features

- Two Bidirectional 8-bit HyperTransport™ interfaces
 - Up to 400MHz DDR (Double Data Rate) for peak bandwidth of 800 MB/s simultaneously in each direction
- Complies with HyperTransport™ 1.0 Interface specification (Lightning Data Transport Interface Specification Rev 1.0)
 - Supports 8-bit links only and no Dynamic frequency reprogramming
- Tunnels between the two HyperTransport™ interfaces
- No protocol-induced maximum HyperTransport™ link length, which allows system designers to optimize speed vs. distance
- The HT interfaces support double hosted chain (Host CPU on each port)
- 64-bit, 66MHz PCI bus
- Complies with PCI local Bus Specifications, Rev. 2.2
 - Supports with parity and error checking features
- Supports daisy-chaining up to 31 devices. The bandwidth is shared among the devices using a fairness algorithm
- Programmable interrupt controller with up to 16 interrupts
- Built-in 2-level PCI arbiter with support for up to 6 devices
 - Can also be configured to support an external arbiter
- Programmable pre-fetch of up to 1024 bytes, among up to four outstanding requests
- Transaction forwarding for the following commands:
 - All I/O and memory commands
 - Type 1 to Type 1 configuration commands (downstream only)
 - Type 1 to Type 0 configuration commands (downstream only)
- Internal buffers to support high-speed operation, including:
 - 512-bytes HyperTransport™ forwarding
 - 192-bytes upstream write
 - 64-bytes downstream write
 - 1024-bytes upstream read
 - 192-bytes downstream read
- 40-bit memory mapped space and 25-bit I/O space
- Evaluation board available with firmware & software drivers
- 4.5 Watt max, 2.5V core, 1.2V HT IO, 3.3V PCI IO
- 352-pin SBGA package

Device Block Diagram



Summary of Benefits

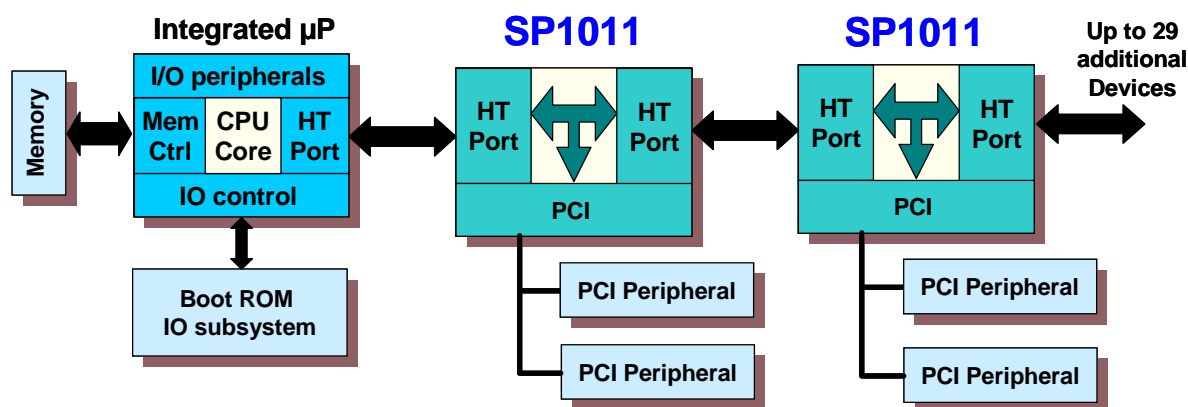
- Bridges between HyperTransport and legacy PCI bus, breathing new life into legacy systems, which are encumbered by the limits of traditional PCI fabrics
- 1.6GB/sec bandwidth supports the needs of data transfer applications
- Host CPUs can be connected to both HT interfaces for greater system flexibility and sharing PCI based resources
- Supports PCI Plug-N-Play reduces system design complexity and time to market
- Low power consumption increases system reliability
- Built-in PCI arbiter reduces system cost
- Uses existing PCI drivers and firmware to reduce system development and debug time
- 31 devices can be daisy-chained to enable a flexible and modular system implementation
- Deterministic low latency per tunnel meets the requirements of real-time applications

Target Applications

The feature set of the SP1011 makes it ideal for a variety of computing and embedded systems including:

- Enterprise LAN Switches
- Storage Systems and Switches (SAN, NAS, RAID, FC)
- Firewalls and Security Gateways
- High End Computing Systems
- Servers and Server Clusters
- Printers, Graphics and Imaging Systems
- VPN Switches / Routers
- Edge and Access Routers
- MAN Switches
- Wireless Gateways
- Voice and Multimedia Access Gateways
- Multiservice Access Concentrators
- IP Service Switches and Core Routers
- Test Equipment and Network Probes

System Block Diagram



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