Integrated Circuit Systems, Inc.

ICS83905I

LOW SKEW, 1:6 CRYSTAL INTERFACE-TO-LVCMOS / LVTTL FANOUT BUFFER

GENERAL DESCRIPTION

The ICS83905I is a low skew, 1-to-6 LVCMOS / LVTTL Fanout Buffer and a member of the HiPerClockS™family of High Performance Clock Solutions from ICS. The low impedance LVCMOS/LVTTL outputs are designed to drive 50W series or parallel terminated transmission lines. The effective fanout can be increased from 6 to 12 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS83905I is characterized at full 3.3V, 2.5V, and 1.8V, mixed 3.3V/2.5V, 3.3V/1.8V and 2.5V/1.8V output operating supply mode. Guaranteed output and part-to-part skew characteristics along with the 1.8V output capabilities makes the ICS83905I ideal for high performance, single ended applications that also require a limited output voltage.

FEATURES

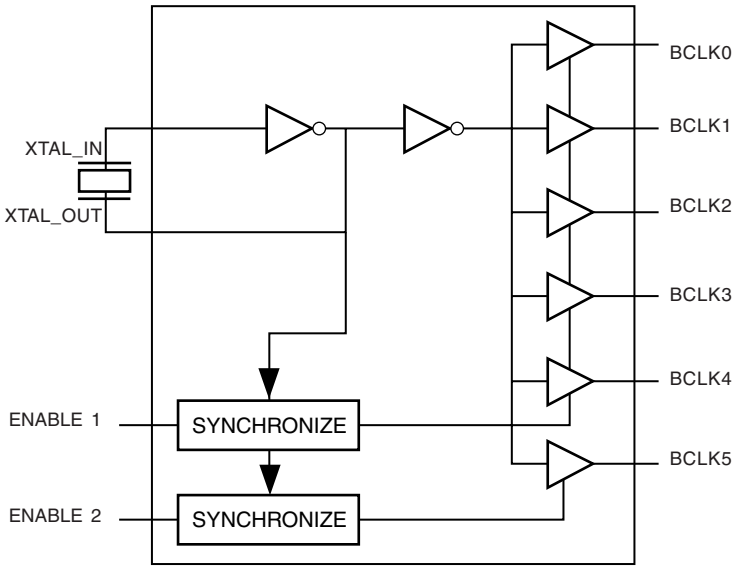
- 6 LVCMOS / LVTTL outputs
- Outputs able to drive 12 series terminated lines
- Crystal oscillator interface
- Crystal input frequency range: 10MHz to 40MHz
- Output skew: 80ps (maximum)
- RMS phase jitter @ 25MHz, (100Hz - 1MHz): 0.26ps (typical) (V_{DD} = V_{DDO} = 2.5V)

  Phase noise:

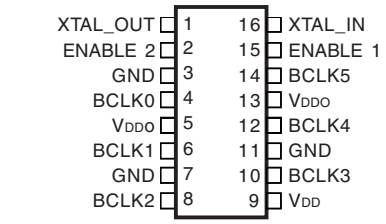
Offset	Noise Power
100Hz	-129.7 dBc/Hz
1kHz	-144.4 dBc/Hz
10kHz	-147.3 dBc/Hz
100kHz	-157.3 dBc/Hz

- 5V tolerant enable inputs
- Synchronous output enables
- Operating power supply modes:
  Full 3.3V, 2.5V and 1.8V,
  mixed 3.3V core/2.5V output operating supply,
  mixed 3.3V core/1.8V output operating supply,
  mixed 2.5V core/1.8V output operating supply
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS83905I
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm body package
G Pacakge
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	XTAL_OUT	Output		Crystal oscillator interface. XTAL_OUT is the output.
2, 15	ENABLE 2, ENABLE 1	Input		Clock enable. LVCMOS / LVTTL interface levels. See Table 3.
3, 7, 11	GND	Power		Power supply ground.
4, 6, 8, 10, 12, 14	BCLK0, BCLK1, BCLK2, BCLK3, BCLK4, BCLK5	Output		Clock outputs. LVCMOS / LVTTL interface levels.
5, 13	V_{DDO}	Power		Output supply pin.
9	V_{DD}	Power		Core supply pin.
16	XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDO} = 3.465V			19	pF
		V_{DDO} = 2.625V			18	pF
		V_{DDO} = 2V			16	pF
R_{OUT}	Output Impedance	V_{DDO} = 3.3V ± 5%		7		Ω
		V_{DDO} = 2.5V ± 5%		7		Ω
		V_{DDO} = 1.8V ± 0.2V		10		Ω

TABLE 3. OUTPUT ENABLE AND CLOCK ENABLE FUNCTION TABLE

Control Inputs		Outputs	
ENABLE 1	ENABLE 2	BCLK0:BCLK4	BCLK5
0	0	LOW	LOW
0	1	LOW	Toggling
1	0	Toggling	LOW
1	1	Toggling	Toggling

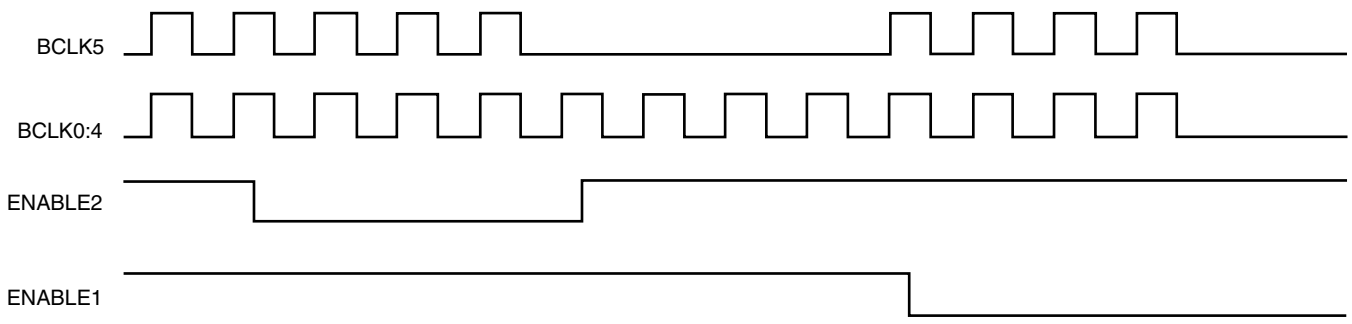


FIGURE 1. ENABLE TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA} 16 Lead TSSOP package	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	ENABLE 1:2 = 00			10	mA
I_{DDO}	Output Supply Current	ENABLE 1:2 = 00			5	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	ENABLE 1:2 = 00			8	mA
I_{DDO}	Output Supply Current	ENABLE 1:2 = 00			4	mA

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		1.6	1.8	2.0	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current	ENABLE 1:2 = 00			5	mA
I_{DDO}	Output Supply Current	ENABLE 1:2 = 00			3	mA

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	ENABLE 1:2 = 00			10	mA
I_{DDO}	Output Supply Current	ENABLE 1:2 = 00			4	mA

TABLE 4E. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current	ENABLE 1:2 = 00			10	mA
I_{DDO}	Output Supply Current	ENABLE 1:2 = 00			3	mA

TABLE 4F. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 2.5V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current	ENABLE 1:2 = 00			8	mA
I_{DDO}	Output Supply Current	ENABLE 1:2 = 00			3	mA

TABLE 4G. LVCMOS/LVTTL DC CHARACTERISTICS, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	ENABLE 1, ENABLE 2	V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
			V_{DD} = 1.8V ± 0.2V	0.65*V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	ENABLE 1, ENABLE 2	V_{DD} = 3.3V ± 5%	-0.3		0.8	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
			V_{DD} = 1.8V ± 0.2V	-0.3		0.35*V_{DD}	V
V_{OH}	Output High Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1	2.6			V
			V_{DDO} = 2.5V ± 5%; I_{OH} = -1mA	2			V
			V_{DDO} = 2.5V ± 5%; NOTE 1	1.8			V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1	V_{DDO} - 0.3			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1			0.5	V
			V_{DDO} = 2.5V ± 5%; I_{OL} = 1mA			0.4	V
			V_{DDO} = 2.5V ± 5%; NOTE 1			0.45	V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1			0.35	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		DC		100	MHz
odc	Output Duty Cycle			48		52	%
*t*sk(o)	Output Skew; NOTE 2, 4					80	ps
*t*jit(Ø)	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.13		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		800	ps
t_{EN}	Output Enable Time; NOTE 3	ENABLE 1				4	cycles
		ENABLE 2				4	cycles
t_{DIS}	Output Disable Time; NOTE 3	ENABLE 1				4	cycles
		ENABLE 2				4	cycles

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.
Terminated at 50Ω to $V_{DDO}/2$.
NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		DC		100	MHz
odc	Output Duty Cycle			47		53	%
*t*sk(o)	Output Skew; NOTE 2, 5					80	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3		25MHz @ (Integration Range: 100Hz-1MHz)		0.26		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		800	ps
t_{EN}	Output Enable Time; NOTE 4	ENABLE 1				4	cycles
		ENABLE 2				4	cycles
t_{DIS}	Output Disable Time; NOTE 4	ENABLE 1				4	cycles
		ENABLE 2				4	cycles

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.
Terminated at 50Ω to $V_{DDO}/2$.
NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Please refer to phase noise plot.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6C. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		DC		100	MHz
odc	Output Duty Cycle			47		53	%
*t*sk(o)	Output Skew; NOTE 2, 4					80	ps
*t*jit(Ø)	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.27		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		900	ps
t_{EN}	Output Enable Time; NOTE 3	ENABLE 1				4	cycles
		ENABLE 2				4	cycles
t_{DIS}	Output Disable Time; NOTE 3	ENABLE 1				4	cycles
		ENABLE 2				4	cycles

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.
Terminated at 50Ω to $V_{DDO}/2$.
NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6D. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		DC		100	MHz
odc	Output Duty Cycle			48		52	%
*t*sk(o)	Output Skew; NOTE 2, 4					80	ps
*t*jit(Ø)	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.14		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		800	ps
t_{EN}	Output Enable Time; NOTE 3	ENABLE 1				4	cycles
		ENABLE 2				4	cycles
t_{DIS}	Output Disable Time; NOTE 3	ENABLE 1				4	cycles
		ENABLE 2				4	cycles

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.
Terminated at 50Ω to $V_{DDO}/2$.
NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6E. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDO} = 1.8V±0.2V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		DC		100	MHz
odc	Output Duty Cycle			48		52	%
*t*sk(o)	Output Skew; NOTE 2, 4					80	ps
*t*jit(Ø)	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.18		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		900	ps
t_{EN}	Output Enable Time; NOTE 3	ENABLE 1				4	cycles
		ENABLE 2				4	cycles
t_{DIS}	Output Disable Time; NOTE 3	ENABLE 1				4	cycles
		ENABLE 2				4	cycles

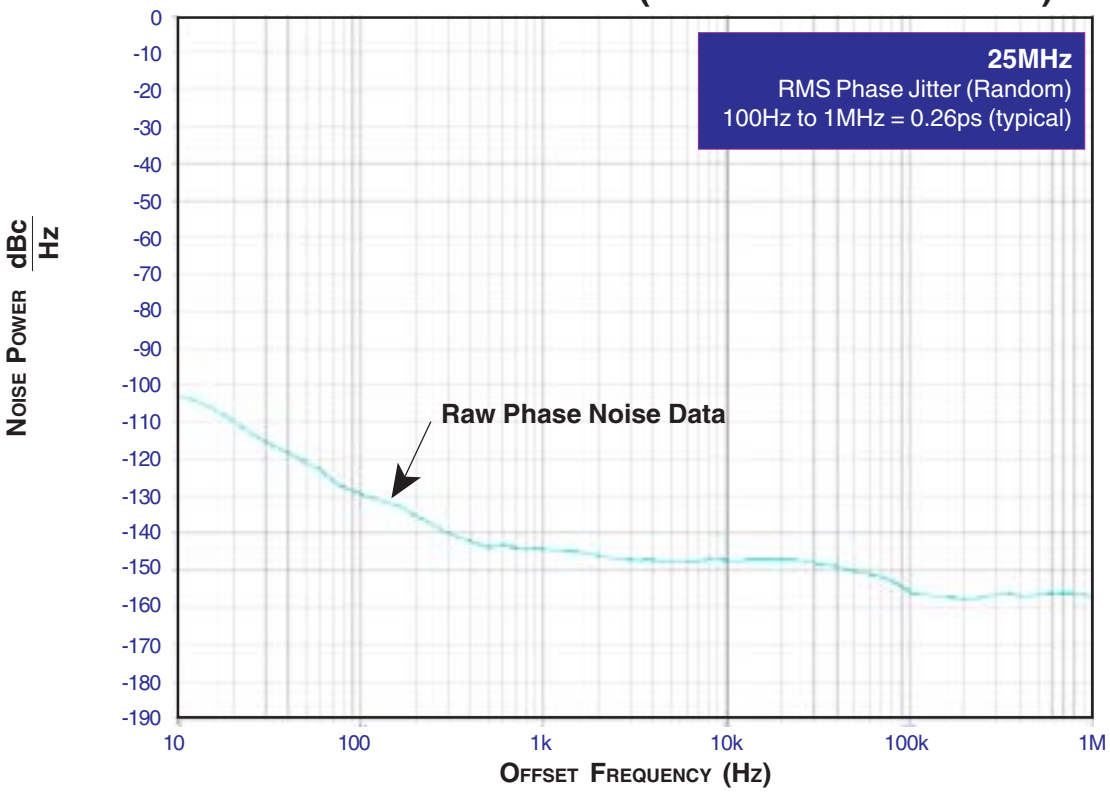
All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.
Terminated at 50Ω to $V_{DDO}/2$.
NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 6F. AC CHARACTERISTICS, V_{DD} = 2.5V±5%, V_{DDO} = 1.8V±0.2V, T_A = -40°C TO 85°C

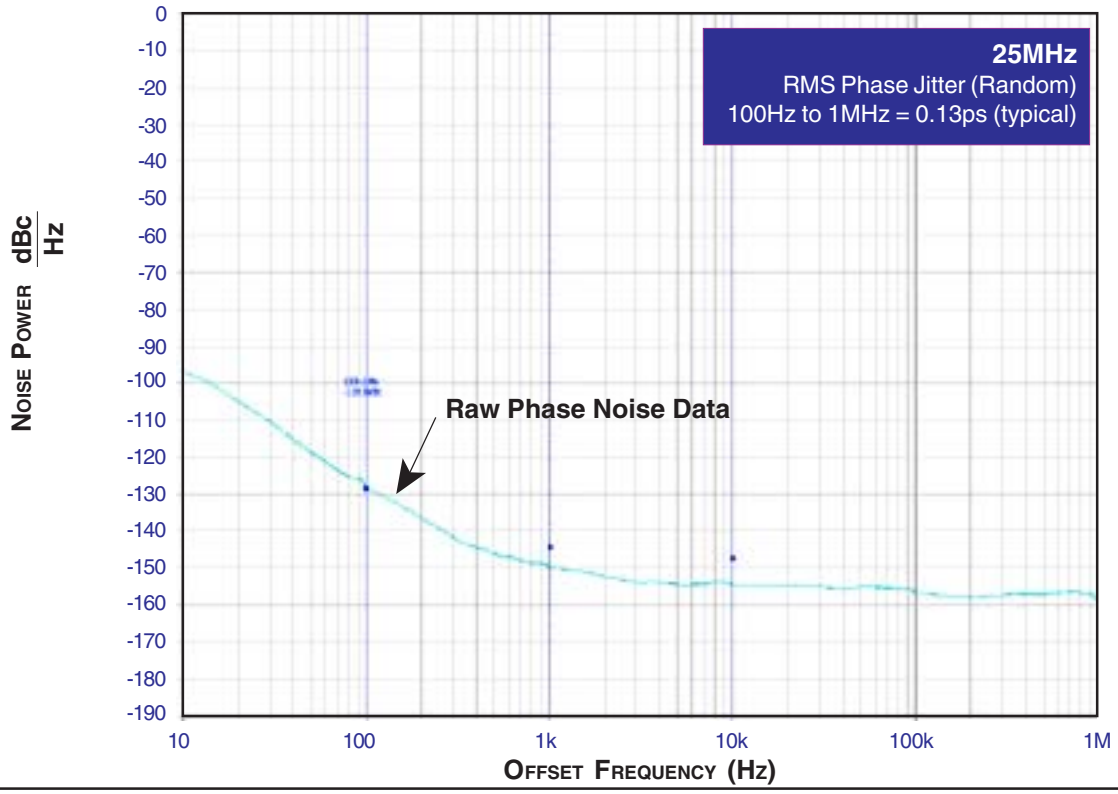
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		DC		100	MHz
odc	Output Duty Cycle			47		53	%
*t*sk(o)	Output Skew; NOTE 2, 4					80	ps
*t*jit(Ø)	RMS Phase Jitter (Random)		25MHz @ (Integration Range: 100Hz-1MHz)		0.19		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	200		900	ps
t_{EN}	Output Enable Time; NOTE 3	ENABLE 1				4	cycles
		ENABLE 2				4	cycles
t_{DIS}	Output Disable Time; NOTE 3	ENABLE 1				4	cycles
		ENABLE 2				4	cycles

All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.
Terminated at 50Ω to $V_{DDO}/2$.
NOTE 1: XTAL_IN can be overdriven relative to a signal a crystal would provide.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: These parameters are guaranteed by characterization. Not tested in production.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

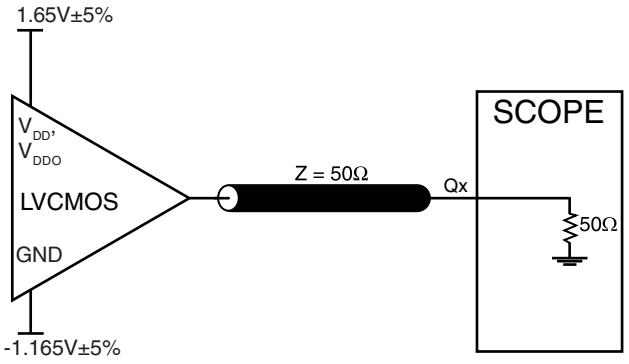
TYPICAL PHASE NOISE AT 25MHZ (2.5V CORE/ 2.5V OUTPUT)



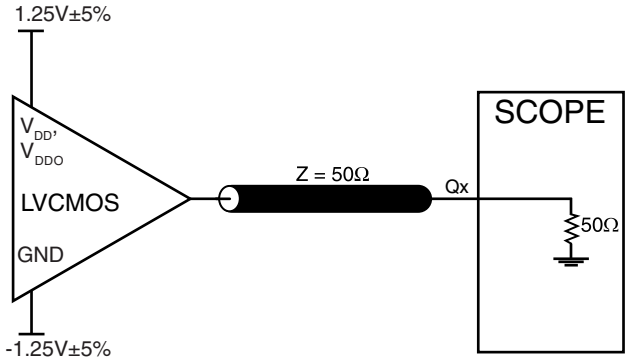
TYPICAL PHASE NOISE AT 25MHZ (3.3V CORE/ 3.3V OUTPUT)



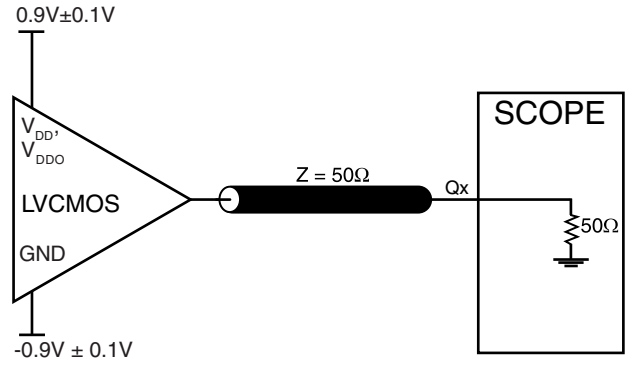
PARAMETER MEASUREMENT INFORMATION



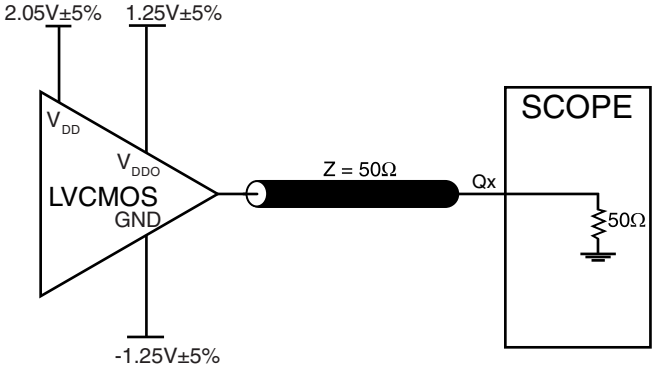
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



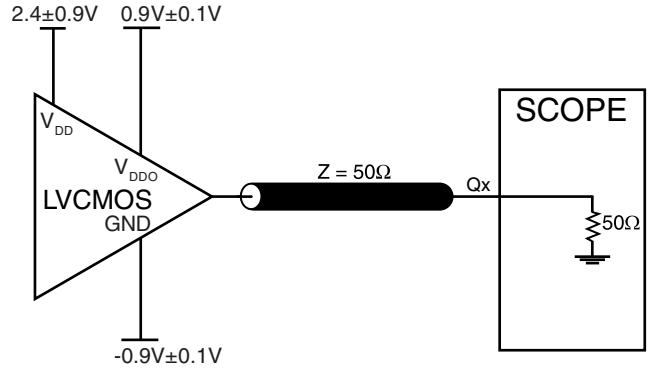
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



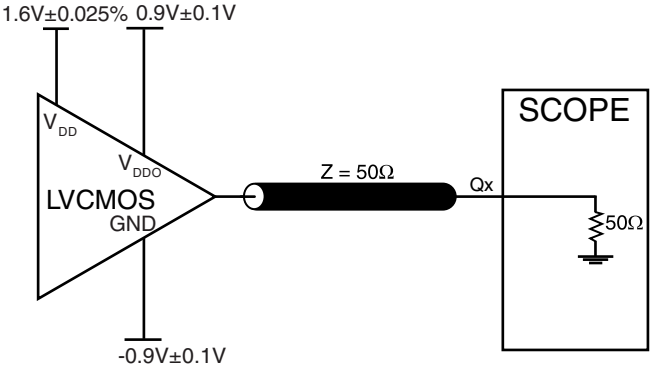
1.8V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



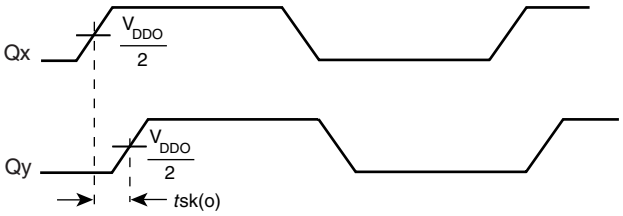
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



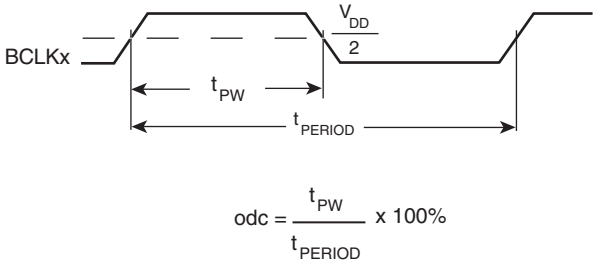
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



2.5 CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT

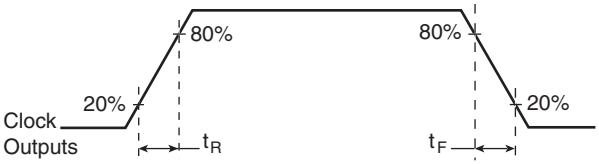


OUTPUT SKEW



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE

Figure 1A shows an example of ICS83905I crystal interface with a parallel resonant crystal. The frequency accuracy can be fine tuned by adjusting the C1 and C2 values. For a parallel crystal with loading capacitance CL = 18pF, we suggest C1 = 15pF and C2 = 15pF to start with. These values may be slightly fine tuned further to optimize the frequency accuracy for different board layouts. Slightly increasing the C1 and C2 values will slightly reduce the frequency. Slightly decreasing the C1 and C2 values will slightly increase the frequency. For the oscillator circuit below, R1 can be used, but is not required. For new designs, it is recommended that R1 not be used.

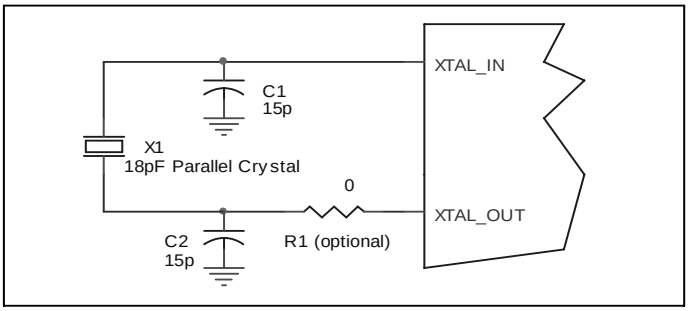


FIGURE 1. CRYSTAL OSCILLATOR INTERFACE

LAYOUT GUIDELINE

Figure 2 shows an example of ICS83905I application schematic. In this example, the device is operated at V_{DD} = 3.3V and V_{DDO} = 3.3V. The decoupling capacitors should be located as close as possible to the power pins. The input is driven by an 18pF load resonant quartz crystal. The tuning capacitors (C1, C2) are fairly accurate, but minor adjustments might be required. For the LVCMOS output drivers, two termination examples are shown in the schematic. For additional termination, examples are shown in the LVCMOS Termination Application Note.

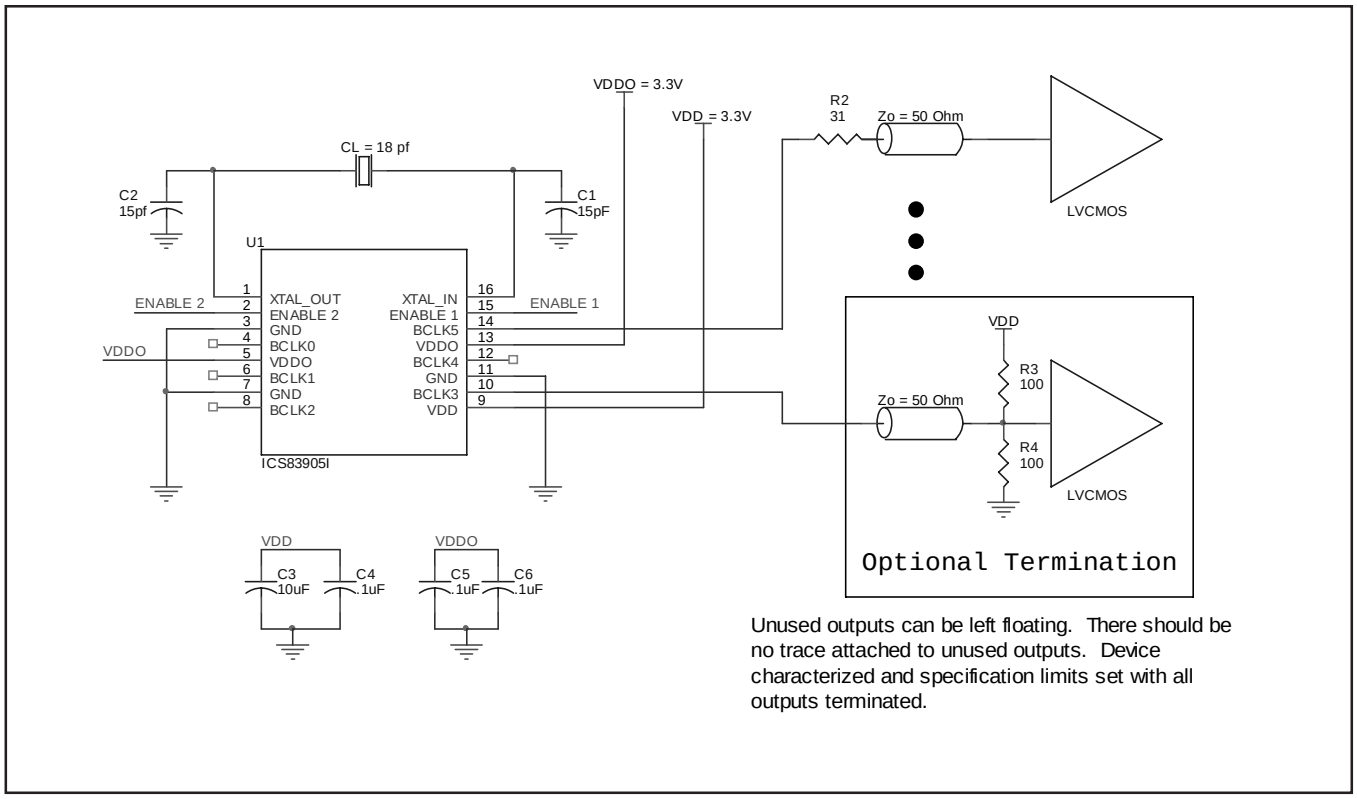


FIGURE 2. SCHEMATIC OF RECOMMENDED LAYOUT

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT
The transistor count for ICS83905I is: 339

Pin compatible to MPC905

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

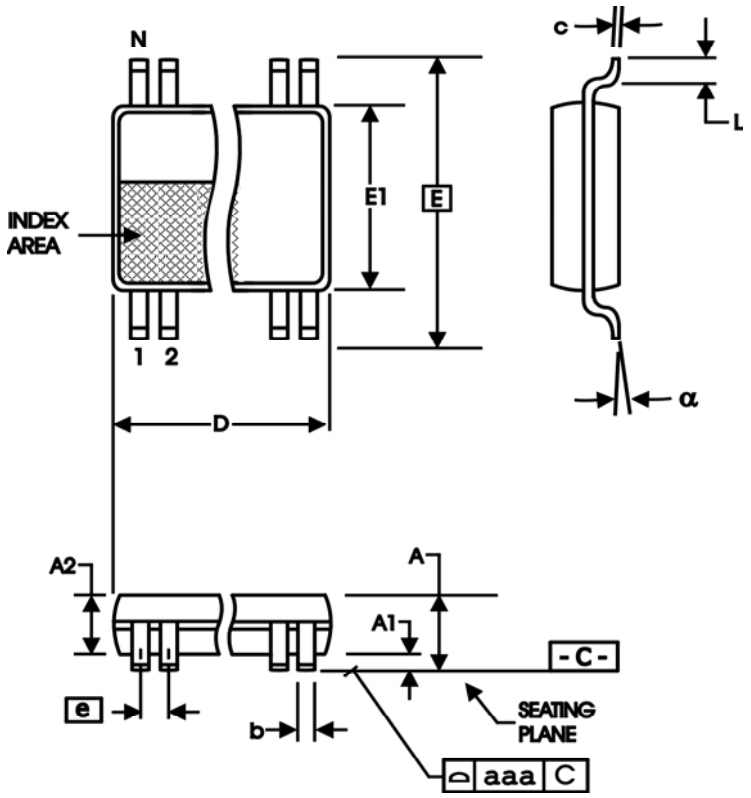


TABLE 8. PACKAGE DIMENSIONS FOR TSSOP

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS83905AGI	TBD	16 Lead TSSOP	tube	-40°C to 85°C
ICS83905AGIT	TBD	16 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS83905AGILF	83905AIL	16 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS83905AGILFT	83905AIL	16 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		2	Added Enable Timing Diagram.	3/28/05
B	6A - 6F	1 5 - 7 8	Features Section - added RMS Phase Jitter bullet. AC Characteristics Tables - added RMS Phase Jitter spec. Corrected ambient operating temperature. Added Phase Noise Plot.	4/8/05
B		11 12	Added Crystal Input Interface in Application Section. Added schematic layout.	5/16/05