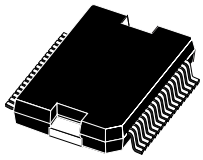
L9362

QUAD LOW SIDE DRIVER

- QUAD LOW-SIDE DRIVER FOR AUTOMOTIVE APPLICATION
- CURRENT FEEDBACK OUTPUT FOR EACH POWER STAGE
- 5V SUPPLY VOLTAGE
- INTERNAL FAILURE DIAGNOSTIC
- OUTPUT VOLTAGE SLOPE CONTROL FOR LOW ELECTRO MAGNETIC EMISSIONS
- INTERNAL SHORT CIRCUIT PROTECTION
- OVERTEMPERATURE PROTECTION AND OVERCURRENT PROTECTION AND DISABLE
- SWITCHING FREQUENCY UP TO 2kHZ
- INTERNAL ZENER CLAMP OF THE OUTPUT VOLTAGE FOR INDUCTIVE LOADS
- PARALLEL INPUT
- SPI FOR DIAGNOSTIC INFORMATION EXCHANGE
- RESET INPUT



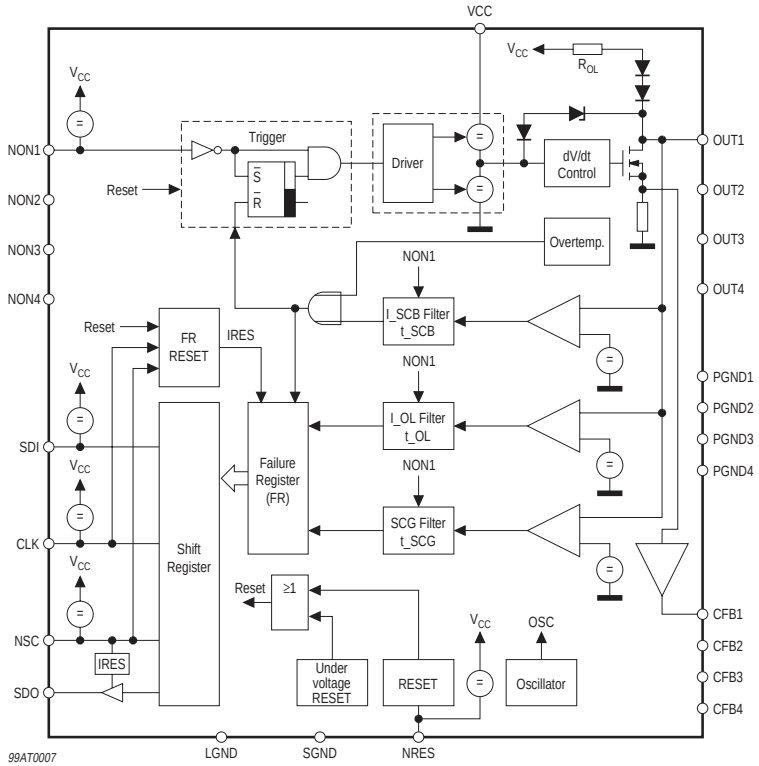
PowerSO36
ORDERING NUMBER: L9362

- TYPICAL INTERNAL OSCILLATOR FREQUENCY 325kHZ

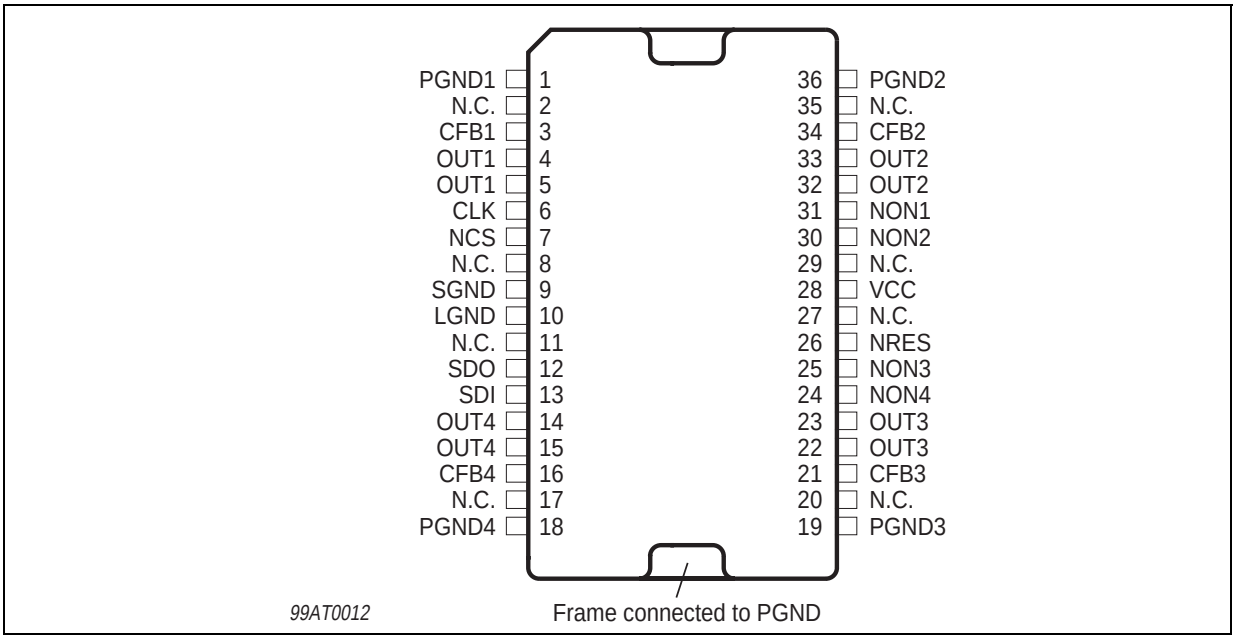
DESCRIPTION

The Quad Driver is an integrated quad low-side power switch with power limitation, load interrupt and shorted load detection, thermal shutdown, error detection via SPI interface and integrated Z-diodes for output clamping, free running diodes.

BLOCK DIAGRAM



PIN CONNECTION



PIN FUNCTIONS

Pin No.	Pin Name	Pin Description	Notes
1	PGND1	Power Ground	
2	N.C.		
3	CFB1	Output Current feedback	Sinks current proportional to I_{OUT1}
4	OUT1	Output Power Switch	
5	OUT1	Output Power Switch	
6	CLK	Input Clock	Digital input, Schmitt trigger, internal Pullup current
7	NCS	inverted Chip Select Input	Digital input, Schmitt trigger, internal Pullup current
8	N.C.		
9	SGND	Signal Ground	
10	LGND	Ground of digital part	
11	N.C.		
12	SDO	Serial Data Output	Digital tristate output
13	SDI	Serial Data Input	Digital input, Schmitt trigger, internal Pullup current
14	OUT4	Output Power Switch	
15	OUT4	Output Power Switch	
16	CFB4	Output Current feedback	Sinks current proportional to I_{OUT4}
17	N.C.		
18	PGND4	Power Ground	
19	PGND3	Power Ground	
20	N.C.		
21	CFB3	Output Current feedback	Sinks current proportional to I_{OUT3}
22	OUT3	Output Power Switch	
23	OUT3	Output Power Switch	
24	NON4	Inverted Control Signal Input	Digital input, Schmitt trigger, internal Pullup current

PIN FUNCTIONS (continued)

Pin No.	Pin Name	Pin Description	Notes
25	NON3	Inverted Control Signal Input	Digital input, Schmitt trigger, internal Pullup current
26	NRES	Inverted Reset Input	Digital input, Schmitt trigger, internal Pullup current
27	N.C.		
28	VCC	5V Supply Voltage Input	
29	N.C.		
30	NON2	Inverted Control Signal Input	Digital input, Schmitt trigger, internal Pullup current
31	NON1	Inverted Control Signal Input	Digital input, Schmitt trigger, internal Pullup current
32	OUT2	Output Power Switch	
33	OUT2	Output Power Switch	
34	CFB2	Output Current feedback	Sinks current proportional to I_{OUT2}
35	N.C.		
36	PGND2	Power Ground	

THERMAL DATA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Thermal resistance						
$R_{th\ j\text{-}case}$	Thermal resistance junction to case (one powerstage in use)	Die must be soldered on the frame.			4.5	°C/W
R_{thja}	Thermal resistance junction-ambient	pad layout		50		°C/W
R_{thja}	Thermal resistance junction-ambient	pad layout + 6 cm^2 on board heat sink		35		°C/W
ESD						
ESD	MIL 883C				±2	KV

ABSOLUTE MAXIMUM RATINGS

For externally applied voltages or currents exceeding these limits damage of the circuit may occur

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltages						
V_{CC}	Supply voltage		-0.3		7	V
Outputs (Out 1 ... 4)						
V_{Out}	Continues output voltage	With no reverse current.	-0.3		45	V
I_{outc}	Continues current				3.0	A
$I_{SCBpeak}$	Peak output current		-10		I_SCB	A
W_{OFF}	Clamped energy at the switching OFF	For 2ms, see fig. 8			50	mJ
Inputs (NONx; NCS; CLK; NRES; SDI)						
V_{IN}	Input voltage		-0.3		7	V
Outputs (SDO; CFB)						
V_{OUT}	Output voltage		-0.3		V_{CC} +0.3	V
Operating junction temperature						
T_j	Operating junction temperature		-40		150	°C

Note: The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

ELECTRICAL CHARACTERISTICS

4.5V ≤ V_{CC} ≤ 5.5V, -40°C ≤ T_J ≤ 125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply current						
I_{CCRES}	Standby current	Without load. T_j ≤ 85°C NRES = LOW			1.3	mA
I_{CCOPM}	Operating mode	$I_{OUT\ 1\ ...\ 4}$ = 2A		11	17	mA
I_{CCLV}	Low voltage supply current	V_{CC} < 0,5V			80	µA
Inputs (NONx; NCS; CLK; NRES; SDI)						
V_{INL}	Low threshold		-0.3		0.2 • V_{CC}	V
V_{INH}	High threshold		0.7 • V_{CC}		V_{CC} +0.3	V
V_{hyst}	Hysteresis		0.85			V
I_{IN}	Input leakage current	V_{IN} = V_{CC}			10	µA
I_{IN}	Input current (NONx, NCS, CLK, SDI)	V_{IN} ≤ 0.8•V_{CC}	20		100	µA
$I_{IN\ NRES}$	Input current NRES		3		20	µA
Serial Data Output						
V_{SDOH}	High output level	(I_{SDO} = -2mA)	V_{CC} - 0.4			V
V_{SDOL}	Low output level	(I_{SDO} = 3.2mA)			0.4	V
I_{SDOL}	Tristate leakage current	(NCS = HIGH; V_{SDO} = 0V ... V_{CC})	-10		10	µA
Outputs (Out 1 ... 4)						
I_{OUTL1}	Leakage current 1	(NON = HIGH; V_{OUT} = 14V; V_{CC} = 5V)			10	µA
V_{clpa}	Output clamp voltage	V_{clpa} (I_{OUT} = 0.5A)	45	50	60	V
W_{OFF}	Clamped energy at the switching OFF [1]	For 2ms, see fig. 8			50	mJ
R_{DSON}	ON resistance	I_{OUT} = 2A; T_j = 150°C; T_j = 25°C [2]		250	500 300	mΩ mΩ
OVR_{p1} OVR_{p2}	Positive output voltage ramp (with inductive load)	V_{OUT} = 30% ... 80% of V_{BAT}=16V 3) V_{OUT} = V_{BAT} ... 0.9 • V_{clp} [3]	0.3 0.75	0.9	1.35 2.25	V/µs V/µs
OVR_n	Negative output voltage ramp	80% ... 30% of V_{BAT} = 16V with inductive load [3]	0.3	0.9	1.35	V/µs
t_{dON}	Turn ON delay	NON = 50%; V_{OUT} = 0.8 • V_{BAT}	0	4	10	µs
t_{dOFF}	Turn OFF delay	NON = 50%; V_{OUT} = 0.3 • V_{BAT}	0	4	10	µs

Note 1: Typical loads for the zener clamping and the output voltage ramps are:
a) 10Ω, 16mH at all outputs or
b) 25Ω, 160mH

Note 2: At 150°C guaranteed by design and electrical characterisation

Note 3: Tested with resistive load of R_{load} = 50Ω

ELECTRICAL CHARACTERISTICS (continued)
4.5V ≤ V_{CC} ≤ 5.5V, -40°C ≤ T_J ≤ 125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Powerstage protection						
I_{SCB}	Short current detection and switch off threshold	With filter-time t_SCB.	3.0		5.0	A
t_SCB	Short circuit switch off delay time			3	30	µs
V_{ccmin}	V_{CC} undervoltage		3.0		4.0	V
Current feedback						
$T_{Ratio\ 1}$	I_{CFB} / I_{OUT} for I_{OUT}=0.4...2A [4]	V_{CFB} ≥ 1.8V	1.45	1.65	2	mA/A
T_{MPS1} [6]	[5]	Temperature stability for 0.4A to < 2.0A, related to 25°C		±3	±6	%
CURS1	for I_{OUT} = 0.4A to 2A [5]	Current stability Δgain/Gain at 2A				
		T_J = -40°C	-12		17	%
		T_J = +25°C	-6		10	%
		T_J = +125°C	-5		5	%
CURlin1 [6] CURlin2	for I_{OUT} = 0.4A to 1.0A [4] for I_{OUT} = 1.0A to 2.0A [4]	Linearity Error (within the calibration points at 0.5A, 1A, 2A)		±0.2	±1 ±0.7	% %

Note 4: At 150°C guaranteed by design and electrical characterisation
Note 5: Guaranteed by design and electrical characterisation
Note 6: Values for T_{MPS1}, CURlin1 and CURlin2 are typical values from testing results

Diagnostic						
V_{REF1}	Short to GND threshold voltage	for I_{OUT} ≤ 2A	0.390 •V_{CC}		0.435 •V_{CC}	V
t_SCG	Short to GND filter time		140		250	µs
I_{OL}	Open load threshold current		10		55	mA
t_OL	Open load filter time		140		265	µs
R_{OL}	Pullup resistor at OUT1, OUT2, OUT3 and OUT4 for OL detection		2.0		8.0	kΩ
T_{OFF}	Temperature detection threshold [7]		155	170	190	°C

Note 7: Guaranteed by measurement and correlation

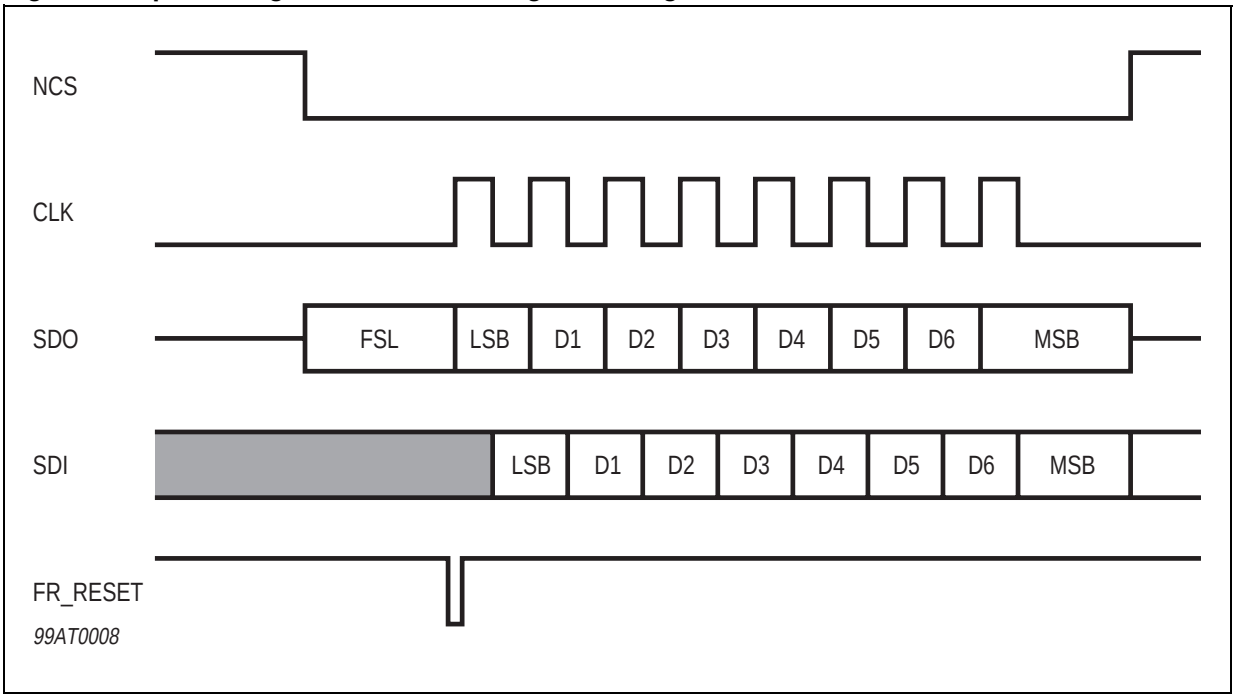
ELECTRICAL CHARACTERISTICS (continued)
4.5V ≤ V_{CC} ≤ 5.5V, -40°C ≤ T_J ≤ 125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Serial diagnostic link (external Load capacitor at SDO = 100pF)						
f_{clk}	Clock frequency	50% duty cycle.	0		3	MHz
t_{clh}	Minimum time CLK = HIGH		100			ns
t_{cll}	Minimum time CLK = LOW		100			ns
t_{pcld}	Propagation delay	CLK to data at SDO valid.			100	ns
t_{csdv}	NCS = LOW	To data at SDO valid.			100	ns
t_{sclch}	CLK low before NCS low	Setup time CLK to NCS change H/L.	100			ns
t_{hclcl}	CLK change L/H after NCS = LOW		100			ns
t_{scld}	SDI input setup time	CLK change H/L after SDI data valid.	20			ns
t_{hcld}	SDI input hold time	SDI data hold after CLK change H/L.	20			ns
t_{sclcl}	CLK low before NCS high		150			ns
t_{hclch}	CLK high after NCS high		150			ns
t_{pchdz}	NCS L/H to output data float				100	ns
t_{fNCS}	NCS filter-time	Pulses ≤ t_{fNCS} will be ignored.	10		40	ns

Note: 8. Input Pin Capacitance of SDI, CLK, NCS, NON1, NON2, NON3, NON4 6pF typical; Output Pin Capacitance of SDO 12pF typica

1.0 Diagnostic Register and SPI timing

Figure 1. Impulse diagram to read the Diagnostic Register



Note: FR_RESET means Reset failure storage (internal signal)

Figure 2. Diagnostic Failure Register Structure

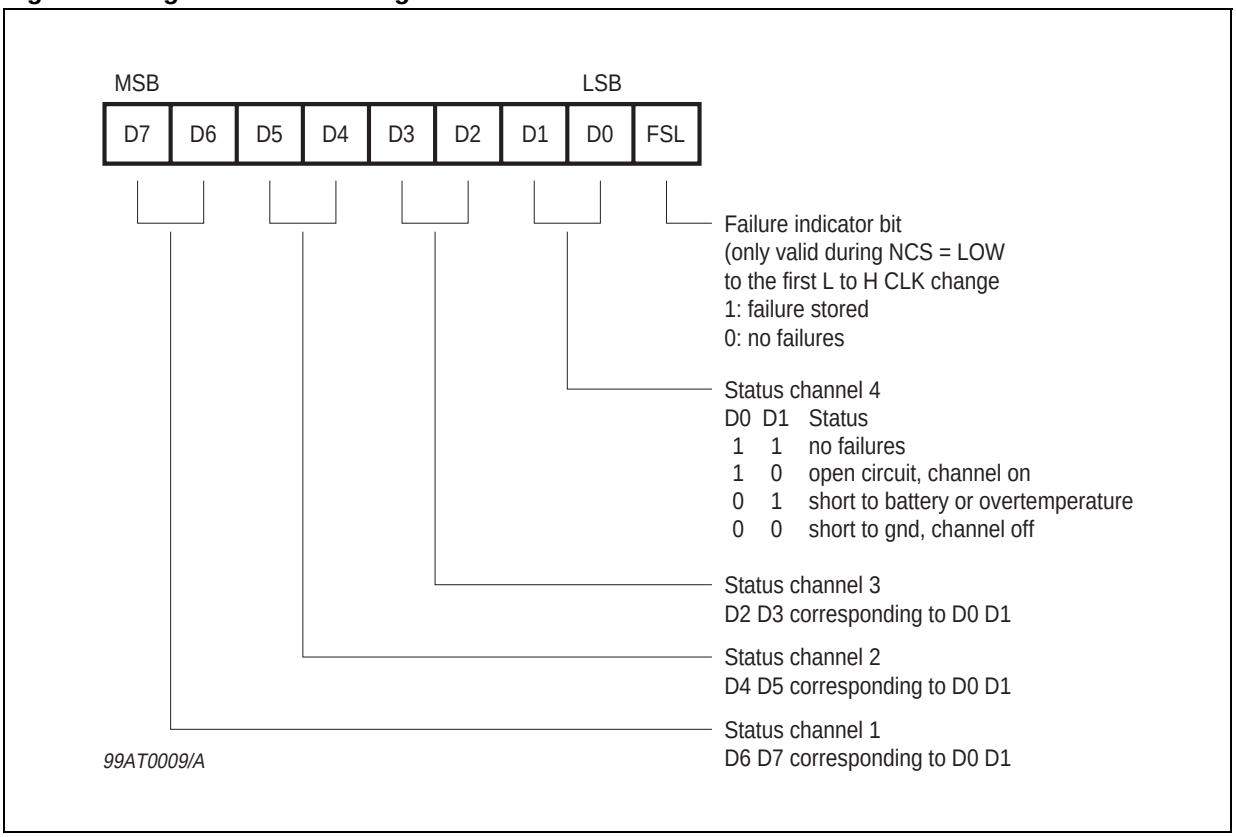


Figure 3. Timing of the Serial Interface

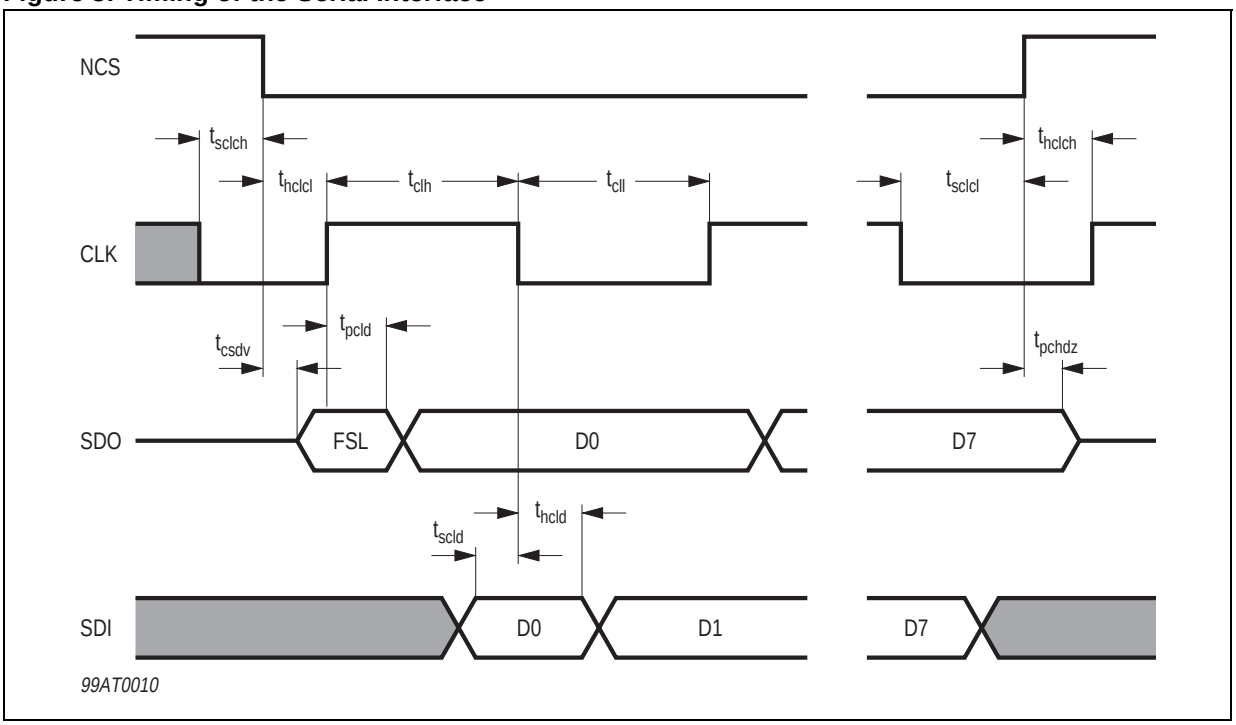


Figure 4. Short-Circuit to GND Failure (SCG-Failure) Detection

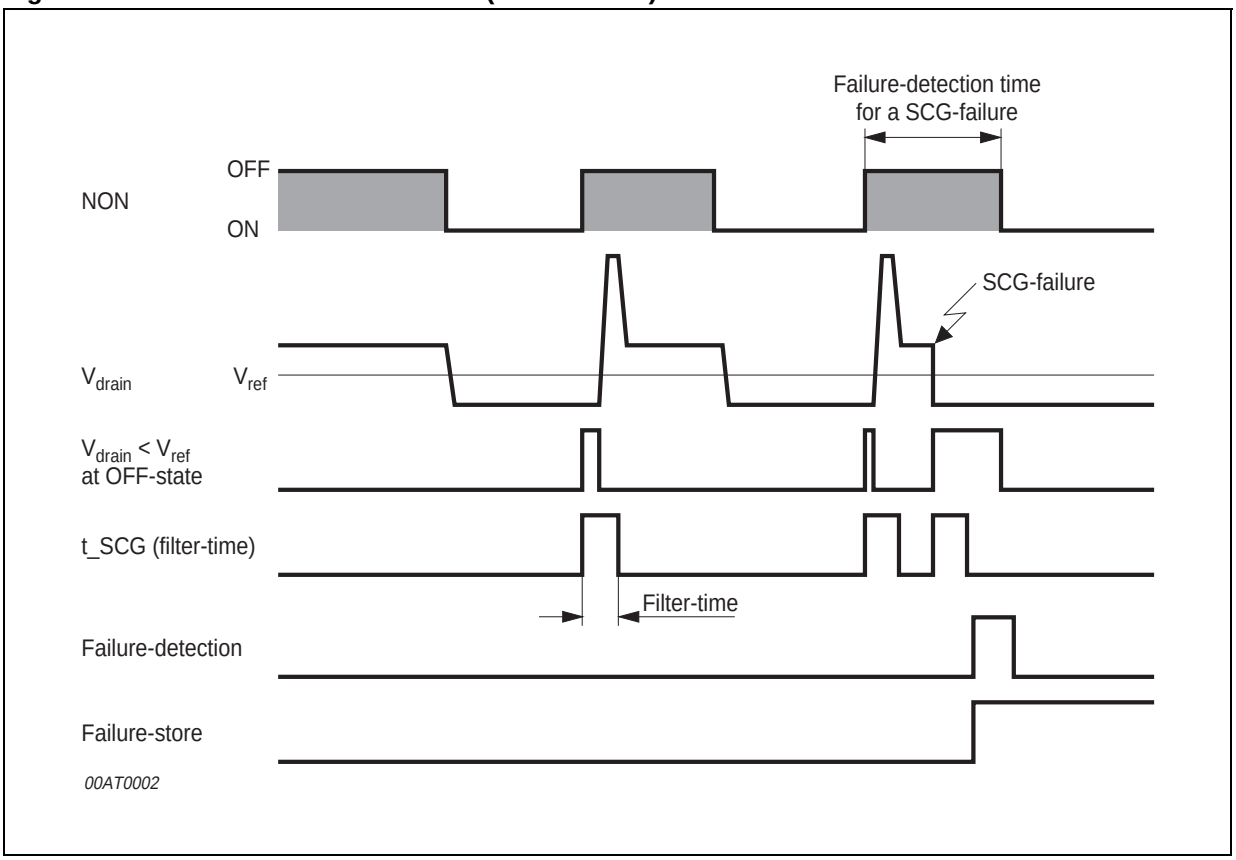


Figure 5. Open-Load Failure (OL-Failure) Detection

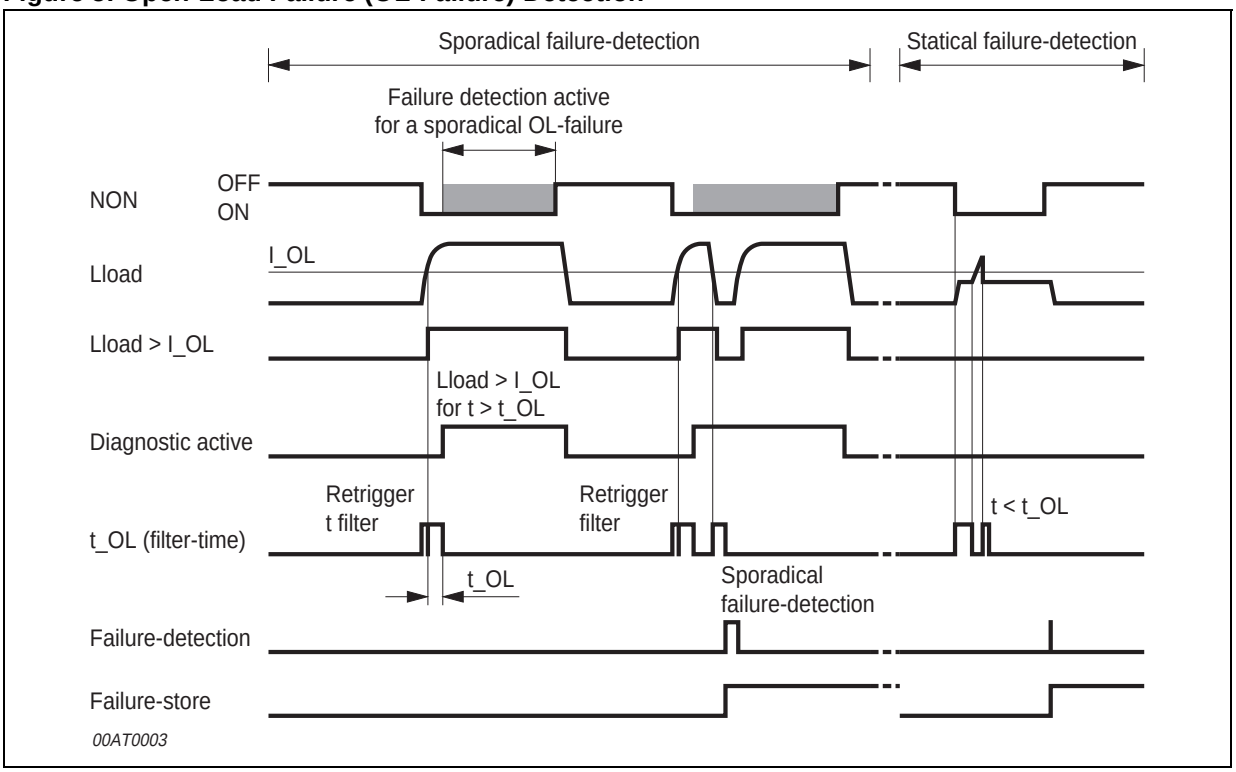


Figure 6. Different cases for an Open Load failure detection (case 1 to 10)

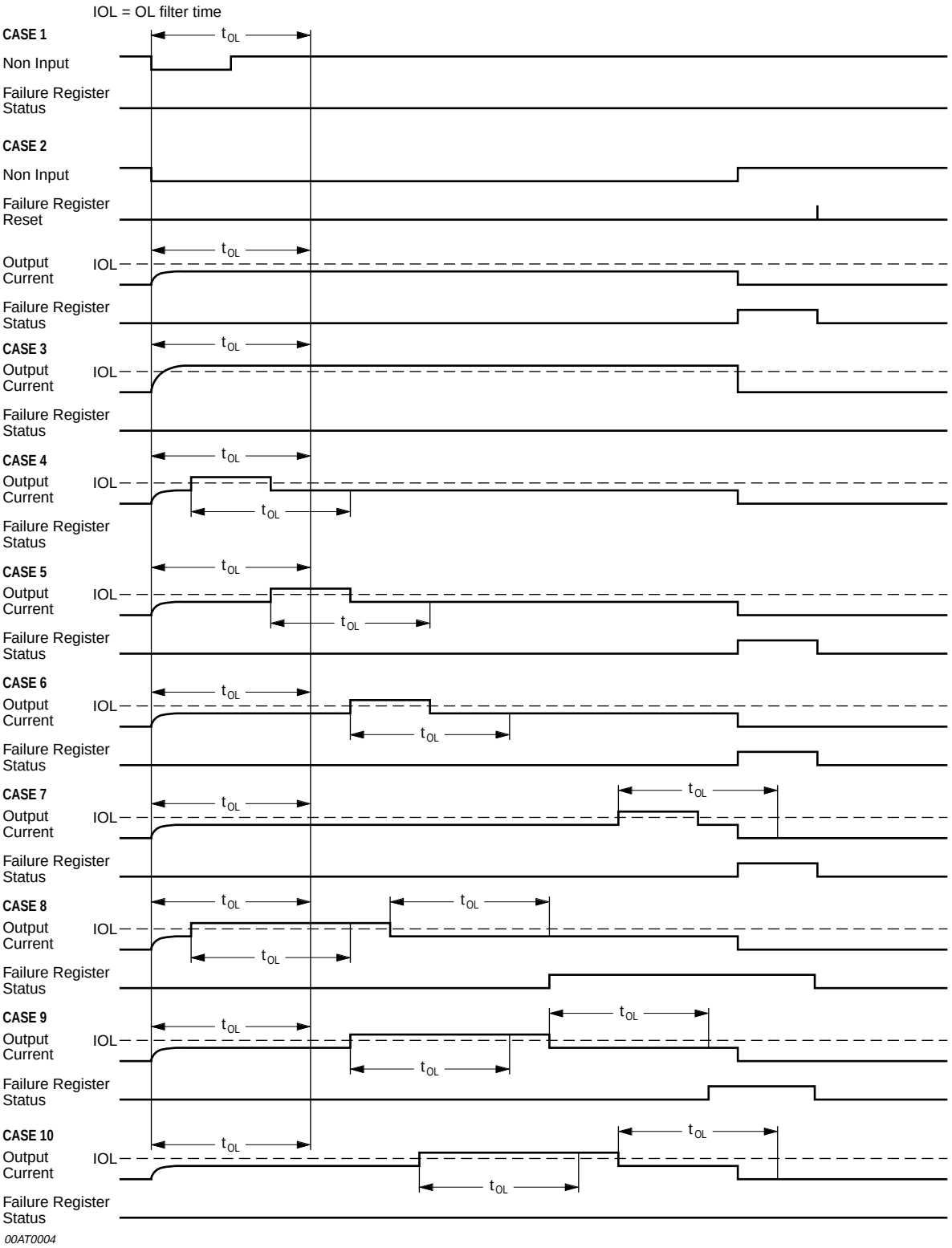


Figure 7. Different cases for an Open Load failure detection (case 11 to 20)

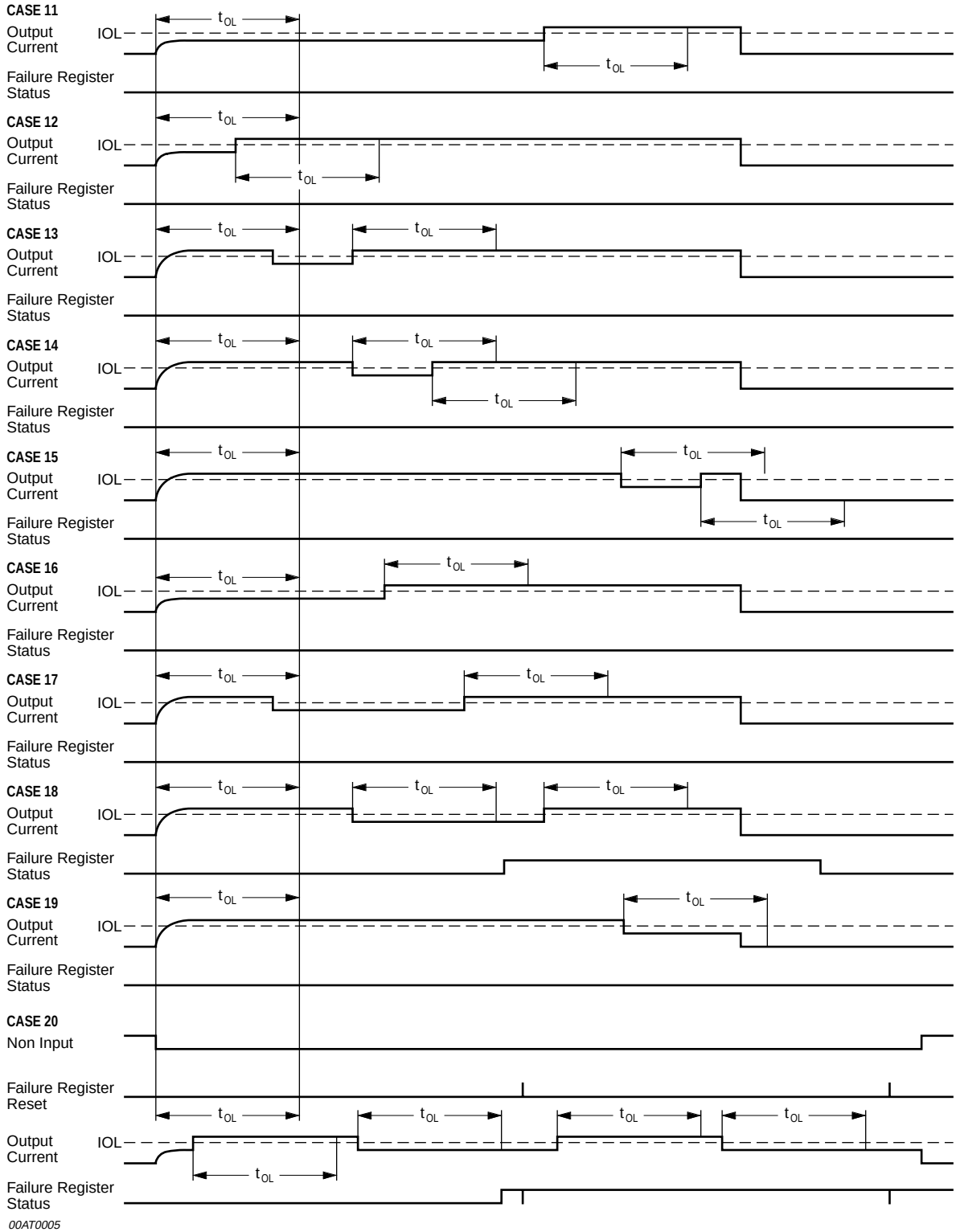


Figure 8. Max Clamp Energy Specification

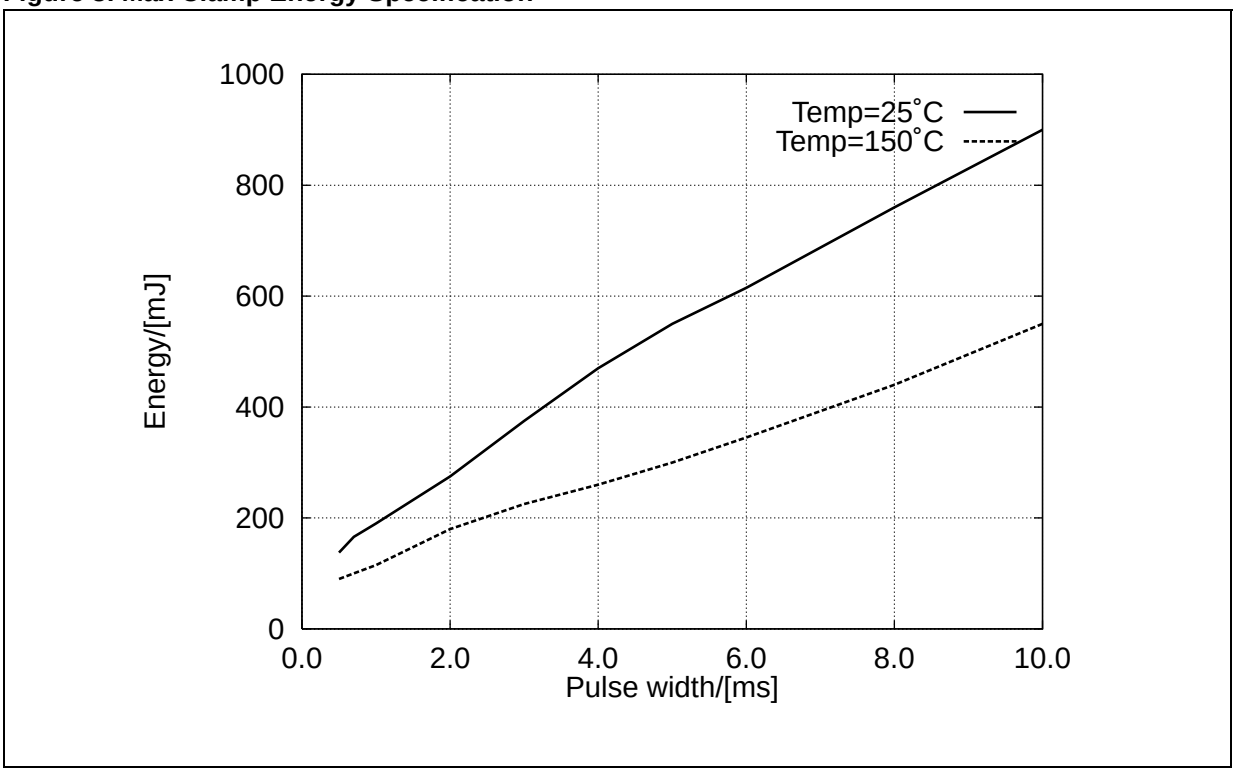


Figure 9. Tratio of Current Feedback output versus output current

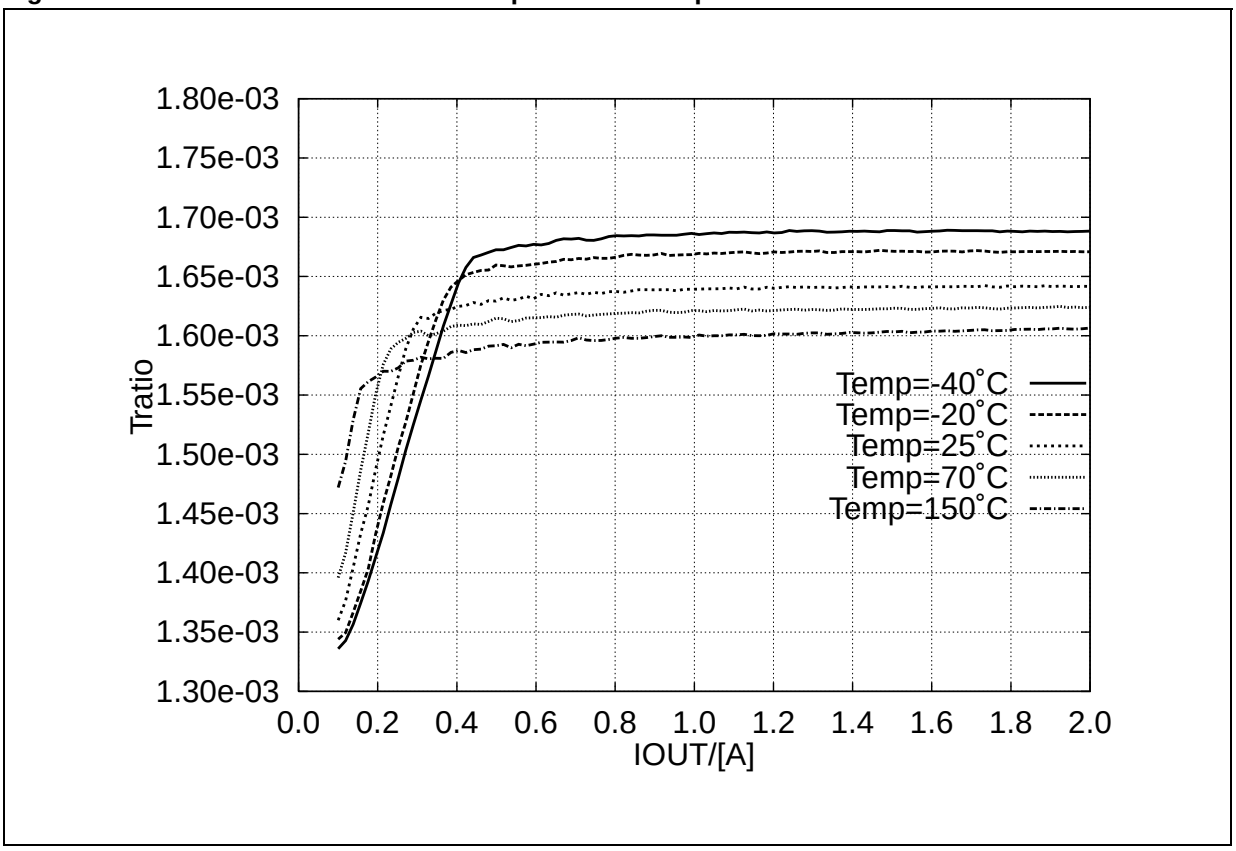
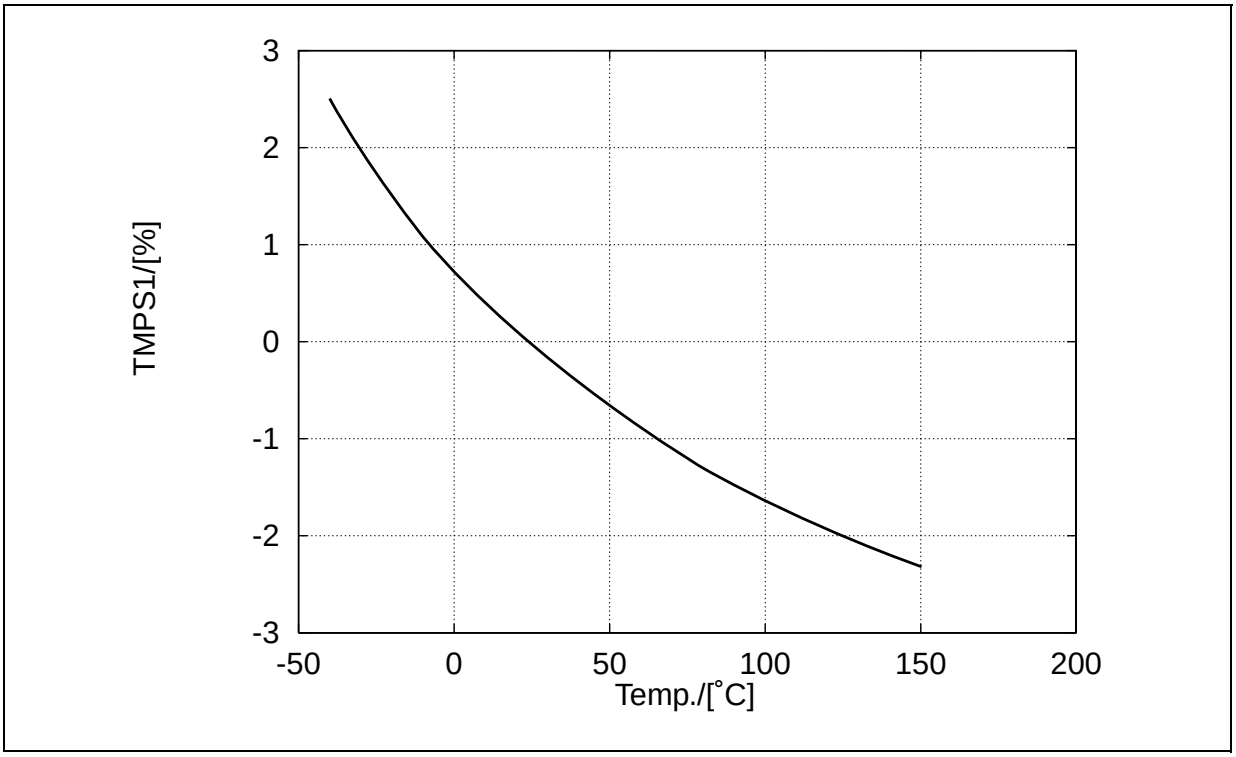


Figure 10. TMPS1 vs. Temperature ($4.5V \leq V_{cc} \leq 5.5V$; $0.5A \leq I_{out1...4} \leq 3A$)**.**



FUNCTIONAL DESCRIPTION

Introduction

The Quad Low Side Driver UF07 is built up of four identical channels (Low Side Drivers), controlled by four CMOS input stages. Each Channel is protected against short to V_{Bat} and by a zener clamp against overvoltage. A diagnostic logic recognizes four failure types at the output stage: overcurrent, short to GND, open-load and overtemperature.

The failures are stored individually for each channel in one byte which can be read out via a serial interface (SPI).

Each channel has a current feedback output which sinks a current proportional to the load current of the Low Side Switch.

Output Stage Control

Each of the four output stages is switched ON and OFF by an individual control line (NON-Input). The logic level of the control line is CMOS compatible. The output transistors are switched off when the inputs are not connected.

Power Transistors

Each of the four output stages has its own zener clamp. This causes a voltage limitation at the power transistors when inductive loads are switched off. Output voltage ramp occurring when the output is switched on or off, is within defined limits. Output transistors can be connected in parallel to increase the current capability. In this case, the associated inputs, outputs and current feedback outputs should be connected together.

Diagnostics

Following failures at the output stage are recognized:

Short circuit to V_{Bat} or overtemp.....= SCB (Highest priority)

Short circuit to GND.....=SCG

Open Load.....= OL (Lowest Priority)

Short-Circuit and Overtemperature Protection (SCB)
If the output current increases above the short current limit for a longer time than t_SCB or if the temperature increases above T_{OFF}, then the power transistor is immediately switched off. It remains switched off until the control signal at the NON-Input is switched off and on again. This filter time has the purpose to suppress wrong detection on short spikes.
All four outputs have an independent overtemperature detection and shutdown. This measurement is active while the powerstage is switched on.
The Short circuit detection and the overtemperature detection are using the same bit in the Diagnostic (one for each channel).

A **SCG** failure will be recognized, when the drain voltage of the output stage is lower as the “Short Cut to Ground threshold voltage”, while the output stage is switched off (see Fig. 4). The SCG failure is filtered with a digital filter (t_SCG) to suppress the storage of a failure at small SCG spikes, which are typical during the transition of the power output. This filter is triggered by the NON input and the (analog) SCG detection.
If the current through the output stage is lower than the IOL-reference, then an **OL** failure will be recognized after a filter time. This measurement is active while the powerstage is switched on.
The Open Load failure detection has 2 different modes, the statical failure detection and the sporadic failure detection. One main difference is, that a statical failure is transferred to the Failure register with the next rising edge of NON, whereas a sporadic failure is transferred immediately to the Failure register (see fig. 5, 6 and 7). In both failure modes the OL detection is filtered (t_OL=t_{OL}) and is using together with the SCG detection the same digital filter for suppression of spikes.
The failures are stored regarding to their priority (see above). A failure with a higher priority overwrites an eventually already detected failure with a lower priority.

Diagnostic interface
The communication between the microprocessor and the failure register runs via the SPI link. If there is a failure stored in the failure register, the first bit of the shift register is set to a high level. With the H/L change at the NCS pin the first bit of the diagnostic shift register will be transmitted to the SDO output. The SDO output is the serial output from the diagnostic shift register and it is tristate when the NCS pin is high. The CLK pin clocks the diagnostic shift register. New SDO data will appear on every rising edge of the CLK pin and new SDI data will be latched on every falling edge into the shift register. With the first positive pulse of the CLK the contents of the failure register is copied to the SPI shift register and a internal reset (FR_RESET) is generated. This internal reset clears the failure register and thus the failure register is capable of detecting failures also during the SPI read cycle. There is no bus collision at a small spike at the NCS. The CLK has to be LOW, while the NCS signal is changing.

Current feedback
Each channel has a current feedback output which sinks a current proportional to the load current of the Low Side Switch. Using this output servo loop applications can be realized by applying a PWM signal to the NON input. A typical diagram of the Current Feedback output at different temperatures is shown in figure 9.

Reset

There are two different reset functions realized:

Undervoltage reset

As long as the voltage of Vcc is lower than V_{ccmin}, the powerstages are switched off, the failure register is reset and the SDO output remains tristate.

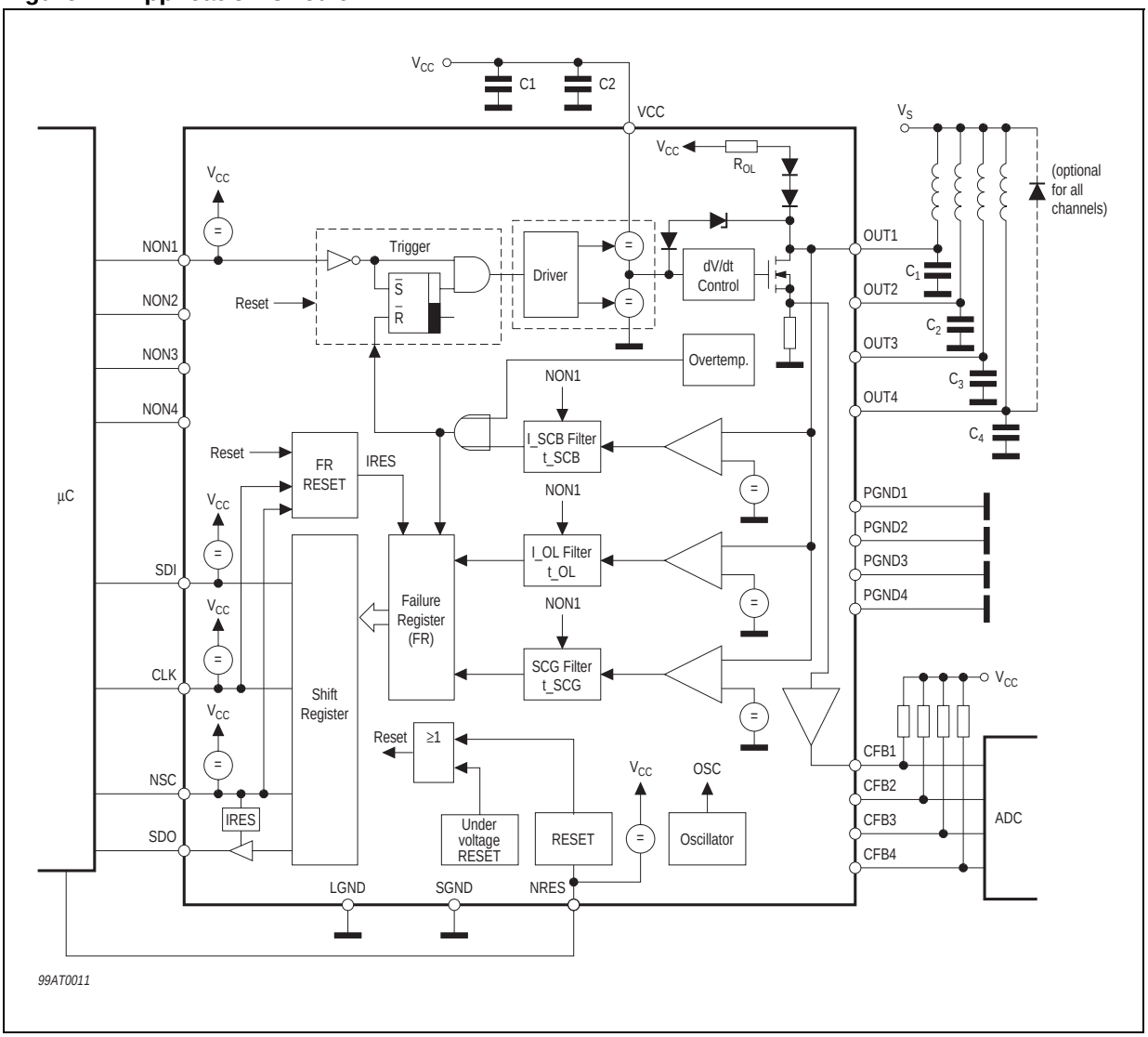
External reset

As long as the NRES pin is low following circuits are reset:
Powerstages
Failure register
and the SDO output is tristate.

Undervoltage protection

At Vcc below V_{ccmin} the device remains switched off even if there is a voltage ramp at the OUT pin.

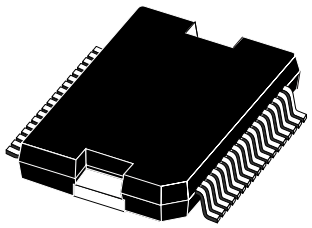
Figure 11. Application Circuit



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.141
a1	0.10		0.30	0.004		0.012
a2			3.30			0.130
a3	0		0.10	0		0.004
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D (1)	15.80		16.00	0.622		0.630
D1	9.40		9.80	0.370		0.385
E	13.90		14.50	0.547		0.570
e		0.65			0.0256	
e3		11.05			0.435	
E1 (1)	10.90		11.10	0.429		0.437
E2			2.90			0.114
E3	5.80		6.20	0.228		0.244
E4	2.90		3.20	0.114		0.126
G	0		0.10	0		0.004
H	15.50		15.90	0.610		0.626
h			1.10			0.043
L	0.80		1.10	0.031		0.043
N	10°(max.)					
S	8 °(max.)					

(1): "D" and "E1" do not include mold flash or protrusions
- Mold flash or protrusions shall not exceed 0.15mm (0.006 inch)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO36