

PM5363

TUPP+622

SONET/SDH TRIBUTARY UNIT PAYLOAD PROCESSOR FOR 622 MBIT/S INTERFACES

DATA SHEET ERRATA

ISSUE 4: JULY 2000

REVISION HISTORY

Issue No.	Issue Date	Details of Change
4	Jul 2000	Removed section on datasheet discrepancies. Removed TU3 Inband Error from the functional discrepancies. Aligns with issue 4 of the datasheet.
3	Jun 2000	Aligns with Revision B of the device. Added datasheet discrepancies 2.4-2.8: TUGEN Bit Description, TUGBYP Bit Description, Device ID Revision Number, SOS Bit Description and Boundary Scan ID Change. Removed Issue 2 functional discrepancies 3.1-3.3: Device May Corrupt Data After Reset, Device May Fail to Detect FIFO Over- or Underflow Condition and Device May Fail to Recover From FIFO Over-or-Underflow Condition. Added functional discrepancy 3.2: IAIS Pin Exhibiting Boundary Condition Anomalies
2	Feb 2000	Added TU3 Inband Error description. Added changes to timing and operating conditions. All Input Hold Times for SCLK (19.44MHz) are changed from 1ns to 1.5ns. All Output Max Prop Delay for HSCLK (77.76MHz) is changed from 8ns to 9ns. All Output Min Prop Delay for SCLK (19.44MHz) is changed from 2ns to 3.5ns. Operating Condition for $V_{DD3.3}$ is changed from $3.3V \pm 10\%$ to $3.3V \pm 0.3V$ and the operating condition for $V_{DD2.5}$ is changed from $2.5V \pm 10\%$ to $2.5V \pm 0.2V$.
1	Nov 1999	Document Creation.

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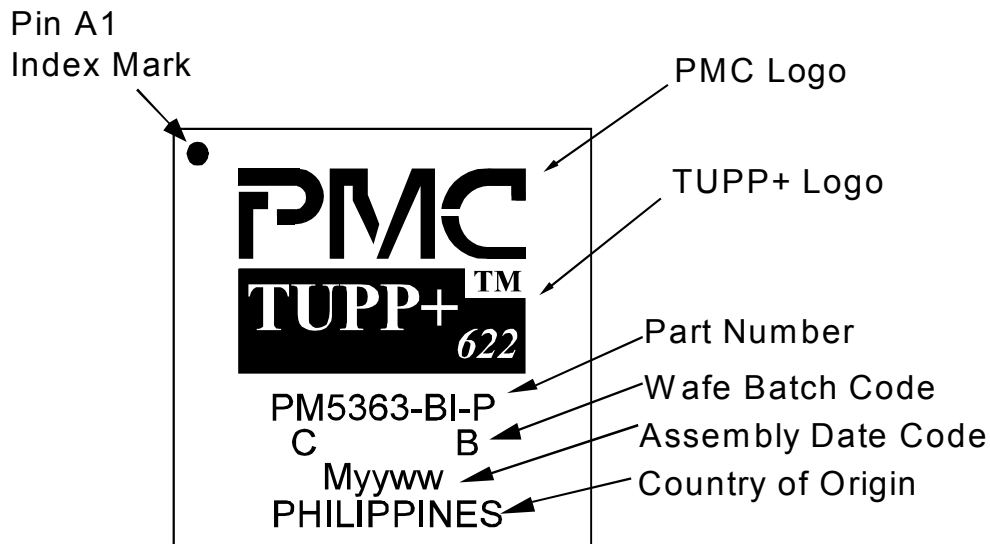
1 ISSUE 4 ERRATA

This Issue 4 Errata notifies that changes have been made to Issue 4 of the PMC-1981421 data sheet. It describes datasheet discrepancies and functional issues in Revision B of TUPP+622, and provides a summary of recommended workarounds.

The Issue 4 Datasheet and Issue 4 Errata supersede all prior editions and versions.

1.1 Device Identification

The information in this document applies only to the PM5363 TUPP+622 Revision B device. The device revision is marked at the end of the wafer batch code on the face of the device.



TOP VIEW
SCALE 1.5:1
(APPROX.)

2 FUNCTIONAL DISCREPANCIES

2.1 IAIS Pin Exhibiting Boundary Condition Anomalies

2.1.1 Description

The IAIS (IAIS[4:1]) pin is used for tributary AIS insertion when the pointer bypass mode is enabled in the VTPP block (i.e. tributary pointer interpreter is turned off). During the POH or fixed stuff column time-slot, the immediately preceding tributary remains selected. As a result, the corresponding AIS status register maybe updated erroneously if the AIS assertion via the IAIS pin does not persist over the POH or fixed stuff column.

2.1.2 Software Workaround

The software workaround is implemented by setting the IPAIS register bit associated with a particular tributary in the VTPP TSB if and when an AIS condition needs to be generated in that tributary.

2.1.3 Hardware Workaround

The hardware workaround is implemented by extending or holding the AIS assertion of tributary time-slot immediately preceding the POH or fixed stuff column until the next valid tributary time-slot. The holding period may extend across transport overhead columns of the SONET/SDH frame.

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