HN58S256AI Series

32768-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

ADE-203-669A (Z)
Rev. 1.0
May. 20, 1997

Description

The Hitachi HN58S256AI is electrically erasable and programmable ROM organized as 32768-word × 8-bit. It has realized high speed, low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 64-byte page programming function to make the write operations faster.

Features

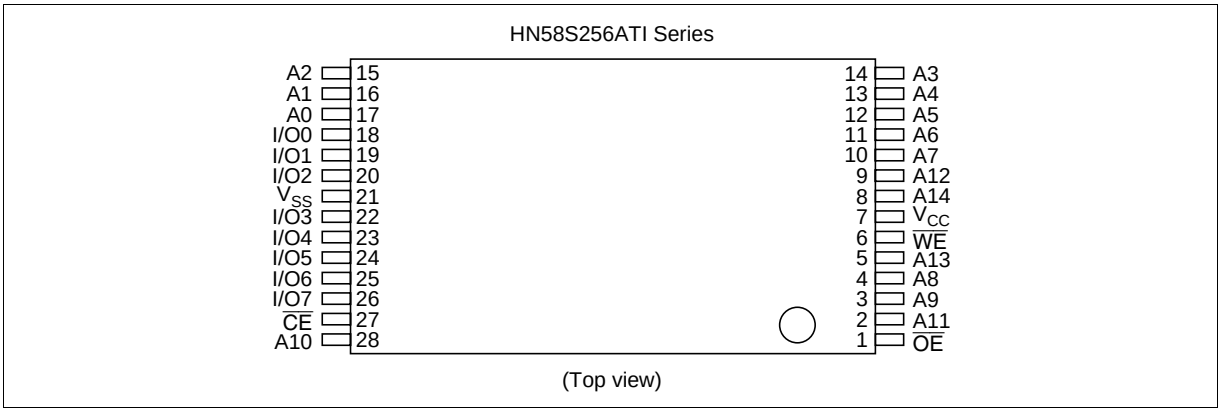
- Single 3 V supply: 2.2 to 3.6 V
- Access time: 150 ns/200 ns (max)
- Power dissipation
  - —Active: 10 mW/MHz (typ)
  - —Standby: 36 µW (max)
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 15 ms (max)
- Automatic page write (64 bytes): 15 ms (max)
- $\overline{Data}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Wide temperature range: – 40 to 85˚C

Hitachi semiconductor

Ordering Information

Type No.	Access time	Package
HN58S256ATI-15	150 ns	28-pin plastic TSOP (TFP-28DB)
HN58S256ATI-20	200 ns	

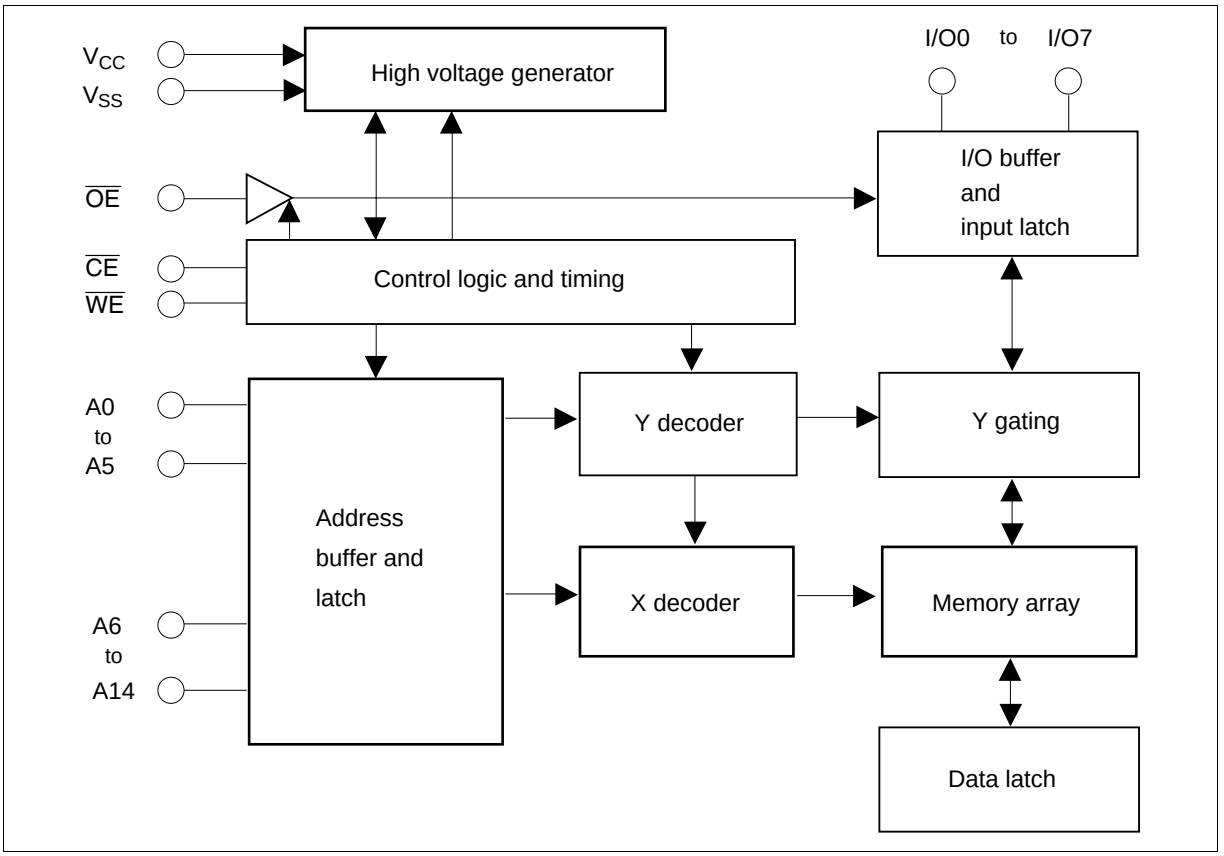
Pin Arrangement



Pin Description

Pin name	Function
A0 to A14	Address input
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Operation Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Dout
Standby	V_{IH}	×*2	×	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z
Write inhibit	×	×	V_{IH}	—
	×	V_{IL}	×	—
Data polling	V_{IL}	V_{IL}	V_{IH}	Dout (I/O7)

Notes: 1. Refer to the recommended DC operating condition.
2. ×: Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.6 to +4.6	V
Input voltage relative to V_{SS}	Vin	–0.5*[1] to +4.6*[3]	V
Operating temperature range*[2]	Topr	–40 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. Vin min = –3.0 V for pulse width ≤ 50 ns
2. Including electrical characteristics and data retention
3. Should not exceed V_{CC} + 1.0 V.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.2	3.0	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IL}	–0.3*[1]	—	0.4	V
	V_{IH}	Vcc × 0.7	—	V_{CC} + 0.3*[2]	V
Operating temperature	Topr	–40	—	85	°C

Notes: 1. V_{IL} min: –1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns.

DC Characteristics (Ta = – 40 to +85°C, V_{CC} = 2.2 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	V_{CC} = 3.6 V, Vin = 0 to 3.6 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 3.6 V, Vout = 3.6/0.4 V, $\overline{CE}$ = V_{IH}, Vin = 0 to 3.6 V
Standby V_{CC} current	I_{CC1}	—	—	10	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	500	µA	$\overline{CE}$ = V_{IH}
Operating V_{CC} current	I_{CC3}	—	—	8	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.6 V
		—	—	15	mA	Iout = 0 mA, Duty = 100%, Cycle = 150 ns at V_{CC} = 3.6 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA
Output high voltage	V_{OH}	V_{CC} × 0.8	—	—	V	I_{OH} = –100 µA

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*[1]	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*[1]	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = – 40 to +85°C, V_{CC} = 2.2 to 3.6 V)

Test Conditions

- Input pulse levels: 0.4 V to 1.9 V ($V_{CC} \leq 2.7V$), 0.4V to 2.4 V ($V_{CC} > 2.7$ V)
- Input rise and fall time: ≤ 5 ns
- Input timing reference levels: 0.8, 1.8 V
- Output load: 1TTL Gate +100 pF
- Output reference levels: 1.1 V, 1.1 V ($V_{CC} \leq 2.7V$),1.5 V, 1.5 V ($V_{CC} > 2.7$ V)

Read Cycle

		HN58S256AI					
		-15		-20			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	150	—	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	150	—	200	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	80	10	100	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	100	0	100	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

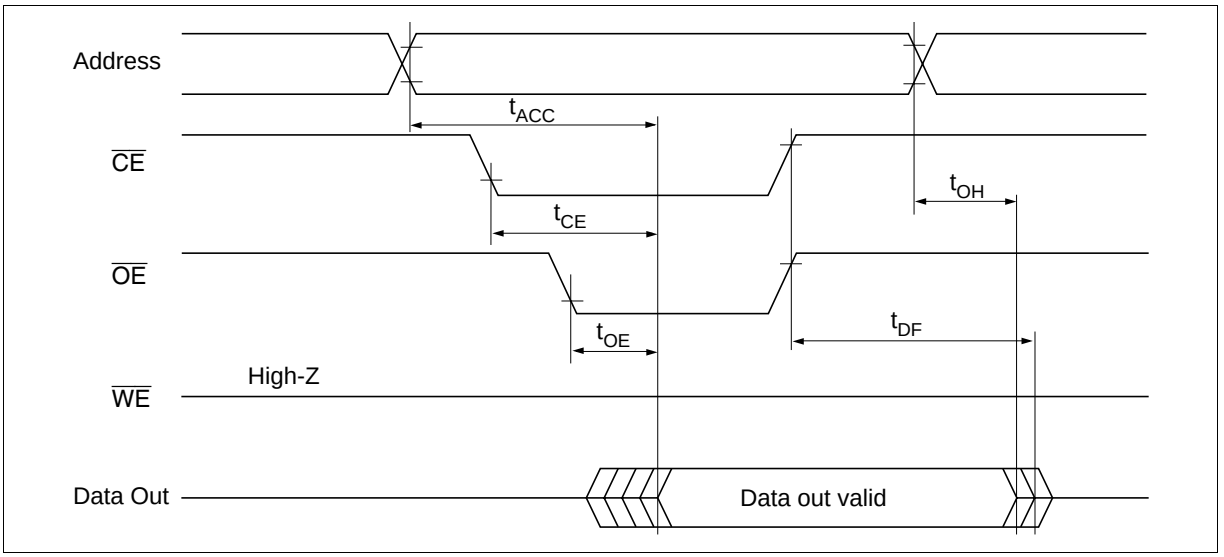
Write Cycle

Parameter	Symbol	Min*[2]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	150	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	200	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	200	—	—	ns	
Byte load cycle	t_{BLC}	0.4	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	15*[3]	ms	
Write start time	t_{DW}	0*[4]	—	—	ns	

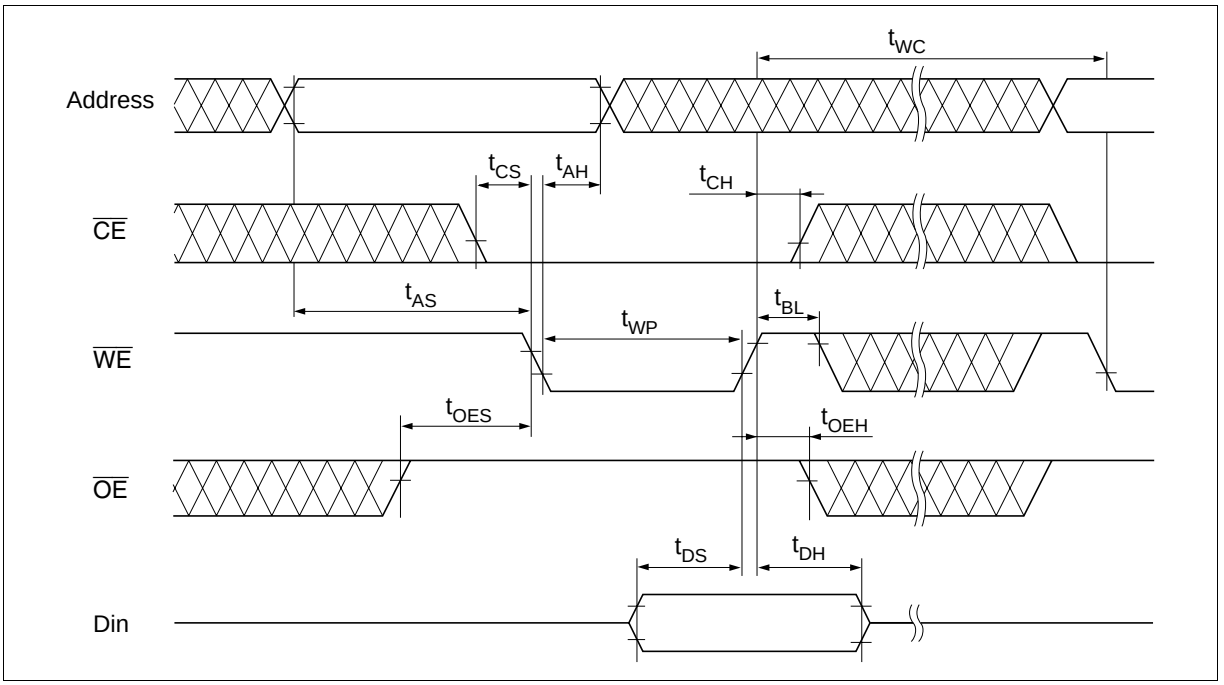
Notes: 1. t_{DF} is defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

2. Use this device in longer cycle than this value.
3. t_{WC} must be longer than this value unless polling techniques is used. This device automatically completes the internal write operation within this value.
4. Next read or write operation can be initiated after t_{DW} if polling techniques is used.
5. A16 through A14 are page addresses and these addresses are latched at the first falling edge of $\overline{WE}$.
6. A16 through A14 are page addresses and these addresses are latched at the first falling edge of $\overline{CE}$.
7. See AC read characteristics.

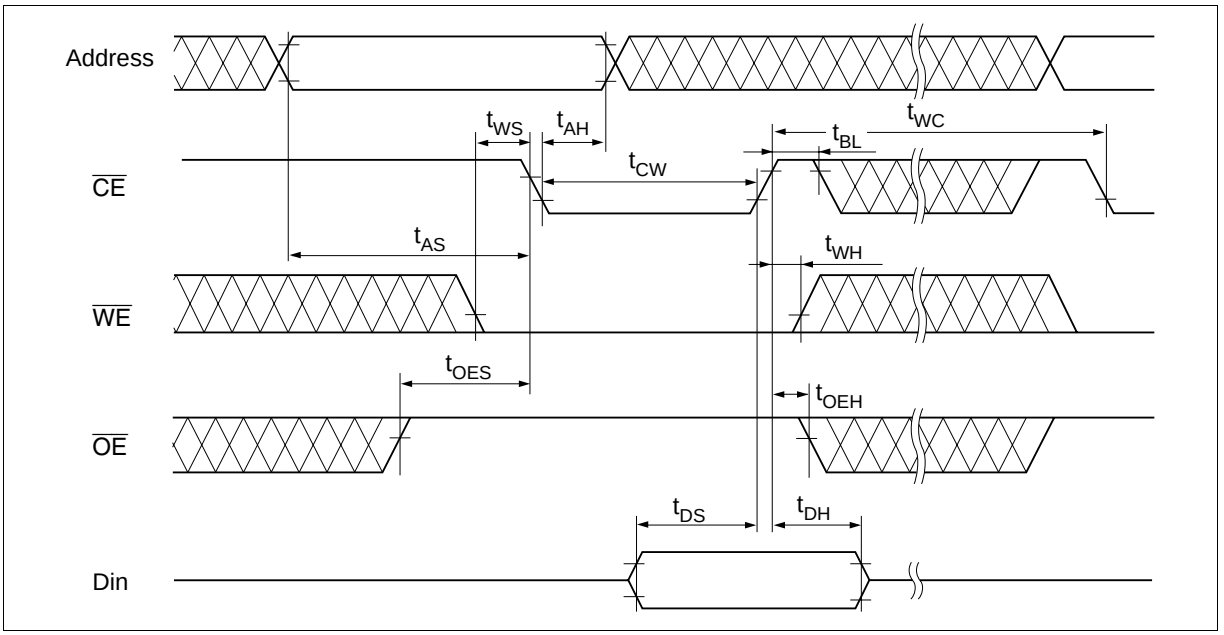
Read Timing Waveform



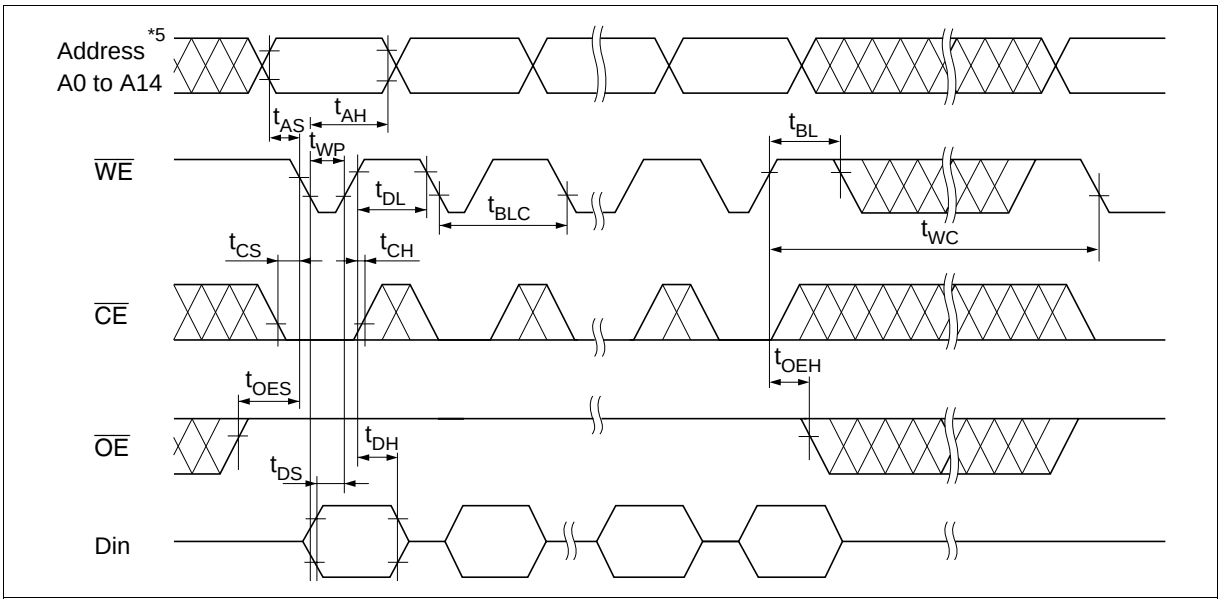
Byte Write Timing Waveform (1) ($\overline{WE}$ Controlled)



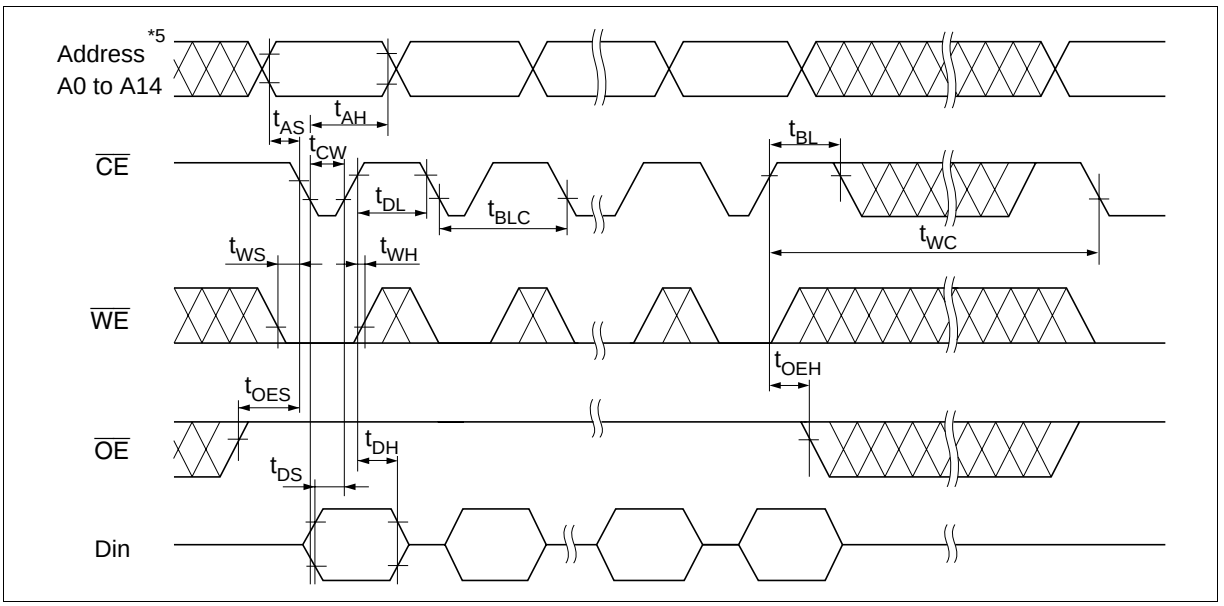
Byte Write Timing Waveform (2) ($\overline{CE}$ Controlled)



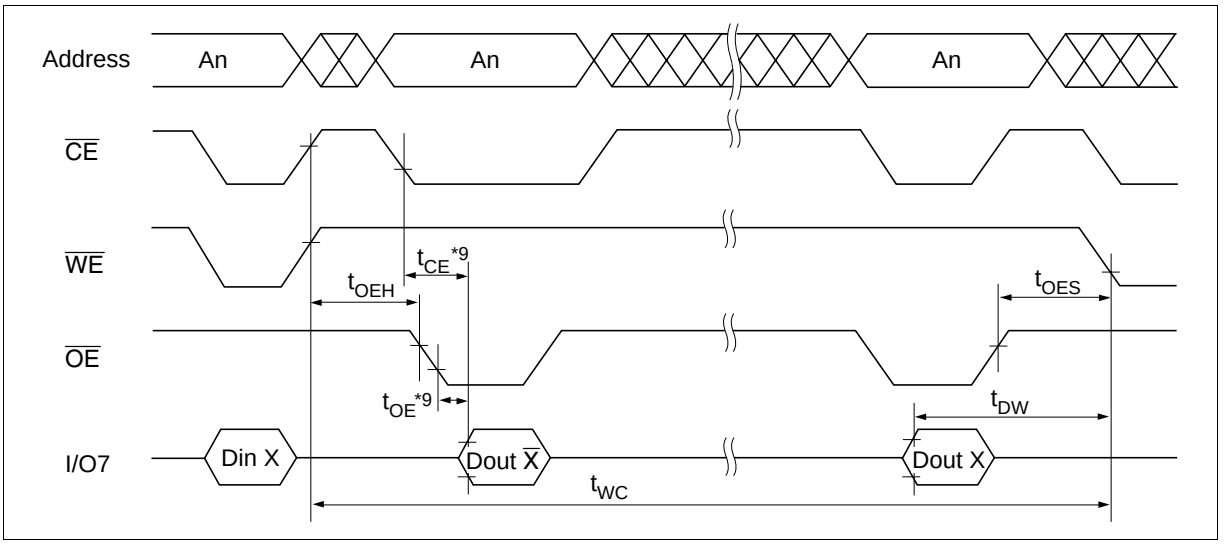
Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



$\overline{\text{Data}}$ Polling Timing Waveform

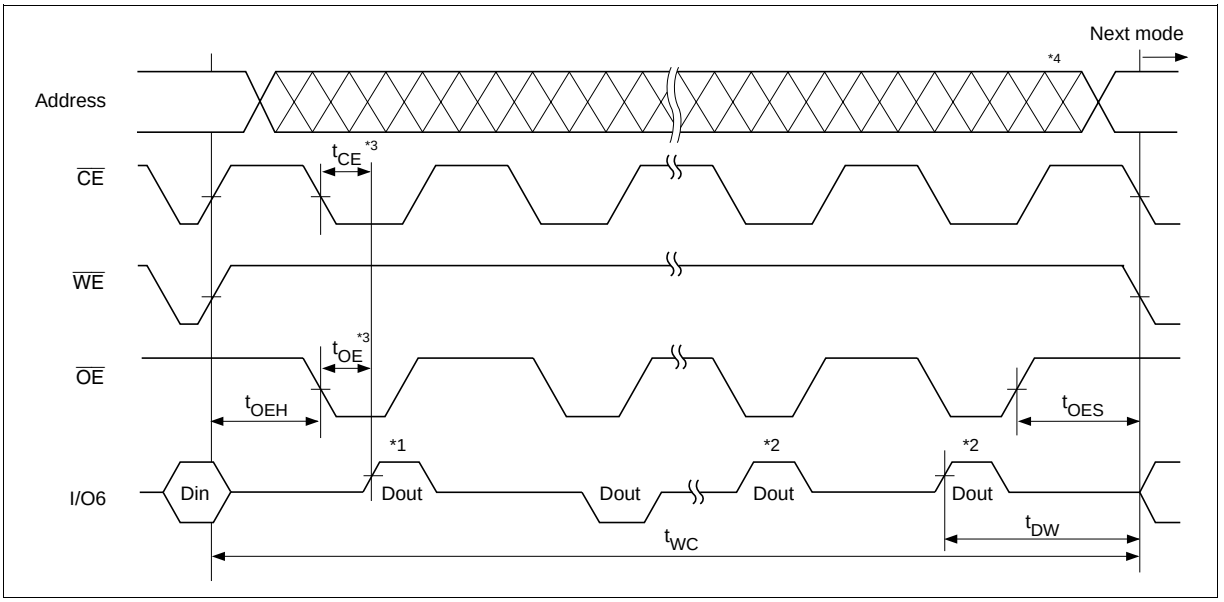


Toggle bit

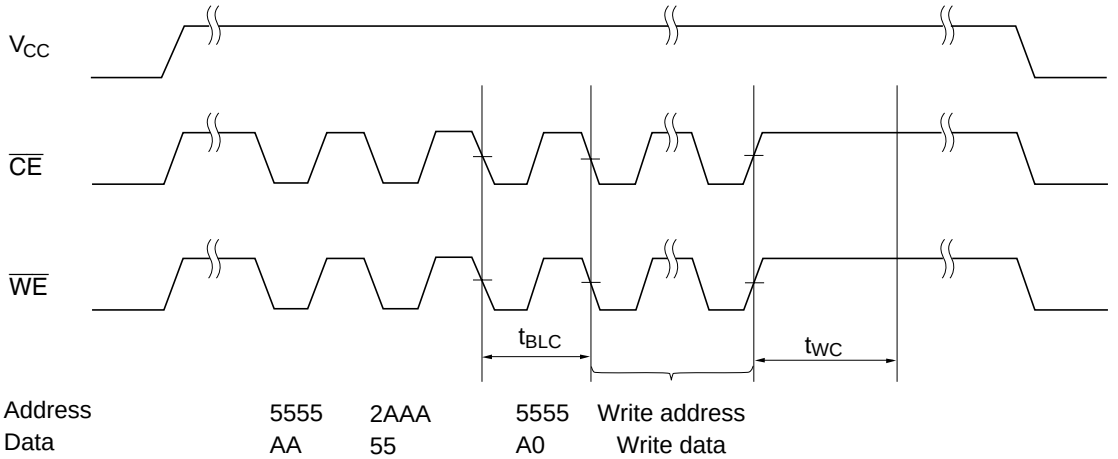
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle bit Waveform

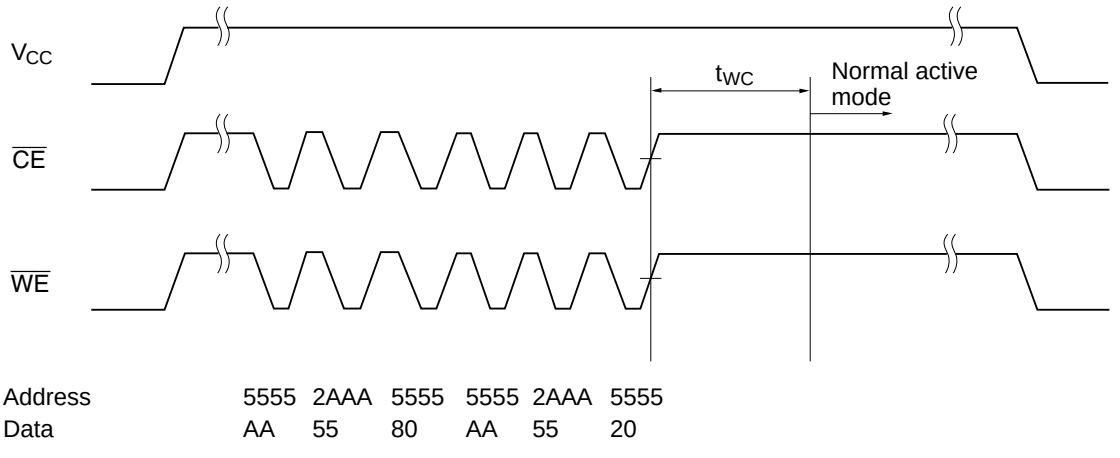
Notes: 1. I/O6 beginning state is "1".
2. I/O6 ending state will vary.
3. See AC read characteristics.
4. Any address location can be used, but the address must be fixed.



Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{Data}$ Polling

$\overline{Data}$ polling indicates the status that the EEPROM is in a write cycle or not. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data outputs from I/O7 to indicate that the EEPROM is performing a write operation.

$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

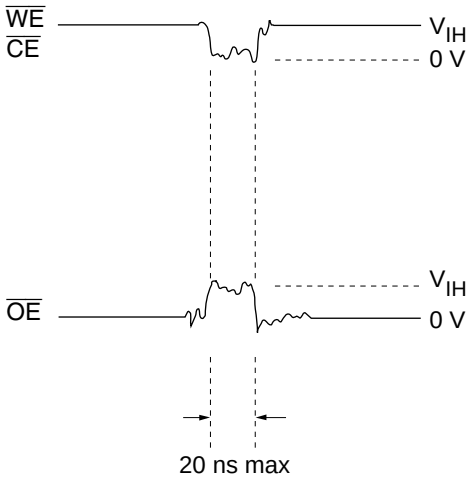
Data Protection

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 20 ns or less.

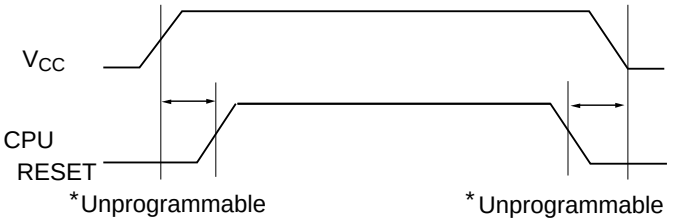
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

Note: The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.



(1) Protection by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{cc}	×	×
$\overline{OE}$	×	V_{ss}	×
$\overline{WE}$	×	×	V_{cc}

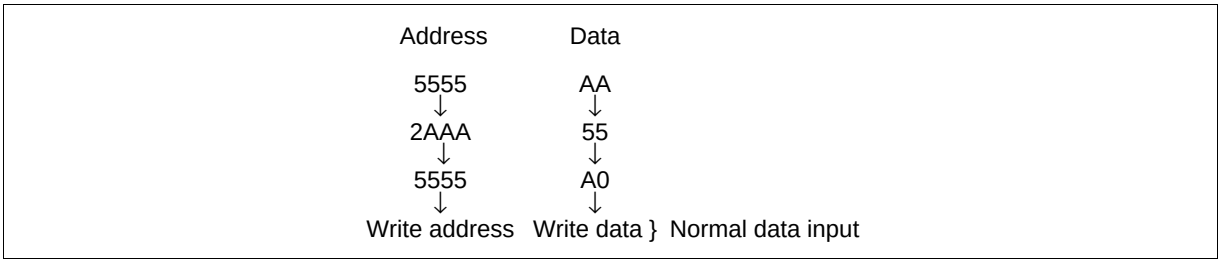
×: Don't care.

V_{cc}: Pull-up to V_{cc} level.

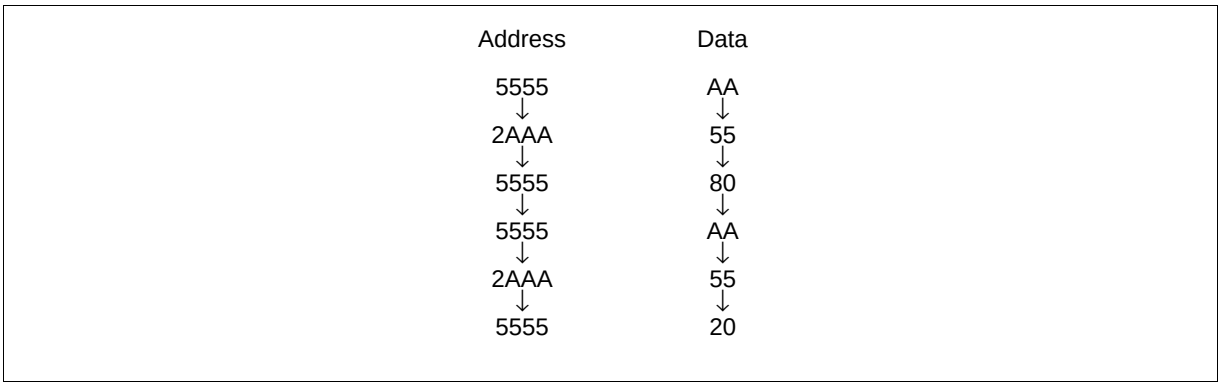
V_{ss}: Pull-down to V_{ss} level.

3. Software data protection

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the following 3 bytes code and write data. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data.



The SDP mode is disabled by inputting the following 6 bytes code. Note that, if data is input in the SDP disable cycle, data not be written.

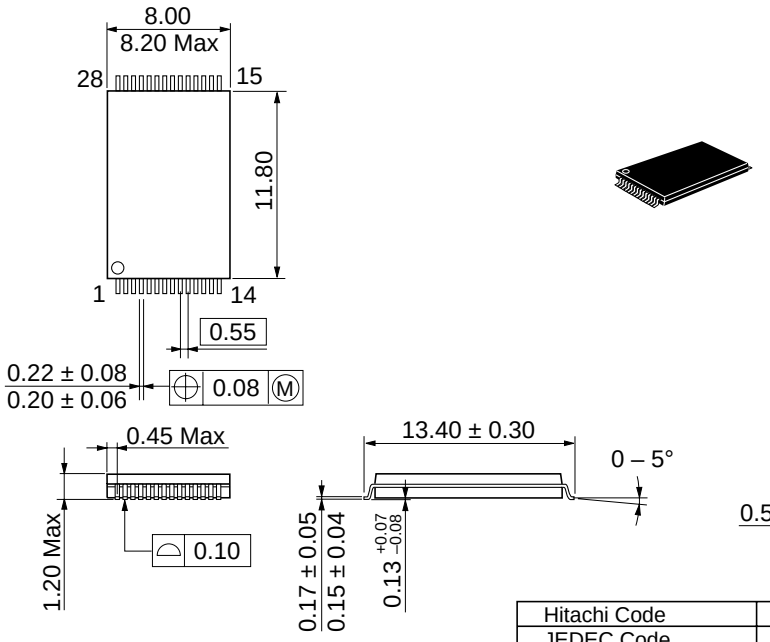


The software data protection is not enabled at the shipment.

Note: There are some differences between Hitachi's and other company's for enable/disable sequence of software data protection. If there are any questions , please contact with Hitachi sales offices.

Package Dimensions

HN58S256ATI Series (TFP-28DB) Unit: mm



Hitachi Code	TFP-28DB
JEDEC Code	—
EIAJ Code	—
Weight	0.23 g

When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. MEDICAL APPLICATIONS: Hitachi's products are not authorized for use in MEDICAL APPLICATIONS without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in MEDICAL APPLICATIONS.

HITACHI

Hitachi, Ltd.
Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Oct. 21, 1996	Initial issue	Y. Nagai	T. Wada
0.1	Mar. 4, 1997	Functional Description Data Protection 3: Addition of note	Y. Nagai	K. Furusawa
1.0	May. 20, 1997	Functional Description Data Protection 3: Change of description		