Motor Control Current Measurement
1-Bit, 10MHz, 2nd-Order, Delta-Sigma Modulator

FEATURES

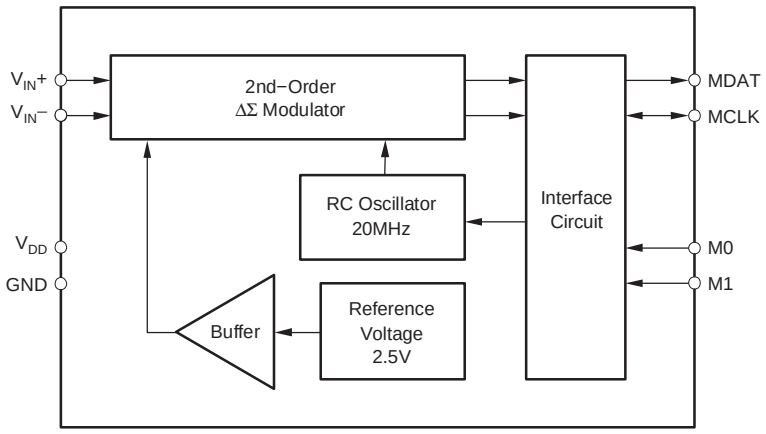
- **16-Bit Resolution**
- **14-Bit Linearity**
- **±250mV Input Range with Single +5V Supply**
- **1% Internal Reference Voltage**
- **1% Gain Error**
- **Flexible Serial Interface with Four Different Modes**
- **Implemented Twinned Binary Coding as Split-Phase or Manchester Coding for One-Line Interfacing**
- **Operating Temperature Range: −40°C to +85°C**

APPLICATIONS

- **Motor Control**
- **Current Measurement**
- **Industrial Process Control**
- **Instrumentation**
- **Smart Transmitters**
- **Portable Instruments**
- **Weight Scales**
- **Pressure Transducers**

DESCRIPTION

The ADS1203 is a delta-sigma (ΔΣ) modulator with a 95dB dynamic range, operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers or low-level signals. With the appropriate digital filter and modulator rate, the device can be used to achieve 16-bit analog-to-digital (A/D) conversion with no missing codes. An effective resolution of 14 bits or SNR of 85dB (typical) can be maintained with a digital filter bandwidth of 40kHz at a modulator rate of 10MHz. The ADS1203 is designed for use in medium- to high-resolution measurement applications including current measurements, smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation. It is available in an 8-lead TSSOP package. A 16-pin QFN (3x3) package will be available soon.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM GAIN ERROR (%)	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1203(2)	±3	±1	TSSOP-8	PW	−40°C to +85°C	AZ1203	ADS1203IPWT	Tape and Reel, 250
							ADS1203IPWR	Tape and Reel, 2000

(1) For the most current specification and package information, refer to our web site at www.ti.com.
(2) 16-pin QFN (3x3) package available soon.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	ADS1203	UNIT
Supply voltage, GND to V_{DD}	−0.3 to +6	V
Analog input voltage range	GND − 0.4 to V_{DD} + 0.3	V
Digital input voltage range	GND − 0.3 to V_{DD} + 0.3	V
Power Dissipation	0.25	W
Operating Virtual Junction Temperature Range, T_J	−40 to +150	°C
Operating Free-Air Temperature Range, T_A	−40 to +85	°C
Storage Temperature Range, T_{STG}	−65 to +150	°C
Lead Temperature (1.6mm or 1/16″ from case for 10s)	+260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}	4.5	5.0	5.5	V
Analog Input Voltage	−250		+250	mV
Operating Common-Mode Signal	0		+5	V
External Clock(1)	16	20	24	MHz
Operating Junction Temperature Range	−40		+105	°C

(1) With reduced accuracy, clock can go from 1MHz up to 32MHz; see Typical Characteristic curves.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$(1)	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
TSSOP-8	483.6mW	3.868mW/°C	309.5mW	251.4W

(1) This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$). Thermal resistances are not production tested and are for informational purposes only.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at −40°C to +85°C, V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, Mode 3, MCLK input = 20MHz, and 16-bit Sinc3 filter, with OSR = 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1203IPW			UNITS
			MIN	TYP(1)	MAX	
Resolution			16			Bits
DC Accuracy						
INL	Integral linearity error(2)			±1	±3	LSB
				0.001	0.005	%
DNL	Differential nonlinearity(3)				±1	LSB
V_{OS}	Input offset			−220	±1000	µV
TCV_{OS}	Input offset drift			3.5	8	µV/°C
G_{ERR}	Gain error(4)			−0.2	±1	%
TCG_{ERR}	Gain error drift			20		ppm/°C
PSRR	Power-supply rejection ratio	4.75V < V_{DD} < 5.25V		80		dB
Analog Input						
FSR	Full-scale differential range	(V_{IN}+) − (V_{IN}−)			±320	mV
	Operating common-mode signal(3)		−0.1		5	V
	Input capacitance	Common-mode		3		pF
	Input leakage current				±1	nA
	Differential input resistance	Equivalent		28		kΩ
	Differential input capacitance			5		pF
CMRR	Common-mode rejection ratio	At DC		92		dB
		V_{IN} = 0V to 5V at 50kHz		105		dB
Internal Voltage Reference						
V_{OUT}	Reference voltage output	Scale to 320mV	2.475	2.5	2.525	V
	Accuracy	Scale to 320mV			±1	%
dV_{OUT}/dT	Reference temperature drift			±20		ppm/°C
PSRR	Power-supply rejection ratio			80		dB
	Startup time	to 0.1% at C_L = 0		0.1		ms
Internal Clock for Modes 0, 1, and 2						
	Clock frequency		9	10	11	MHz
External Clock for Mode 3						
	Clock frequency(5)		16	20	24	MHz
AC Accuracy						
SINAD	Signal-to-noise + distortion	V_{IN} = ±250mV$_{PP}$ at 5kHz	82.5	85		dB
SNR	Signal-to-noise ratio	V_{IN} = ±250mV$_{PP}$ at 5kHz	83	85		dB
THD	Total harmonic distortion	V_{IN} = ±250mV$_{PP}$ at 5kHz		−95	−88	dB
SFDR	Spurious-free dynamic range	V_{IN} = ±250mV$_{PP}$ at 5kHz	90	95		dB

(1) All typical values are at T_A = +25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for V_{IN}+ = −250mV to +250mV, expressed either as the number of LSBs or as a percent of measured input range (500mV).
(3) Ensured by design.
(4) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(5) With reduced accuracy, minimum clock can go from 1MHz up to 32MHz.

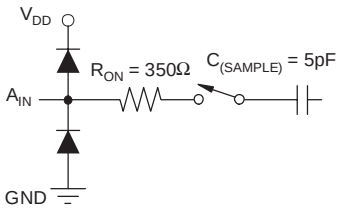
ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating free-air temperature range at −40°C to +85°C, V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, Mode 3, MCLK input = 20MHz, and 16-bit $Sinc^3$ filter, with OSR = 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1203IPW			UNITS
			MIN	TYP(1)	MAX	
Digital Input						
	Logic family		CMOS with Schmitt Trigger			
V_{IH}	High-level input voltage		$0.7 \times V_{DD}$		V_{DD} + 0.3	V
V_{IL}	Low-level input voltage		−0.3		$0.3 \times V_{DD}$	V
I_{IH}	High-level Input current	$V_I = V_{DD}$ or GND			50	nA
I_{IL}	Low-level Input current	$V_I = V_{DD}$ or GND	−50			nA
C_I	Input capacitance			5		pF
Digital Output						
V_{OH}	High-level digital output	V_{DD} = 5V, I_O = −5mA	4.6			V
		V_{DD} = 5V, I_O = −15mA	3.9			V
V_{OL}	Low-level digital output	V_{DD} = 5V, I_O = 5mA			0.4	V
		V_{DD} = 5V, I_O = 15mA			1.1	V
C_O	Output capacitance		5			pF
C_L	Load capacitance			30		pF
Power Supply						
V_{DD}	Supply voltage		4.5	5	5.5	V
I_{CC}	Operating supply current	Mode 0		8.4	9.8	mA
		Mode 3		6.7	7.8	mA
	Power dissipation	Mode 0		42	49	mW
		Mode 3		33.5	39	mW
Operating Temperature Range			−40		+85	°C

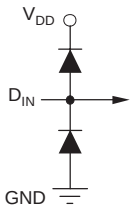
(1) All typical values are at T_A = +25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for V_{IN}+ = −250mV to +250mV, expressed either as the number of LSBs or as a percent of measured input range (500mV).
(3) Ensured by design.
(4) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(5) With reduced accuracy, minimum clock can go from 1MHz up to 32MHz.

EQUIVALENT INPUT CIRCUIT



Diode Turn-on Voltage: 0.4V

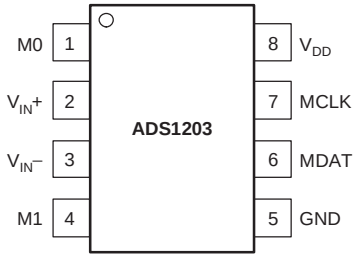
Equivalent Analog Input Circuit



Equivalent Digital Input Circuit

PIN ASSIGNMENTS

TSSOP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
M0	1	I	Mode input
V_{IN}+	2	AI	Noninverting analog input
V_{IN}−	3	AI	Inverting analog input
M1	4	I	Mode input
GND	5	P	Power supply ground
MDAT	6	O	Modulator data output
MCLK	7	I/O	Modulator clock input or output
V_{DD}	8	P	Power supply: +5V nominal

NOTE: AI = analog input, AO = analog output, I = input, O = output, P = power supply.

PARAMETER MEASUREMENT INFORMATION

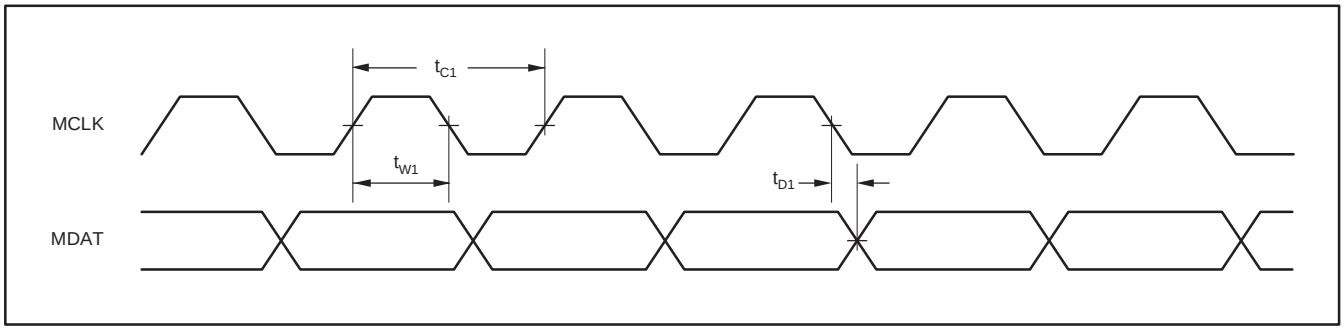


Figure 1. Mode 0 Operation

TIMING CHARACTERISTICS: MODE 0

over recommended operating free-air temperature range at −40°C to +85°C, and V_{DD} = +5V, unless otherwise noted.

PARAMETER		MODE	MIN	MAX	UNIT
t_{C1}	Clock period	0	91	111	ns
t_{W1}	Clock high time	0	$(t_{C1}/2) - 5$	$(t_{C1}/2) + 5$	ns
t_{D1}	Data delay after falling edge of clock	0	−2	2	ns

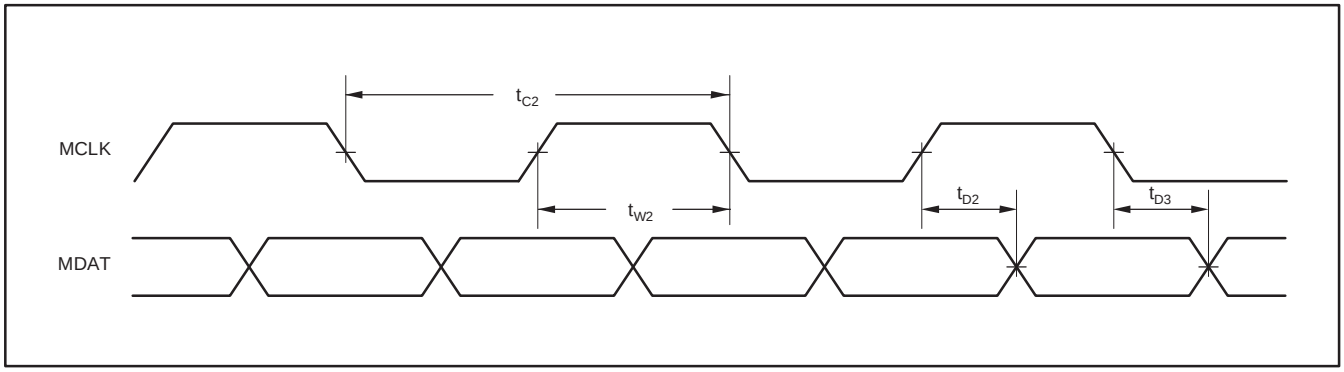


Figure 2. Mode 1 Operation

TIMING CHARACTERISTICS: MODE 1

over recommended operating free-air temperature range at −40°C to +85°C, and V_{DD} = +5V, unless otherwise noted.

PARAMETER		MODE	MIN	MAX	UNIT
t_{C2}	Clock period	1	182	222	ns
t_{W2}	Clock high time	1	$(t_{C2}/2) - 5$	$(t_{C2}/2) + 5$	ns
t_{D2}	Data delay after rising edge of clock	1	$(t_{W2}/2) - 2$	$(t_{W2}/2) + 2$	ns
t_{D3}	Data delay after falling edge of clock	1	$(t_{W2}/2) - 2$	$(t_{W2}/2) + 2$	ns

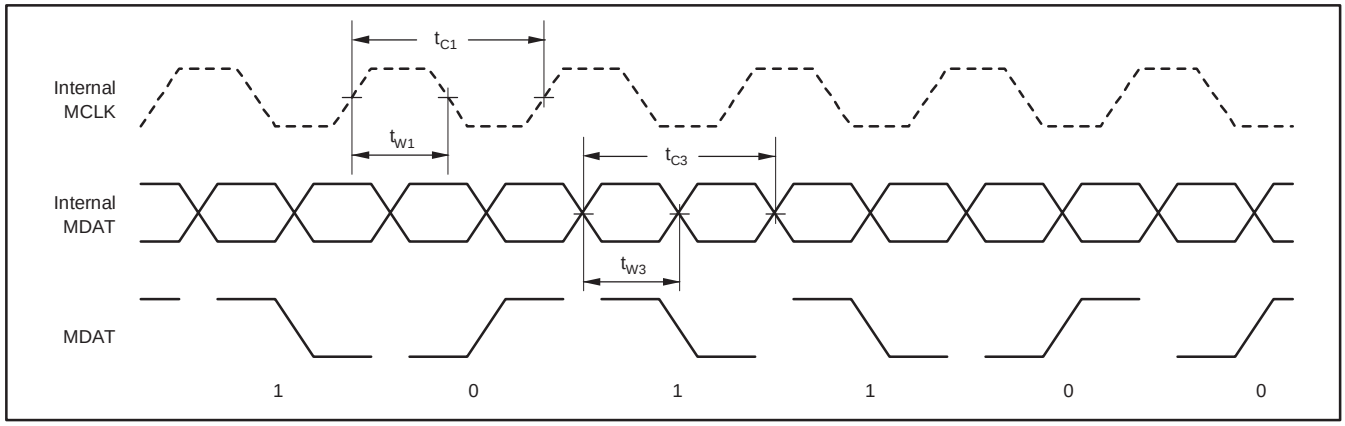


Figure 3. Mode 2 Operation

TIMING CHARACTERISTICS: MODE 2

over recommended operating free-air temperature range at −40°C to +85°C, and V_{DD} = +5V, unless otherwise noted.

PARAMETER		MODE	MIN	MAX	UNIT
t_{C1}	Clock period	2	91	111	ns
t_{W1}	Clock high time	2	$(t_{C1}/2) - 5$	$(t_{C1}/2) + 5$	ns
t_{C3}	Clock period	2	91	111	ns
t_{W3}	Clock high time	2	$(t_{C3}/2) - 5$	$(t_{C3}/2) + 5$	ns

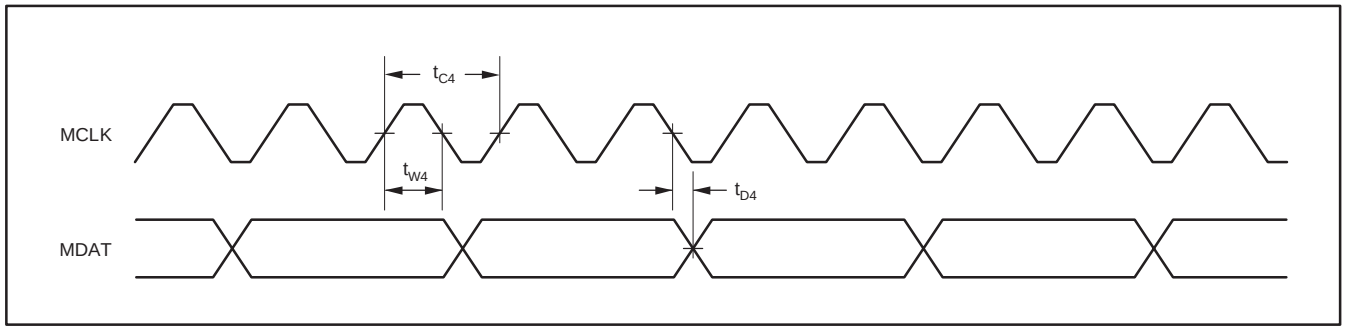


Figure 4. Mode 3 Operation

TIMING CHARACTERISTICS: MODE 3

over recommended operating free-air temperature range at −40°C to +85°C, and V_{DD} = +5V, unless otherwise noted.

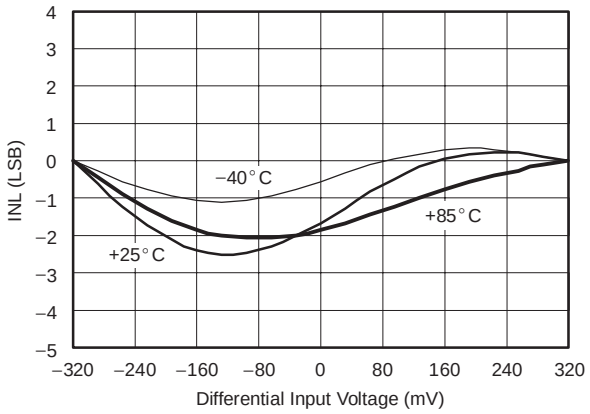
PARAMETER		MODE	MIN	MAX	UNIT
t_{C4}	Clock period	3	41	62	ns
t_{W4}	Clock high time	3	10	$t_{C4} - 10$	ns
t_{D4}	Data delay after falling edge of clock	3	0	10	ns
t_R	Rise time of clock	3	0	10	ns
t_F	Fall time of clock	3	0	10	ns

NOTE: Clock signal is specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$; see Figure 4.

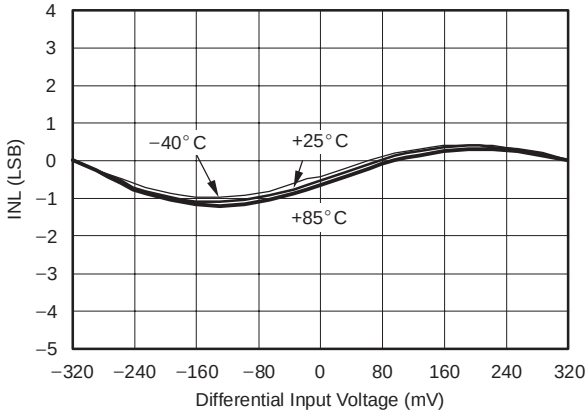
TYPICAL CHARACTERISTICS

V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, MCLK input = 20MHz, and 16-bit Sinc^3 filter, with OSR = 256, unless otherwise noted.

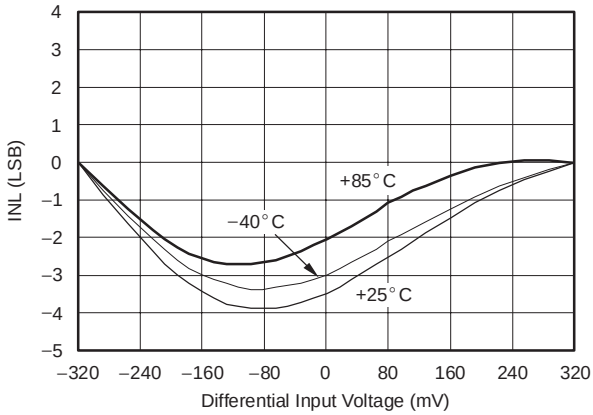
INTEGRAL NONLINEARITY vs INPUT SIGNAL
(Mode 0)



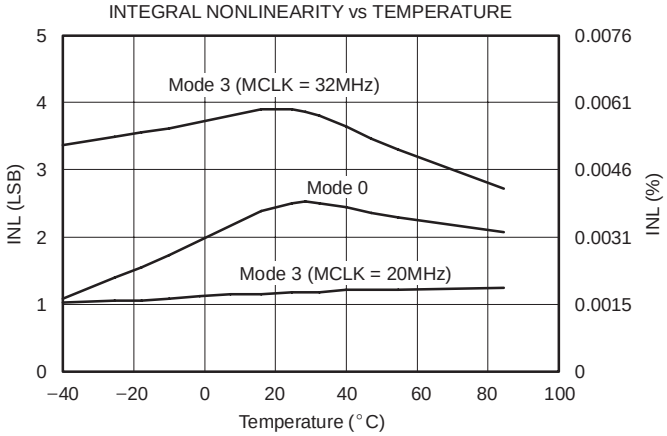
INTEGRAL NONLINEARITY vs INPUT SIGNAL
(Mode 3, MCLK = 20MHz)



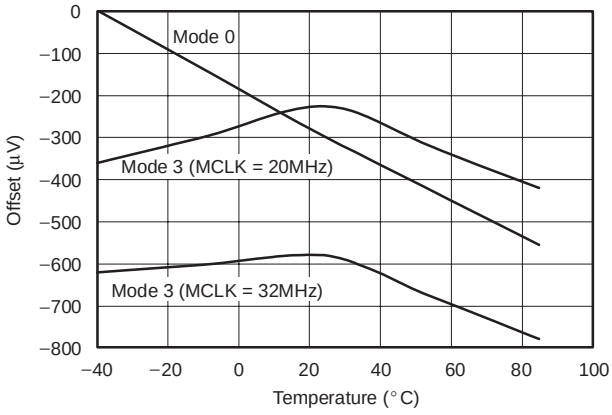
INTEGRAL NONLINEARITY vs INPUT SIGNAL
(Mode 3, MCLK = 32MHz)



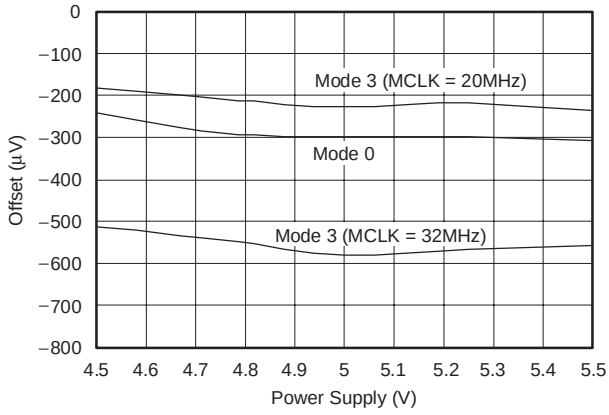
INTEGRAL NONLINEARITY vs TEMPERATURE



OFFSET vs TEMPERATURE



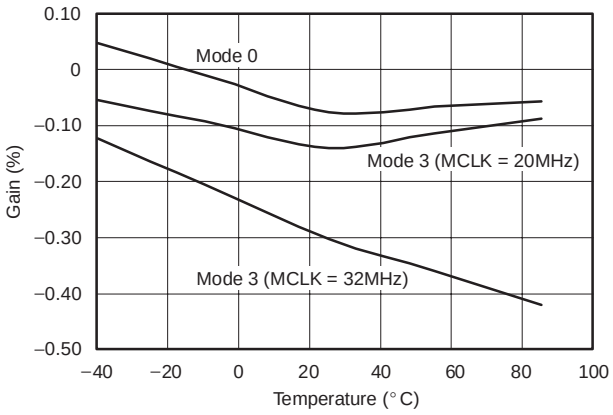
OFFSET vs POWER SUPPLY



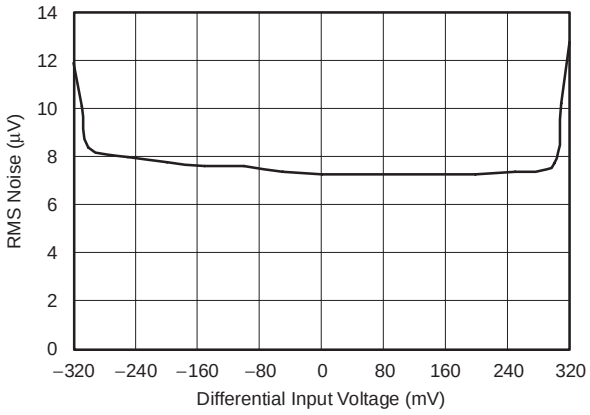
TYPICAL CHARACTERISTICS (continued)

V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, MCLK input = 20MHz, and 16-bit Sinc^3 filter, with OSR = 256, unless otherwise noted.

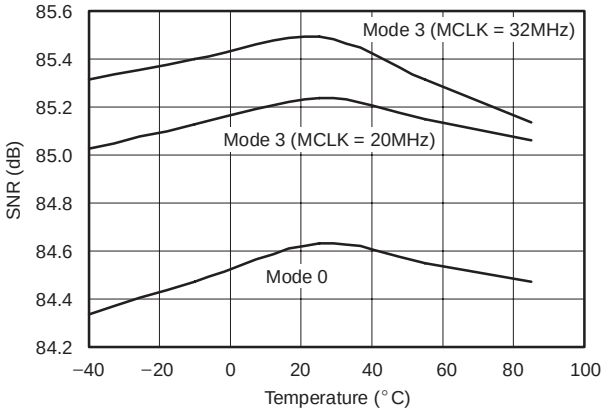
GAIN vs TEMPERATURE



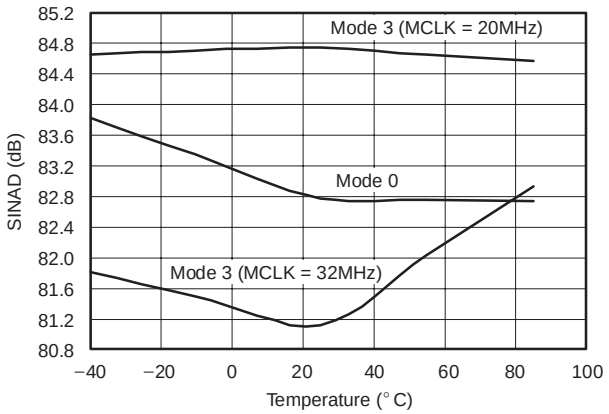
RMS NOISE vs INPUT VOLTAGE LEVEL



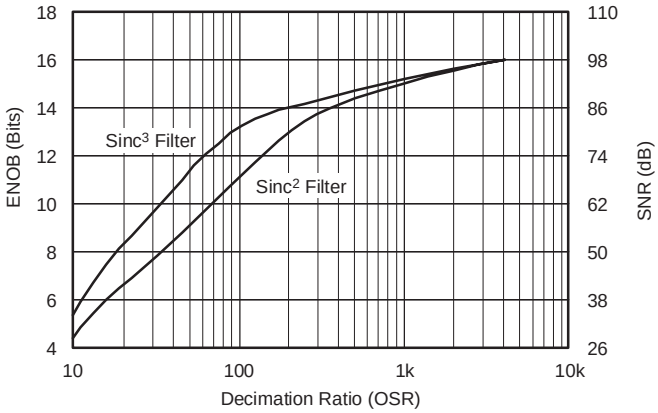
SIGNAL−TO−NOISE RATIO vs TEMPERATURE



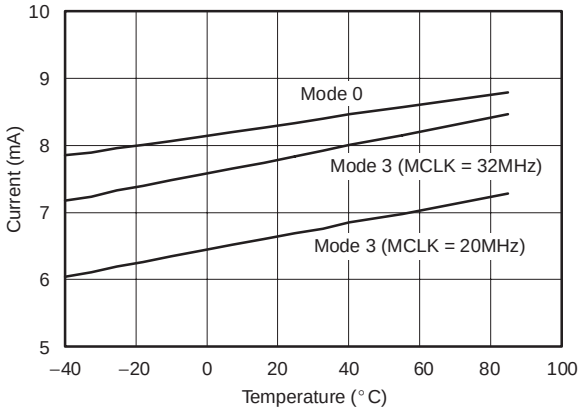
SIGNAL−TO−NOISE + DISTORTION vs TEMPERATURE



EFFECTIVE NUMBER OF BITS vs DECIMATION RATIO



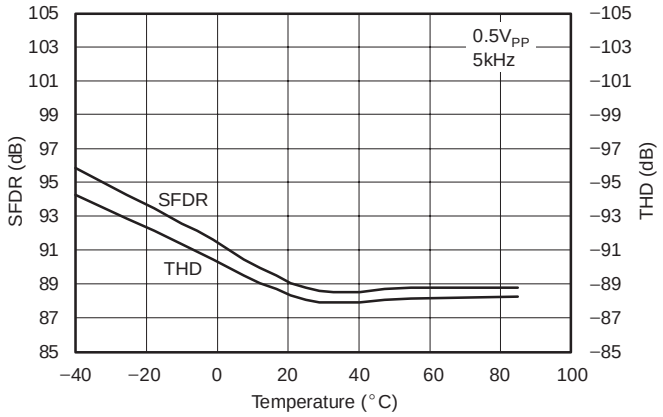
POWER−SUPPLY CURRENT vs TEMPERATURE



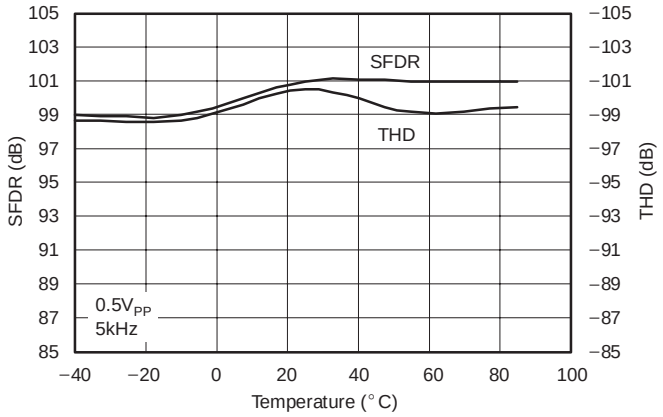
TYPICAL CHARACTERISTICS (continued)

V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, MCLK input = 20MHz, and 16-bit Sinc^3 filter, with OSR = 256, unless otherwise noted.

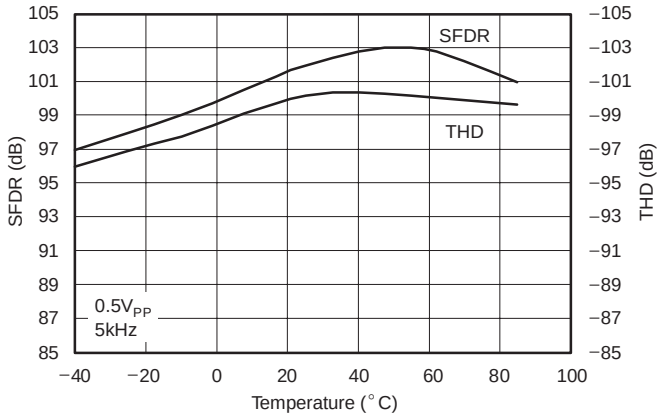
SPURIOUS−FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs TEMPERATURE (Mode 0)



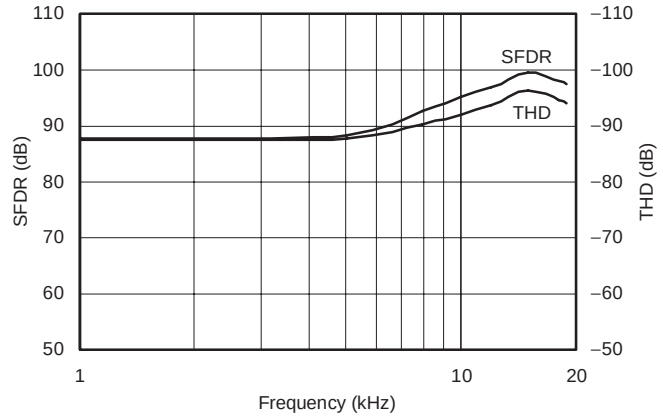
SPURIOUS−FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs TEMPERATURE (Mode 3, MCLK = 20MHz)



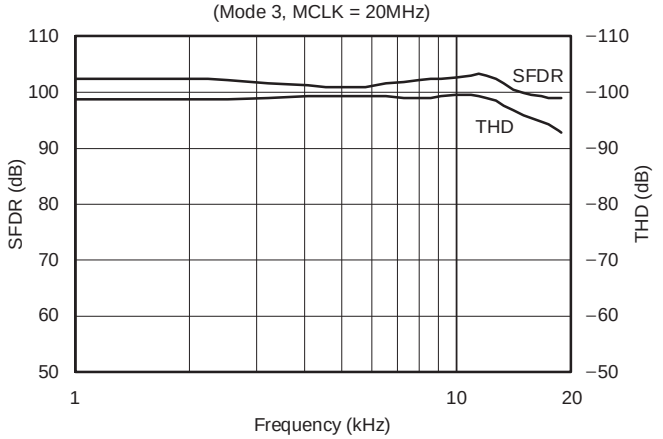
SPURIOUS−FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs TEMPERATURE (Mode 3, MCLK = 32MHz)



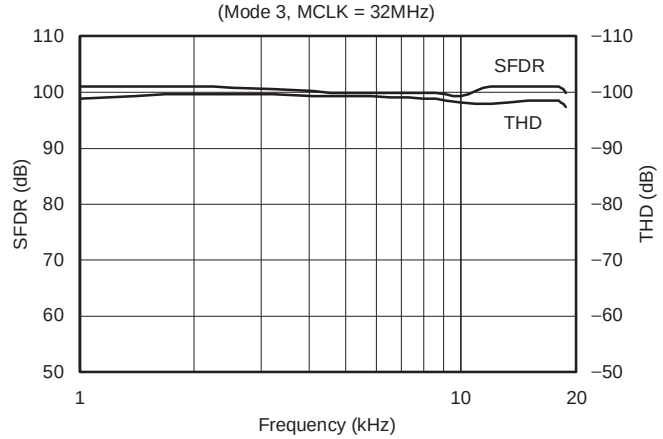
SPURIOUS−FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY (Mode 0)



SPURIOUS−FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY (Mode 3, MCLK = 20MHz)



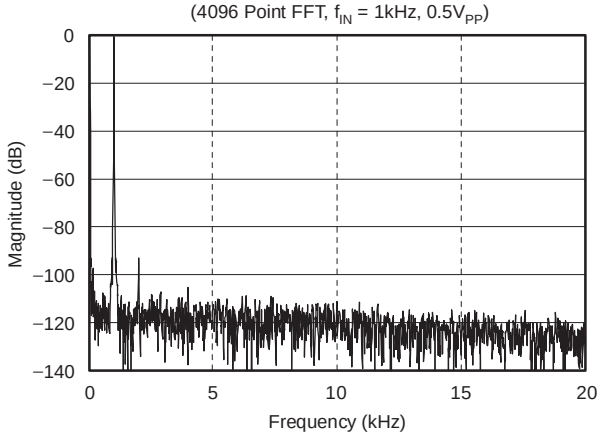
SPURIOUS−FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY (Mode 3, MCLK = 32MHz)



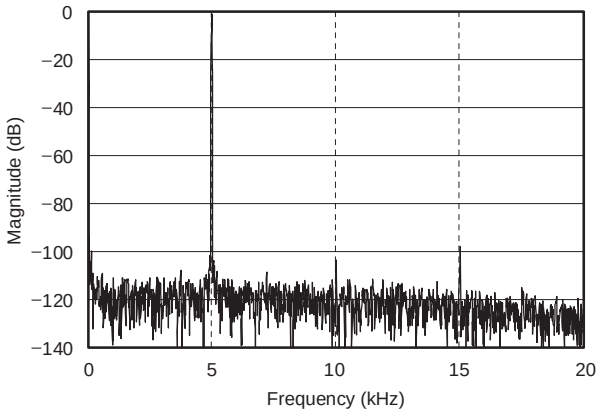
TYPICAL CHARACTERISTICS (continued)

V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, MCLK input = 20MHz, and 16-bit Sinc^3 filter, with OSR = 256, unless otherwise noted.

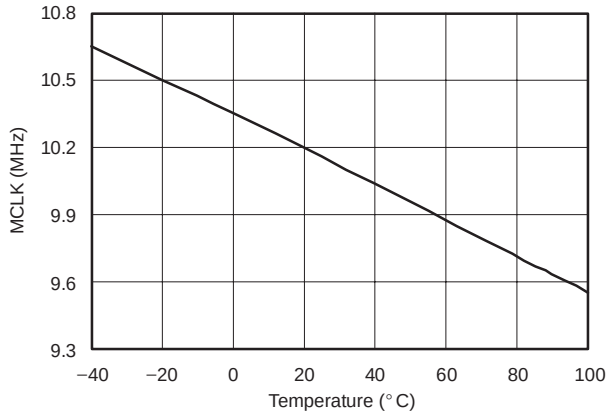
FREQUENCY SPECTRUM
(4096 Point FFT, f_{IN} = 1kHz, 0.5V_{PP})



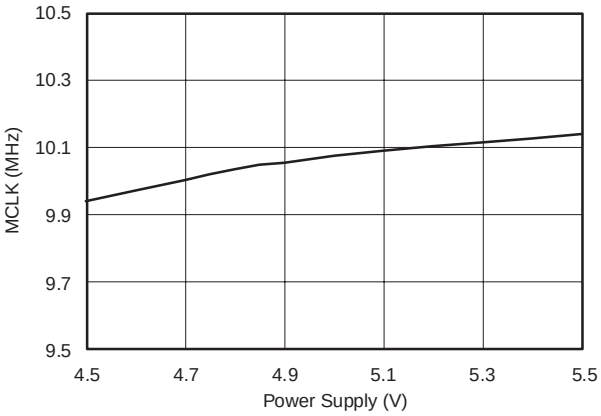
FREQUENCY SPECTRUM
(4096 Point FFT, f_{IN} = 5kHz, 0.5V_{PP})



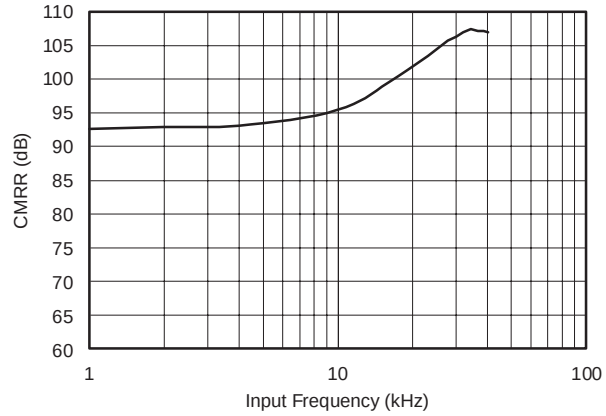
CLOCK FREQUENCY vs TEMPERATURE



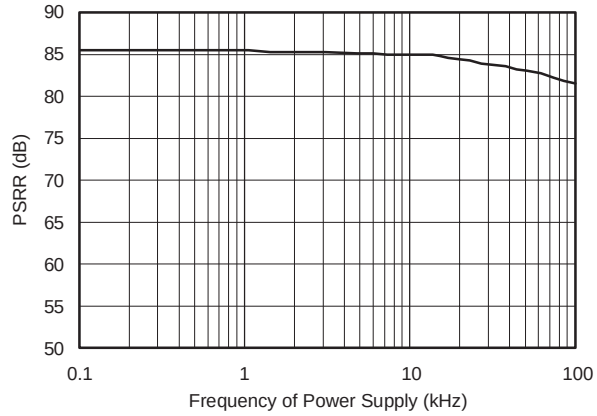
CLOCK FREQUENCY vs POWER SUPPLY



COMMON−MODE REJECTION RATIO
vs FREQUENCY



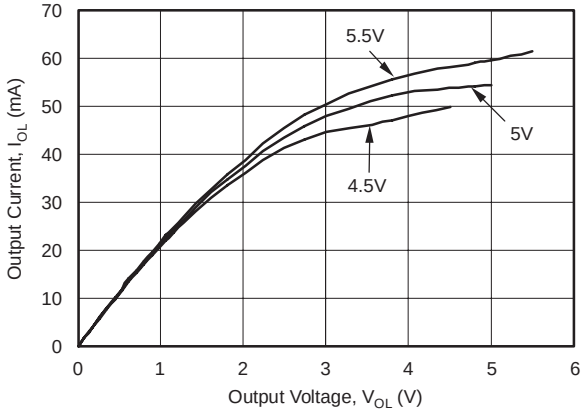
POWER−SUPPLY REJECTION RATIO
vs FREQUENCY



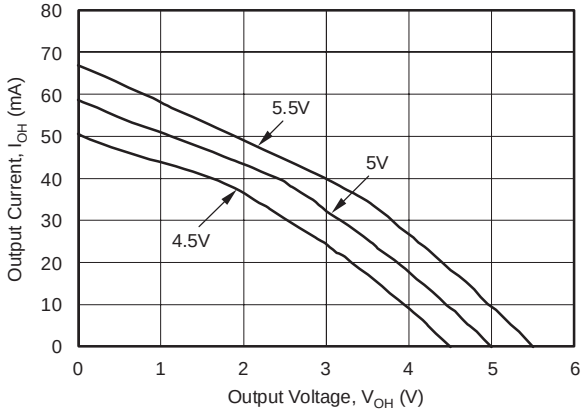
TYPICAL CHARACTERISTICS (continued)

V_{DD} = +5V, V_{IN}+ = −250mV to +250mV, V_{IN}− = 0V, MCLK input = 20MHz, and 16-bit Sinc^3 filter, with OSR = 256, unless otherwise noted.

MCLK AND MDAT
TYPICAL SINK CURRENT



MCLK AND MDAT
TYPICAL SOURCE CURRENT



GENERAL DESCRIPTION

The ADS1203 is a single-channel, 2nd-order, CMOS delta-sigma modulator, designed for medium- to high-resolution A/D conversions from DC to 39kHz with an oversampling ratio (OSR) of 256. The output of the converter (MDAT) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies. A low-pass digital filter should be used at the output of the delta-sigma modulator. The primary purpose of the digital filter is to filter out high-frequency noise. The secondary purpose is to convert the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). A digital signal processor (DSP), microcontroller (μC), or field programmable gate array (FPGA) could be used to implement the digital filter. Figure 5 shows the ADS1203 connected to a DSP.

The overall performance (speed and accuracy) depends on the selection of an appropriate OSR and filter type. A higher OSR produces greater output accuracy while operating at a lower refresh rate. Alternatively, a lower OSR produces lower output accuracy, but operates at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of A/D conversion results that have a dynamic range exceeding 95dB with an OSR = 256.

THEORY OF OPERATION

The differential analog input of the ADS1203 is implemented with a switched-capacitor circuit. This circuit implements a 2nd-order modulator stage, which digitizes the analog input signal into a 1-bit output stream. The clock source can be internal as well as external. Different frequencies for this clock allow for a variety of solutions and signal bandwidths (however, this can only be used in mode 3). The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream, which accurately represents the analog input voltage over time, appears at the output of the converter.

ANALOG INPUT STAGE

Analog Input

The input design topology of the ADS1203 is based on a fully differential switched-capacitor architecture. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (92dB), and excellent power-supply rejection.

The input impedance of the analog input is dependent on the modulator clock frequency (f_{CLK}), which is also the sampling frequency of the modulator. Figure 6 shows the basic input structure of the ADS1203. The relationship between the input impedance of the ADS1203 and the modulator clock frequency is:

$$Z_{IN} = \frac{28k\Omega}{f_{CLK}/10MHz} \quad (1)$$

The input impedance becomes a consideration in designs where the source impedance of the input signal is high. This may cause a degradation in gain, linearity and THD. The importance of this effect depends on the desired system performance. There are two restrictions on the analog input signals, V_{IN}+ and V_{IN}−. If the input voltage exceeds the range GND – 0.4V to V_{DD} + 0.3V, the input current must be limited to 10mA because the input protection diodes on the front end of the converter will begin to turn on. In addition, the linearity and the noise performance of the device is ensured only when the differential analog voltage resides within ±250mV; however, the FSR input voltage is ±320mV.

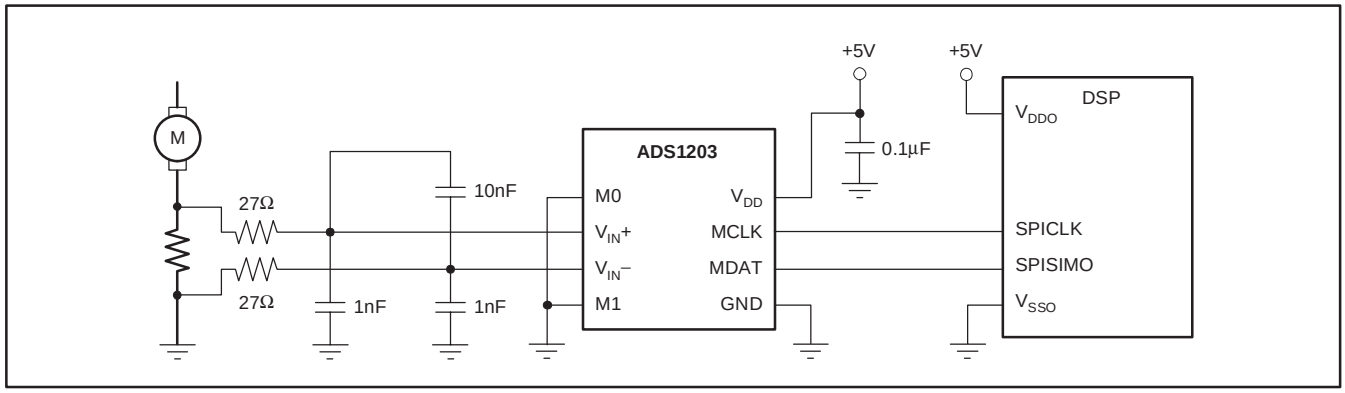


Figure 5. Connection Diagram for the ADS1203 Delta-Sigma Modulator Including DSP

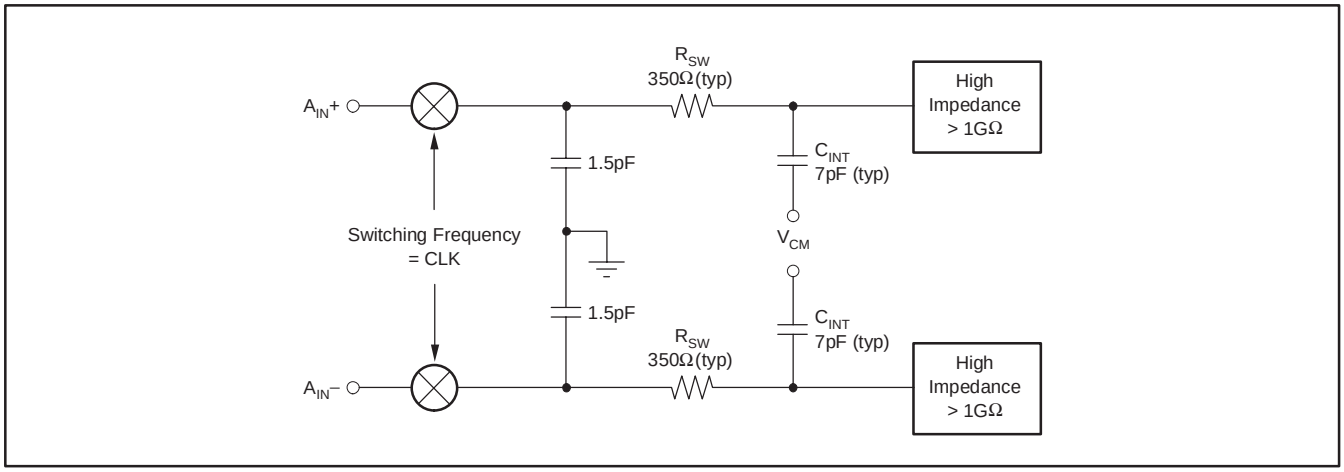


Figure 6. Input Impedance of the ADS1203

Modulator

The ADS1203 can be operated in four modes. Modes 0, 1, and 2 use the internal clock, which is fixed at 20MHz. The modulator can also be operated with an external clock in mode 3. In all modes, the clock is divided by 2 internally and is used as the modulator clock. The frequency of the external clock can vary from 1MHz to 32MHz to adjust for the clock requirements of the application.

The modulator topology is fundamentally a 2nd-order, switched-capacitor, delta-sigma modulator, such as the one conceptualized in Figure 7. The analog input voltage and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing analog voltages at X2 and X3. The voltages at X2 and X3 are presented to their individual integrators. The output of these integrators progress in a negative or positive direction. When the value of the signal at X4 equals the comparator reference voltage, the output of the comparator switches from negative to positive, or positive to negative, depending on its original state. When the output value of the comparator switches from high to low or vice versa, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage at X6, causing the integrators to progress in the opposite direction. The feedback of the modulator to the front end of the integrators forces the value of the integrator output to track the average of the input.

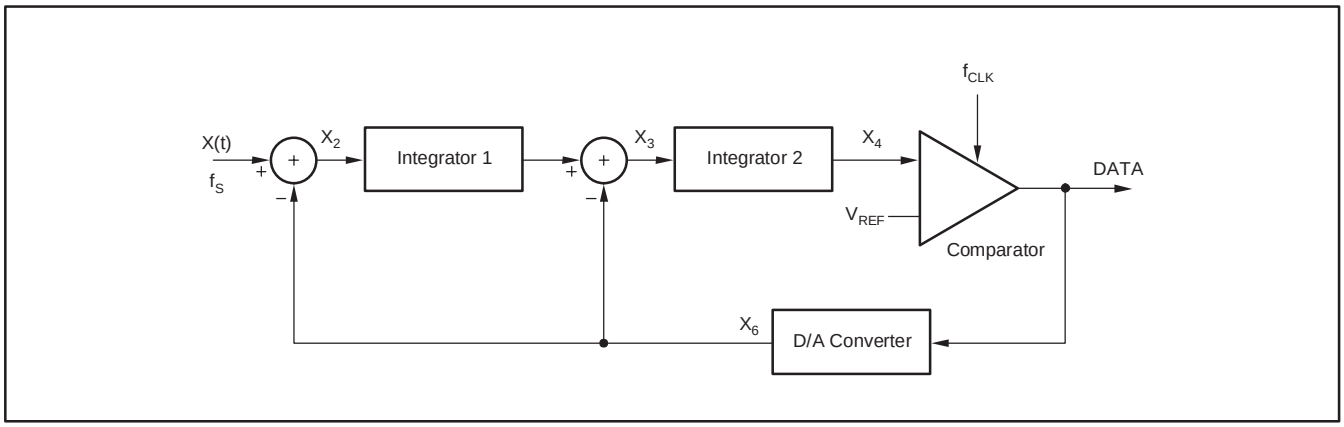


Figure 7. Block Diagram of the 2nd-Order Modulator

DIGITAL OUTPUT

A differential input signal of 0V will ideally produce a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of +256mV will produce a stream of ones and zeros that are high 80% of the time. A differential input of –256mV will produce a stream of ones and zeros that are high 20% of the time. The input voltage versus the output modulator signal is shown in Figure 8.

DIGITAL INTERFACE

INTRODUCTION

The analog signal that is connected to the input of the delta-sigma modulator is converted using the clock signal applied to the modulator. The result of the conversion, or modulation, is the output signal DATA from the delta-sigma modulator. In most applications where a direct connection is realized between the delta-sigma modulator and an ASIC, FPGA, DSP, or µC (each with an implemented filter), the two standard signals (MCLK and MDAT) are provided from the modulator. To reduce the wiring (for example, for galvanic isolation), a single line is preferred. Therefore, in mode 2, the data stream is Manchester encoded.

MODES OF OPERATION

The system clock of the ADS1203 is 20MHz by default. The system clock can be provided either from the internal 20MHz RC oscillator or from an external clock source. For this purpose, the MCLK pin is bidirectional and controlled by the mode setting.

The system clock is divided by 2 for the modulator clock. Therefore, the default clock frequency of the modulator is 10MHz. With a possible external clock range of 1MHz to 32MHz, the modulator operates between 500kHz and 16MHz.

The four modes of operation for the digital data interface are shown in Table 1.

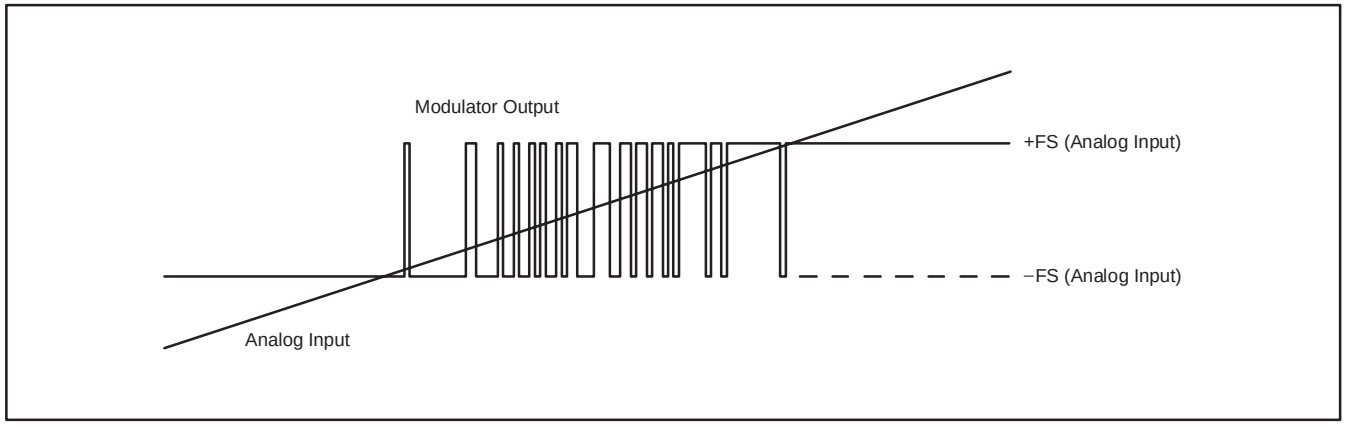


Figure 8. Analog Input vs Modulator Output of the ADS1203

Table 1. Digital Data Interface Modes of Operation

MODE	DEFINITION	M1	M0
0	Internal clock, synchronous data output	Low	Low
1	Internal clock, synchronous data output, half output clock frequency	Low	High
2	Internal clock, Manchester encoded data output	High	Low
3	External clock, synchronous data output	High	High

Mode 0

In mode 0, the internal RC oscillator is running. The data is provided at the MDAT output pin, and the modulator clock at the MCLK pin. The data is changing at the falling edge of MCLK; therefore, it can safely be strobed with the rising edge. See Figure 1 on page 6.

Mode 1

In mode 1, the internal RC oscillator is running. The data is provided at the MDAT output pin. The MCLK pin provides the half modulator clock. The data must be strobed at both the rising and falling edges of MCLK. The data at MDAT is changing in the middle, between the rising and falling edge. In this mode the frequency of both MCLK and MDAT is only 5MHz. See Figure 2 on page 6.

Mode 2

In mode 2, the internal RC oscillator is running. The data is Manchester encoded and is provided at the MDAT pin. The MCLK output is set to low. There is no clock output provided in this mode. The Manchester coding allows the data transfer with only a single line. See Figure 3 on page 7.

Mode 3

In mode 3, the internal RC oscillator is disabled. The system clock must be provided externally at the input MCLK. The system clock must have twice the frequency of the chosen modulator clock. The data is provided at the MDAT output pin. Since the modulator runs with the half system clock, the data changes at every other falling edge of the external clock. The data can safely be strobed at every other rising edge of MCLK. This mode allows synchronous operation to any digital system or the use of clocks different from 10MHz. See Figure 4 on page 7.

FILTER USAGE

The modulator generates only a bitstream, which does not output a digital word like an analog-to-digital converter (ADC). In order to output a digital word equivalent to the analog input voltage, the bitstream must be processed by a digital filter.

A very simple filter built with minimal effort and hardware is the sinc^3 filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^3 \qquad (2)$$

This filter provides the best output performance at the lowest hardware size (for example, count of digital gates). For oversampling ratios in the range of 16 to 256, this is a good choice. All the characterizations in the data sheet are also done using a sinc^3 filter with an oversampling ratio of OSR = 256 and an output word width of 16 bits.

In a sinc^3 filter response (shown in Figure 9 and Figure 10), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK}/OSR$. The –3dB point is located at half the Nyquist frequency or $f_{DATA}/4$. For some applications, it may be necessary to use another filter type for better frequency response.

This performance can be improved, for example, by a cascaded filter structure. The first decimation stage can be a sinc^3 filter with a low OSR and the second stage a high-order filter.

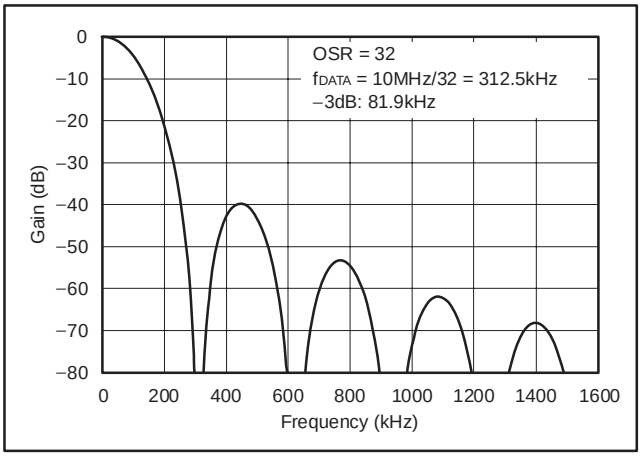


Figure 9. Frequency Response of Sinc^3 Filter

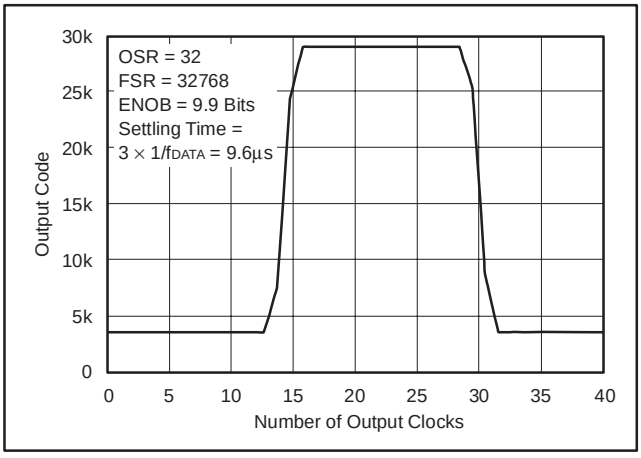


Figure 10. Pulse Response of Sinc^3 Filter (f_{MOD} = 10MHz)

The effective number of bits (ENOB) can be used to compare the performance of ADCs and delta-sigma modulators. Figure 11 shows the ENOB of the ADS1203 with different filter types. In this data sheet, the ENOB is calculated from the SNR:

$$SNR = 1.76dB + 6.02dB \times ENOB \quad (3)$$

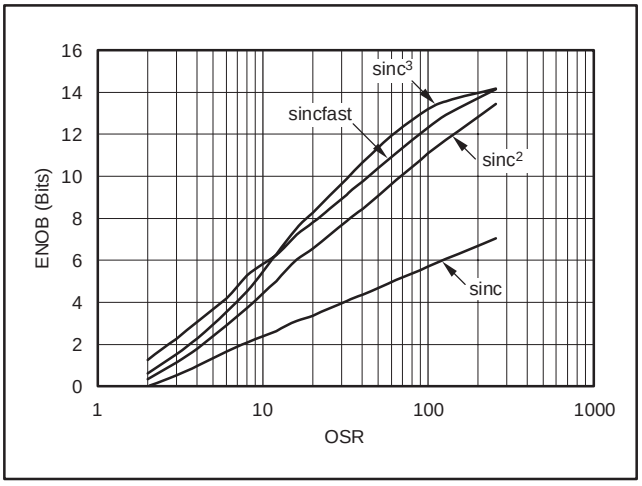


Figure 11. Measured ENOB vs OSR

In motor control applications, a very fast response time for overcurrent detection is required. There is a constraint between 1µs and 5µs with 3 bits to 7 bits resolution. The time for full settling is dependent on the filter order. Therefore, the full settling of the $sinc^3$ filter needs three data clocks and the $sinc^2$ filter needs two data clocks. The data clock is equal to the modulator clock divided by the OSR. For overcurrent protection, filter types other than $sinc^3$ might be a better choice. A simple example is a $sinc^2$ filter. Figure 12 compares the settling time of different filter types. The sincfast is a modified $sinc^2$ filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^2 \left(1 + z^{-2 \times OSR}\right) \quad (4)$$

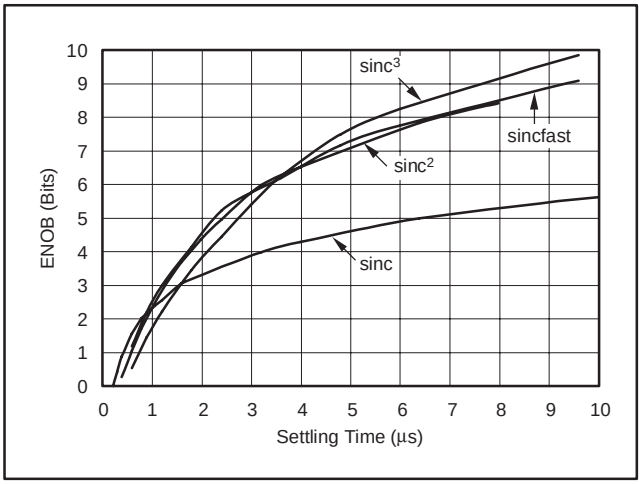


Figure 12. Measured ENOB vs Settling Time

For more information, see application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at www.ti.com.

APPLICATIONS

Operating the ADS1203 in a typical application using mode 0 is shown in Figure 13. Measurement of the motor phase current is done via the shunt resistor. For better performance, both signals are filtered. R_2 and C_2 filter noise on the noninverting input signal, R_3 and C_3 filter noise on the inverting input signal, and C_4 in combination with R_2 and R_3 filter the differential input signal. In this configuration, the shunt resistor is connected via three wires with the ADS1203.

The power supply is taken from the upper gate driver power supply. A decoupling capacitor of 0.1µF is recommended for filtering the power supply. If better filtering is required, an additional 1µF to 10µF capacitor can be added.

The control lines M0 and M1 are both low while the part is operating in mode 0. Two output signals, MCLK and MDAT, are connected directly to the optocoupler. The optocoupler can be connected to transfer a direct or inverse signal because the output stage has the capacity to source and sink the same current. The discharge resistor is not needed in parallel with optocoupler diodes because the output driver has push-pull capability to keep the LED diode out of the charge.

The DSP (such as a C28x or C24x) can be directly connected at the output of two channels of the optocoupler. In this configuration, the signals arriving at C28x or C24x are standard delta-sigma modulator signals and are connected directly to the SPICLK and SPISIMO pins. Being a delta-sigma converter, there is no need to have word sync on the serial data, so an SPI is ideal for connection. McBSP would work as well in SPI mode.

When component reduction is necessary, the ADS1203 can operate in mode 2, as shown in Figure 14. M1 is high and M0 is low. Only the noninverting input signal is filtered. R_2 and C_2 filter noise on the input signal. The inverting input is directly connected to the GND pin, which is simultaneously connected to the shunt resistor.

The output signal from the ADS1203 is Manchester coded. In this case, only one signal is transmitted. For that reason, one optocoupler channel is used instead of two channels, as in the previous example of Figure 13. Another advantage of this configuration is that the DSP will use only one line per channel instead of two. That permits the use of smaller DSP packages in the application.

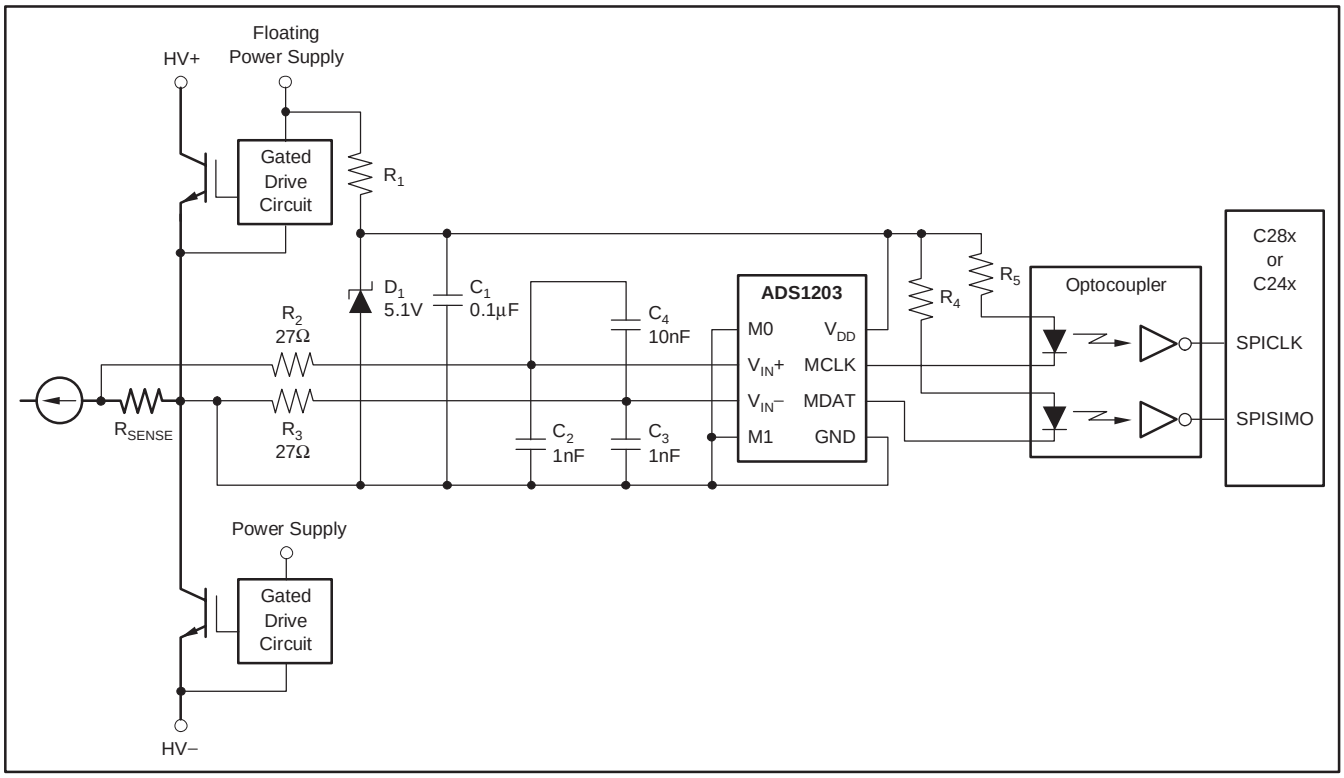


Figure 13. Application Diagram in Mode 0

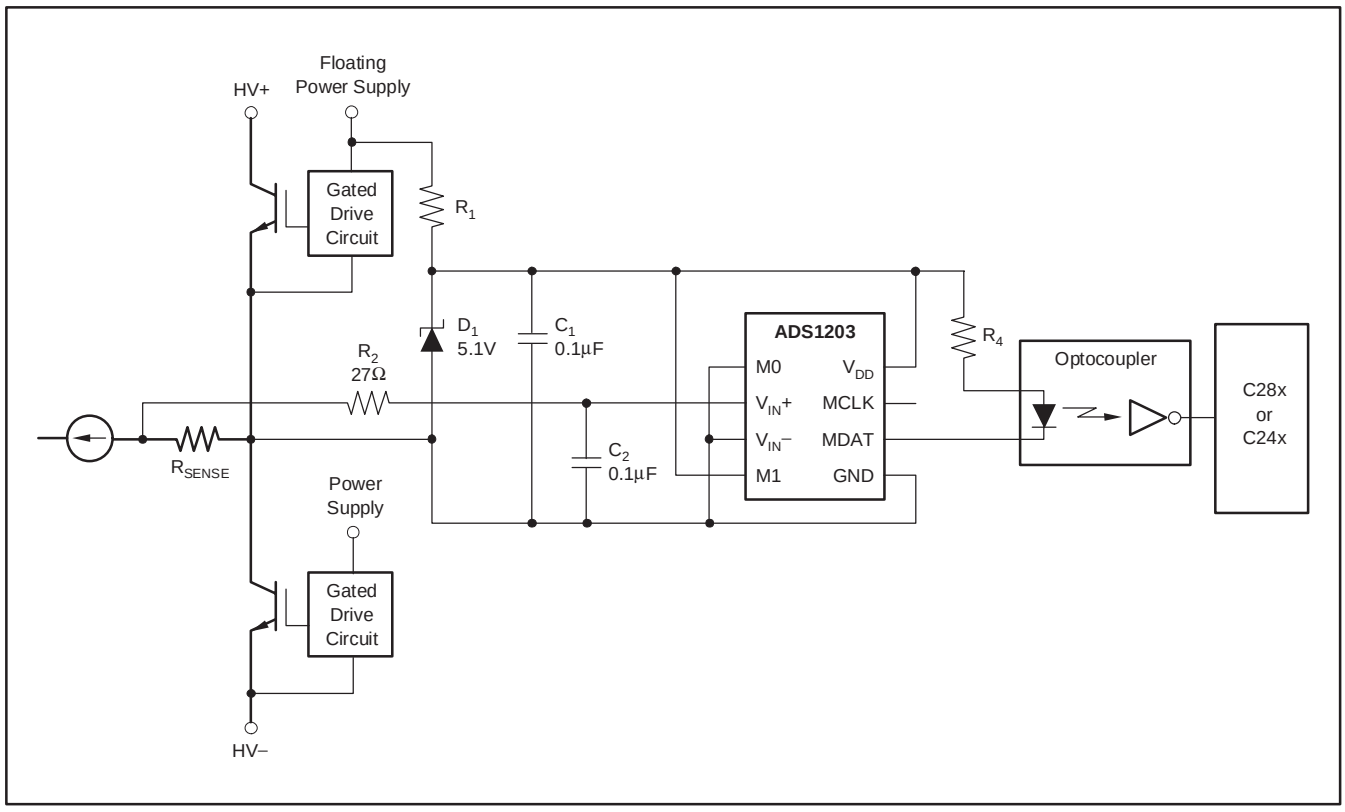


Figure 14. Application Diagram in Mode 2

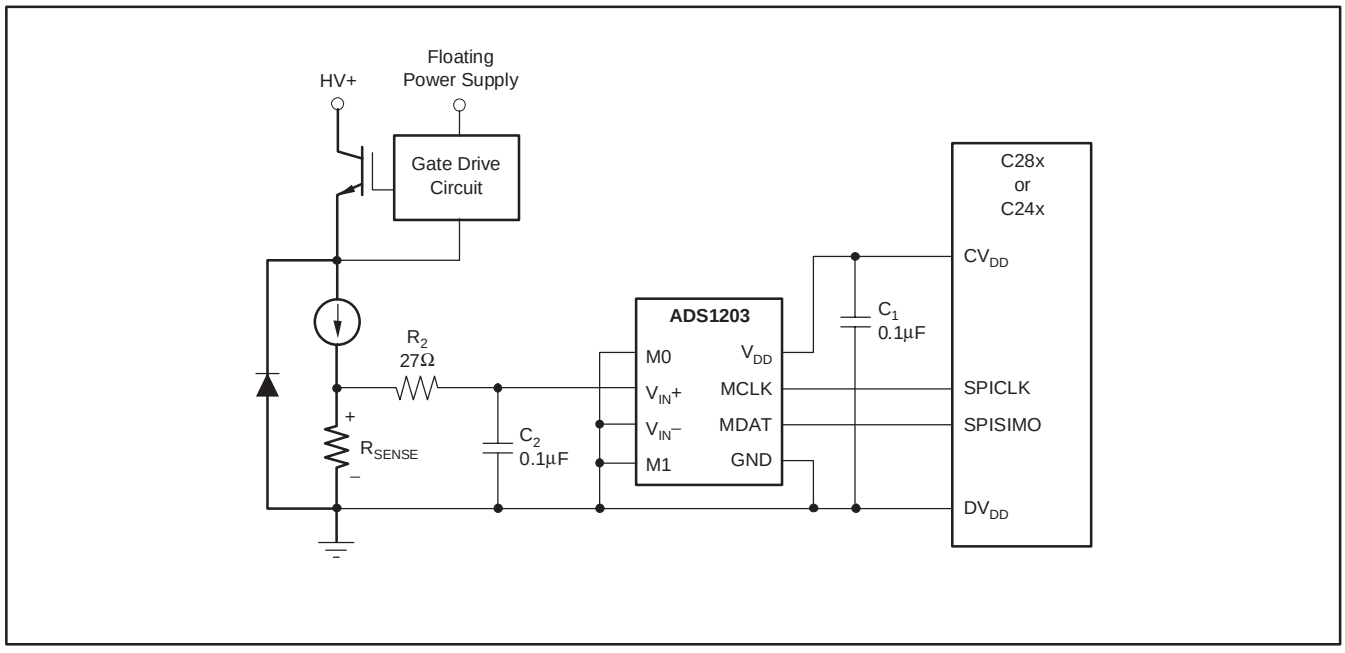


Figure 15. Application Diagram without Galvanic Isolation in Mode 0

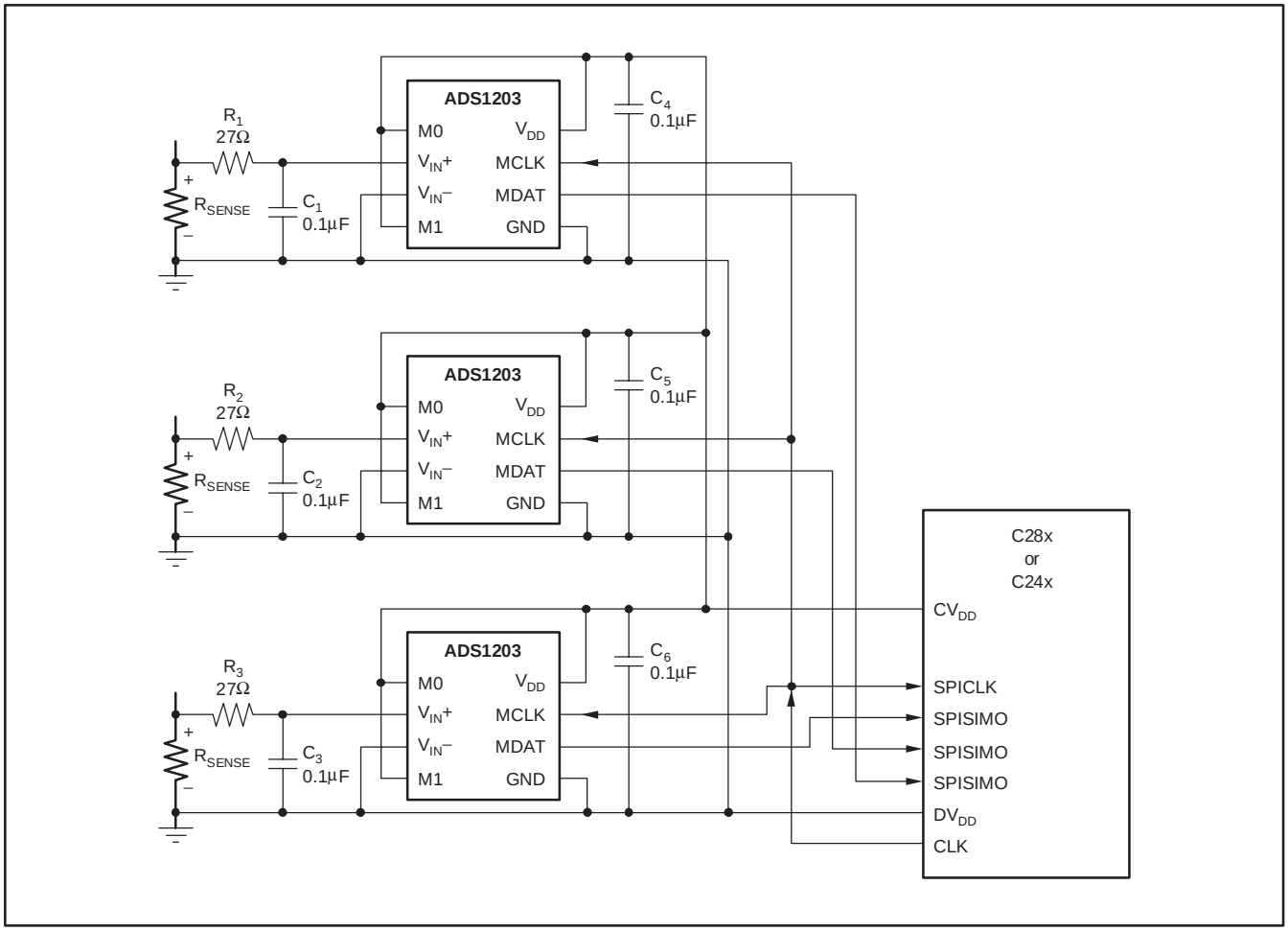


Figure 16. Application Diagram without Galvanic Isolation in Mode 3

LAYOUT CONSIDERATIONS

Power Supplies

The ADS1203 requires only one power supply (V_{DD}). If there are separate analog and digital power supplies on the board, a good design approach is to have the ADS1203 connected to the analog power supply. Another possible approach to control noise is the use of a resistor on the power supply. The connection can be made between the ADS1203 power-supply pins via a 10Ω resistor. The combination of this resistor and the decoupling capacitors between the power-supply pins on the ADS1203 provide some filtering. The analog supply that is used must be well regulated and generate low noise. For designs requiring higher resolution from the ADS1203, power-supply rejection will be a concern. The digital power supply has high-frequency noise that can be capacitively coupled into the analog portion of the ADS1203. This noise can originate from switching power supplies, microprocessors, or DSPs. High-frequency noise will generally be rejected by the external digital filter at integer multiples of MCLK. Just below and above these frequencies, noise will alias back into the passband of the digital filter, affecting the conversion result. Inputs to the ADS1203, such as $V_{IN}+$, $V_{IN}-$, and MCLK should not be present before the power supply is on. Violating this condition could cause latch-up. If these signals are present before the supply is on, series resistors should be used to limit the input current. Experimentation may be the best way to determine the appropriate connection between the ADS1203 and different power supplies.

Grounding

Analog and digital sections of the design must be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. Do not join the ground planes; instead, connect the two with a moderate signal trace underneath the converter. For multiple converters, connect the two ground planes as close as possible to one central location for all of the converters. In some cases, experimentation may be required to find the best point to connect the two planes together.

Decoupling

Good decoupling practices must be used for the ADS1203 and for all components in the design. All decoupling capacitors, specifically the 0.1µF ceramic capacitors, must be placed as close as possible to the pin being decoupled. A 1µF and 10µF capacitor, in parallel with the 0.1µF ceramic capacitor, can be used to decouple V_{DD} to GND. At least one 0.1µF ceramic capacitor must be used to decouple V_{DD} to GND, as well as for the digital supply on each digital component.

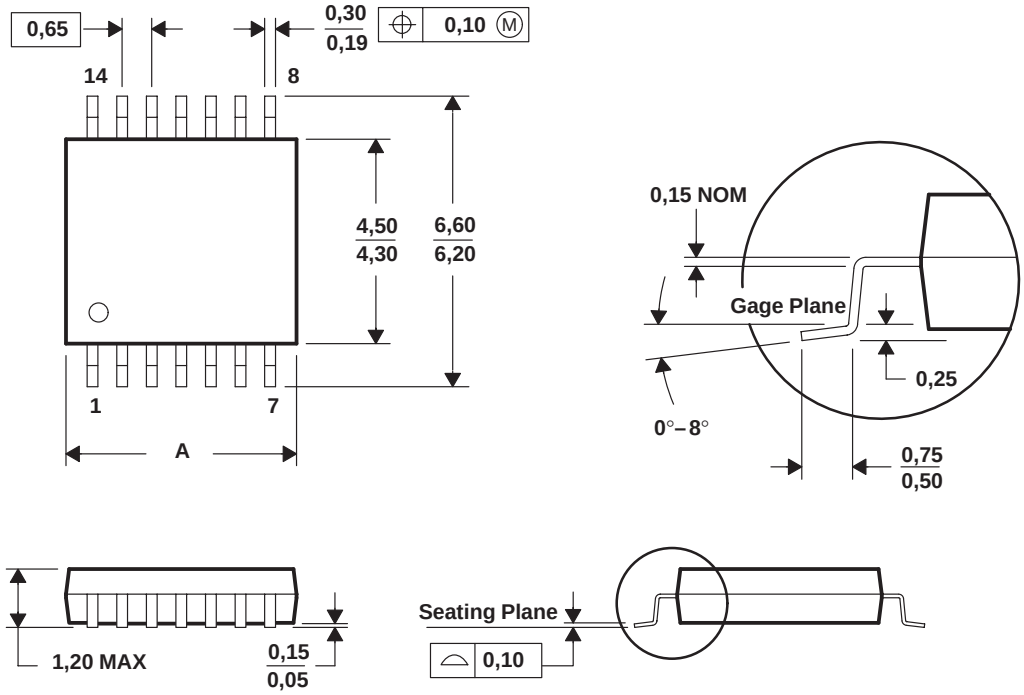
PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
ADS1203IPWR	ACTIVE	TSSOP	PW	8	2000
ADS1203IPWT	ACTIVE	TSSOP	PW	8	250

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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