AUK Semiconductor

SD42C/P1008

4Bit Single Chip Microcontroller

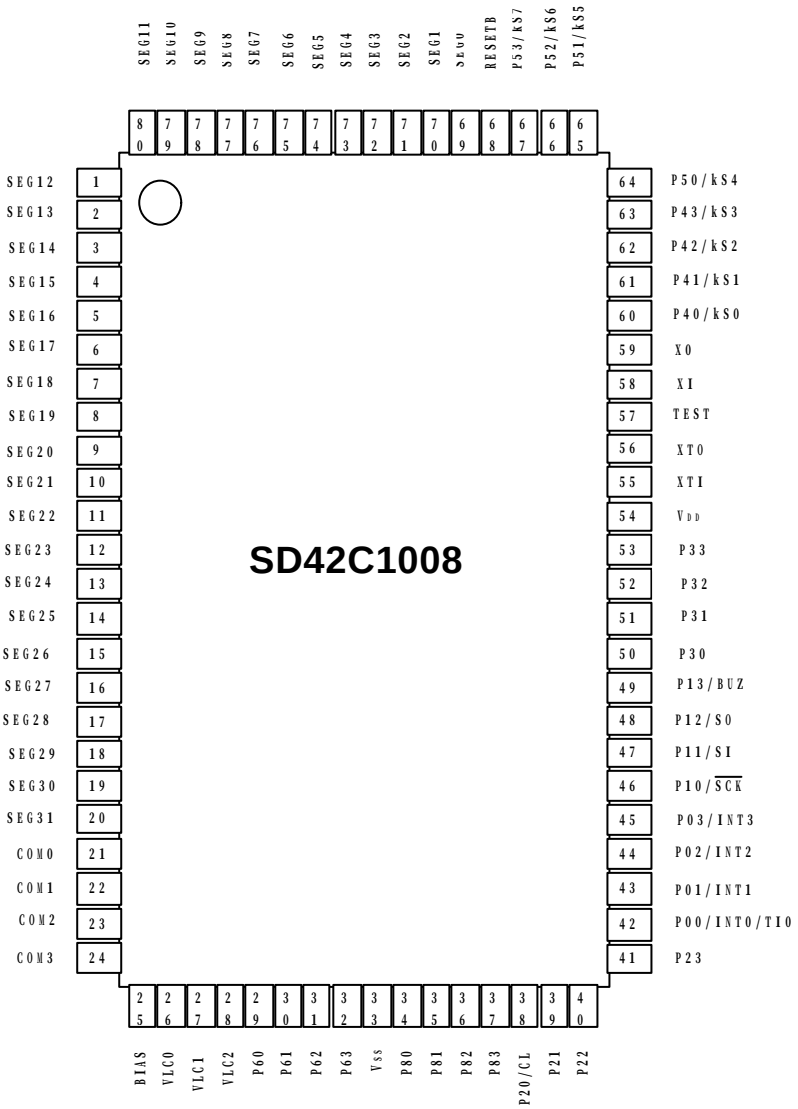
Description

The SD42C1008 is a microcomputer of the 4-bit single chip microcomputer SD42xx series which can match an 8-bit microcomputer in the data processing capability.
The SD42C1008 can handle 1-bit, 4-bit, and 8-bit data as well as operates at high speed (minimum instruction execution time : 0.95us) it contains a LCD pannel controller/driver.

Ordering Information

Type NO.	Marking	Package Code
SD42C1008	SD42C1008	QFP-80

Pin Configuration



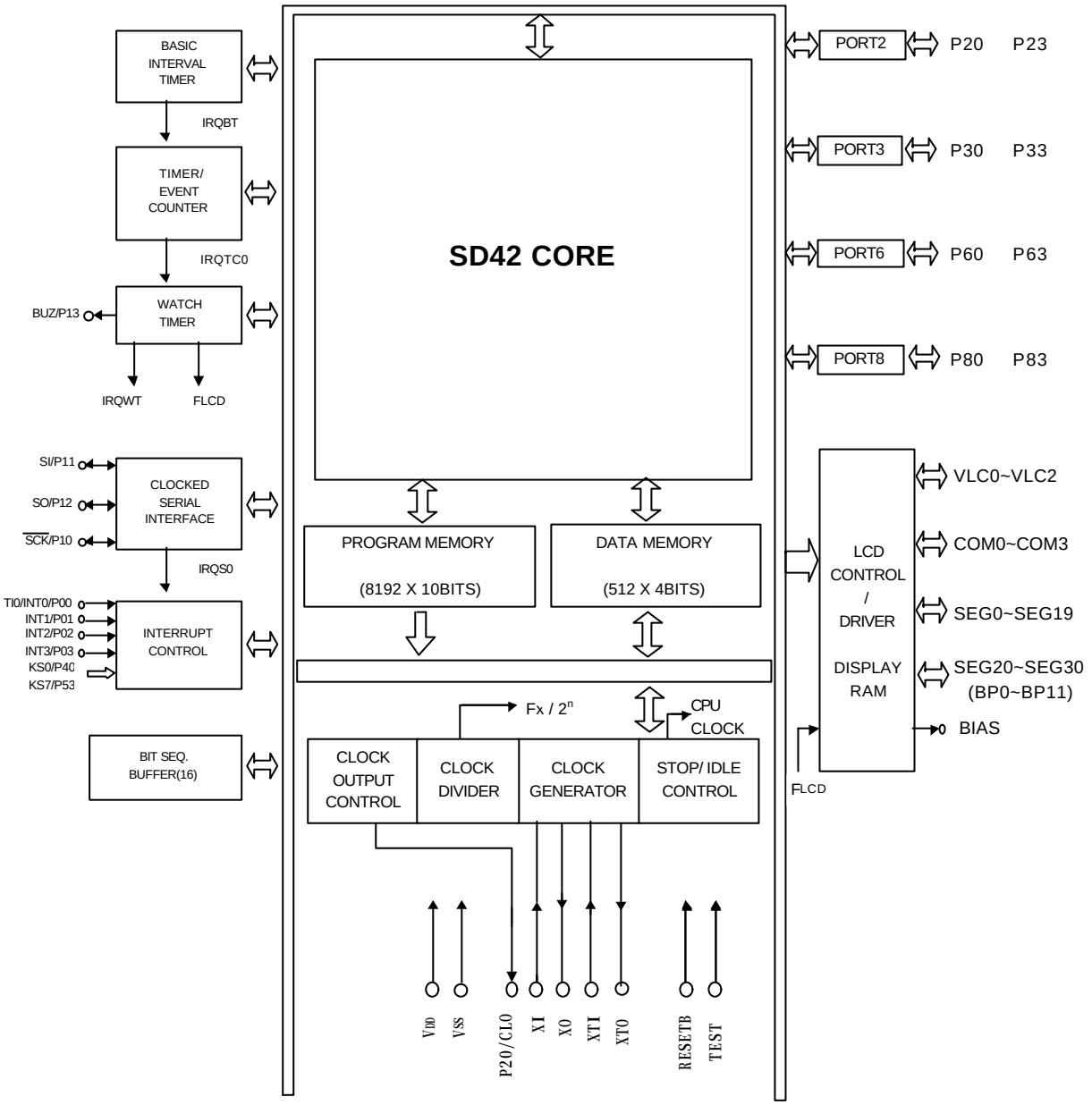
Features

- Memory mapped I/O
- Program memory : 8192 x 10bits
- Data memory : 512 x 4bits
- Instructions
  - Various bit manipulation
  - 8-bit data operation
  - 7-bit relative branch
  - 1 byte absolute call
- Instruction cycle times
  - Main (XI = 4.19MHz)
    . 15.3 us (XI/64 = 65.5KHz)
    . 1.91 us (XI/8 = 524.0KHz)
    . 0.95 us (XI/4 = 1.05MHz)
  - Sub (XTI = 32.768KHz)
    . 122 us (XTI/4 = 8.19KHz)
- 4 Register Bank
- General register : 8 x 4-bit respectively
- Accumulator
  - Bit Accumulator (CY), 4 bit Accumulator (A), 8 bit Accumulator (XA)
- Multiple vectored interrupt source
  - External interrupt : 4
  - Internal interrupt : 4
- Watch timer
  - fast mode : 3.91 msec
  - normal mode : 0.5 sec
  - buzzer output : 1, 2, 4 KHz
- Basic interval timer
  - 8 kinds of period
  - Used stabilization wait timer to wake up Stop mode
- One 8-bit timer / event counter
- 8-bit serial communication interface
  - External / Internal clock selection
  - Mode : Transmit · Receive
    Receive only
    Clock continuous
- LCD controller/driver
  - selectable number of segments ; 20/24/28/32 segment (4/8/12 lines can be specified as bit ports)
  - Display mode selection
    · Static
    · 1/2 duty (1/2 bias)
    · 1/3 duty (1/2 bias)
    · 1/3 duty (1/3 bias)
    · 1/4 duty (1/3 bias)
- Key scan
  - 4, 6, 8 Pins Selectable : Port 4, 5
  - Falling edge operation
- 64 I/O Pins
  - LCD driver output pins : 36
    . Segment ouput pins : 20
    . Segment CMOS output pins : 12
    . Common ounput pins : 4
  - CMOS input/output pins : 32
- Power saving mode
  - STOP : Main clock, CPU clock stop
  - STBY : Only CPU clock stop
    Main clock operation

APPLICATION

VTR, Camera, Rice Cooker, Telephone
Blood Pressure Gauge, CD Player

BLOCK DIAGRAM



Program Memory(ROM)

	CONTENTS
0000H	VECTOR ADDRESS AREA
001FH	
0020H	ZERO-PAGE CALL AREA
002FH	
0060H	**8K Byte**
1FFFH	

Vector Address

	Prioty	INTERRUPT SUORCE	
0000H	0	RESET	Reset Signal
0002H	1	IRQBT	Basic Interval Timer
0004H	2	IRQ0	External interrupt 0
0006H	3	IRQ1	External interrupt 1
0008H	4	IRQTC0	Timer Event Counter 0
000AH			
000CH	6	IRQ2	External interrupt 2
000EH			
0010H	8	IRQ3	External interrupt 3
0012H	9	IRQS0	Serial I/O 0
0014H			
0016H			
0018H	12	IRQWT	Watch Timer
001AH	13	IRQKS	Key Scan
001CH			
001EH	15	-	reserved

Data Memory(RAM)

		DIRECT	INDIRECT		STACK	GENERAL REGISTER	
		m	@HL		@DE @DL		
	$00 PAGE0 (256 Byte) $FF	MB=0	MB=0	MP=0		SPS=0	RB=0 RB=2 / RB=1 RB=4
BANK 0 (1K)	$00 PAGE1 (256 Byte) $FF			MP=1		SPS=1	
	$00 PAGE2 (256 Byte) $FF			MP=2		SPS=2	
	$00 PAGE3 (256 Byte) $FF	I/O MEMORY		MP=3			

; Usable

I/O Address Map

ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL
	b3	b2	b1	b0		1 bit	4 bit	8bit		VALUE
318H	Stack pointer low (SPL)				R/W			O	Stack pointer low	E
319H	Stack pointer high (SPH)				R/W			O	stack pointer high	F
31AH	SP3	SP2	SP1	SP0	R/W			O	Stack Page Select Low (SPSL)	0
31BH	-	-	SP5	SP4	R/W			O	Stack Page Select High (SPSh)	0
31CH	AC		IS1	IS0	R/W	O	O	O	Psw low (PSWL)	0
31DH	CY	Z	OV	T					Psw high (PSWH)	0
320H	T/E counter mode register 0				W	320H.3		O	Clock source select. counter	00
321H	(TMOD0)								start (ch0)	
322H	T/E counter register 0				R				readable count value (ch0)	00
323H	(TMCNT0)									
324H	T/E reference register 0				W				count reference register (ch0)	FF
325H	(TMREF0)									
332H	Basic Timer mode register(BMOD)				R/W	332H.3			clock select, Bit start	0
334H	Basic interval timer count				R				readable count register	00
335H	register(BITCNT)									
336H	Watch timer mode register				R/W	336H.3			clock/buzzer select. bit3	00
337H	(WMOD)								readable	
390H	Lcd display mode register				W			O	duty/bias/clock/seg/bitport	00
391H	(LCDMD)								select	
392H	Lcd control register (LCON)				W		O		display ON/OFF	0
3A0H	Power control register						O		system clock select, idle, stop	00
	(PCON)				R/W				mode	
3A2H	Operating mode register (SCMOD)				R/W	O			main/sub system clock select	0
3A4H	Clock output mode register				W		O		cpu clock output select, clock	00
	(CLOMD)								out EN/DIS	
3A8H	Serial interface mode register0				W	3A8H.3		O	receive/transmit mode. clock	00
3A9H	(SIOM0)								select	
3AAH	Serial interface buffer0				R/W				serial shift register 0	XX
3ABH	(SBUFF0)									
3B2H	Power on flag (PONF)				P/W	3B2H.0		O	power on reset flag	0
3C2H	IME				R/W	3C2H.3		O	Interrupt priorty select, IME flag.	00
3C3H	IPSR3	IPSR2	IPSR1	IPSR0						
3C4H	External interrupt mode register0				W		O		external interrupt 0 edge	00
	(IMOD0)								detection	
3C5H	External interrupt mode register1				W		O		external interrupt 1 edge	00
	(IMOD1)								detection	
3C6H	External interrupt mode register2				W		O		external interrupt 2 edge	00
	(IMOD2)								detection	
3C7H	External interrupt mode register3				W		O		external interrupt 3 edge	00
	(IMOD3)								detection	
3D8H	IE2	IRQ2	IEBT	IRQBT	R/W	O	O		Interrupt EN/IRQ flag	0
3D9H			IEWT	IRQWT	R/W	O	O		Interrupt EN/IRQ flag	0

ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL
	b3	b2	b1	b0		1 bit	4 bit	8bit		VALUE
3DAH	IEKSF	IRQKS	IES0	IRQS0	R/W	O	O		Interrupt EN/IRQ flag	0
3DBH			IETC0	IRQTC0	R/W	O	O		Interrupt EN/IRQ flag	0
3DCH	IE1	IRQ1	IE0	IRQ0	R/W	O	O		Interrupt EN/IRQ flag	0
3DDH			IE3	IRQ3	R/W	O	O		Interrupt EN/IRQ flag	0
3DEH					R/W	O	O		Interrupt EN/IRQ flag	0
3E0H	PW03	PW02	PW01	PW00	W			O	port 0, 1 mode register (PMGA)	00
3E1H	PW13	PW12	PW11	PW10						
3E2H	PW23	PW22	PW21	PW20	W			O	port 2, 3 mode register (PMGB)	00
3E3H	PW33	PW32	PW31	PW30						
3E4H	PW43	PW42	PW41	PW40	W			O	port 4, 5 mode register (PMGC)	00
3E5H	PW53	PW52	PW51	PW50						
3E6H	PW63	PW62	PW61	PW60	W			O	port 6, 7 mode register (PMGD)	00
3E7H	PW73	PW72	PW71	PW70						
3E8H	PW83	PW82	PW81	PW80	W			O	port 8, 9 mode register (PMGE)	00
3E9H	PW93	PW92	PW91	PW90						
3F0H	PORT0 (R0)				R/W	O	O		R0 Port Data Register	0
3F1H	PORT1 (R1)				R/W	O	O		R1 Port Data Register	0
3F2H	PORT2 (R2)				R/W	O	O		R2 Port Data Register	0
3F3H	PORT3 (R3)				R/W	O	O		R3 Port Data Register	0
3F4H	PORT4 (R4)				R/W	O	O	O	R4 Port Data Register	0
3F5H	PORT5 (R5)				R/W	O	O		R5 Port Data Register	0
3F6H	PORT6 (R6)				R/W	O	O		R6 Port Data Register	0
3F8H	PORT8 (R8)				R/W	O	O		R8 Port Data Register	0

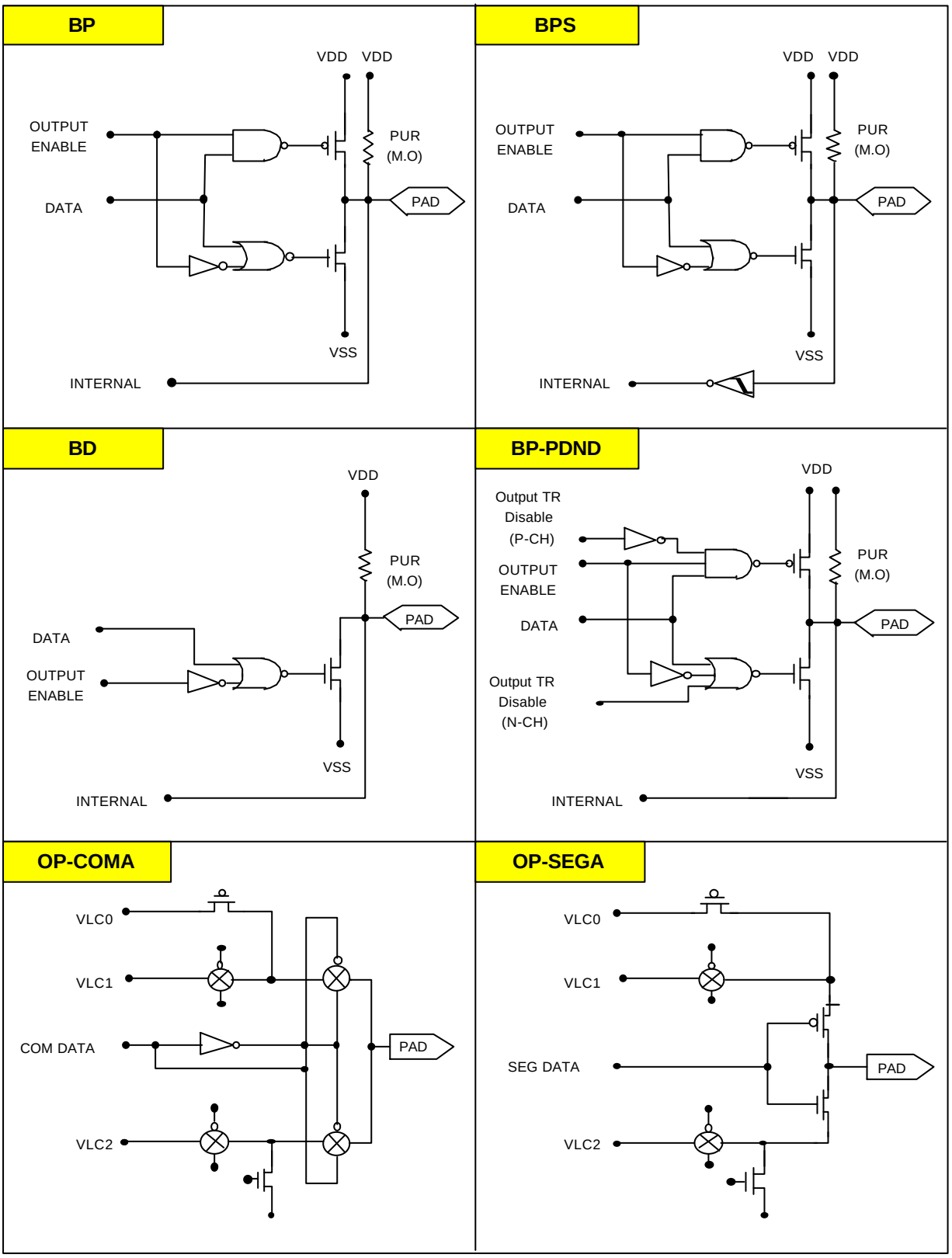
Pin Description

PIN SYMBOL	SHARED PIN	I/O	FUNCTION	RESET	PORT TYPE
P00	INT0/TI0	I/O	- Detection edge selectable - With noise elimination function	INPUT	BPS
P01 P02 P03	INT1 INT2 INT3	I/O	- Edge detection vectored interrupt input pin (detection edge selectable) - Event pulse input port for timer event counter	INPUT	BPS
P10 P11 P12 P13	$\overline{SCK}$ SI SO BUZ	I/O	- Serial clock I/O pin - Serial data input pin - Serial data output pin - Buzzer output pin	INPUT	BPS
P20 P21 P22 P23		I/O	- 4Bit I/O Port	INPUT	BP
P30 P31 P32 P33		I/O	- 4Bit I/O Port	INPUT	BP
P40 P41 P42 P43	KS0 KS1 KS2 KS3	I/O	- Falling edge detection keyscan input pin	INPUT	BD
P50 P51 P52 P53	KS4 KS5 KS6 KS7	I/O	- Falling edge detection keyscan input pin	INPUT	BD
P60 P61 P62 P63		I/O	- 4Bit I/O Pin	INPUT	BP-PDND
P80 P81 P82 P83		I/O	- 4Bit I/O Pin	INPUT	BP

Pin Description

PIN SYMBOL	SHARED PIN	I/O	FUNCTION		RESET	PORT TYPE
SEG0 ~ SEG19		O	- Segment signal output pin			OP-SEGB
SEG20 ~ SEG31	BP0 ~ 11	O	- 1 Bit output port (Bit Port) shared with a segment signal output pin			OP-SEGA
COM0 COM1 COM2 COM3		O	- Common signal output			OP-COMA
VLC0 VLC1 VLC2			- LCD drive power pin split register network (Mask Option)			VLC
BIAS			- LCD power supply bias control			VLC
XI XO		I O	- Main system clock input - Main system clock output			OSC1
XTI XTO		I O	- Sub system clock input - Sub system clock output			OSC2
RESETB		I	- System reset input pin			IP1
TEST		I	- Chip function test input pin	MASK ROM Version		IP2
				OTP ROM Version		BP

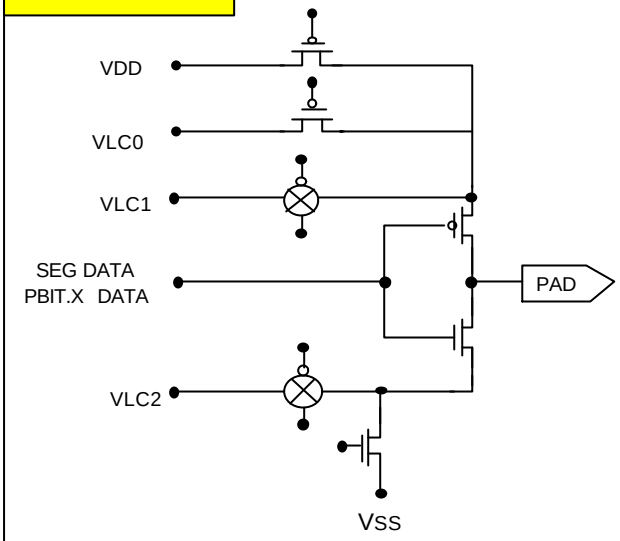
I/O Circuits



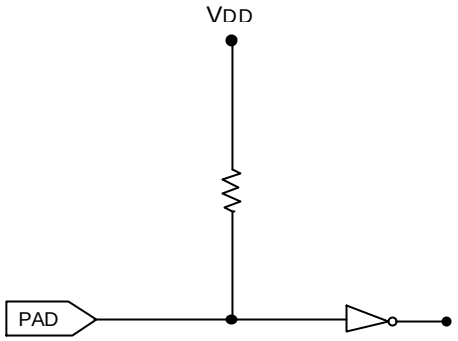
NOTE) PUR : Pull-Up Resistor

M.O : Mask Option

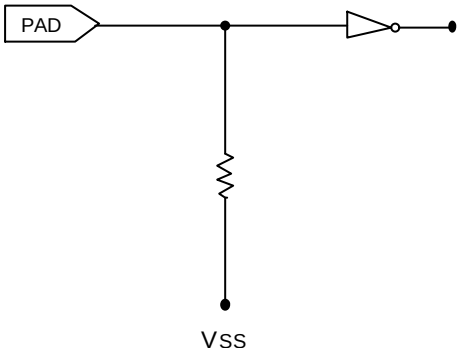
OP-SEGB



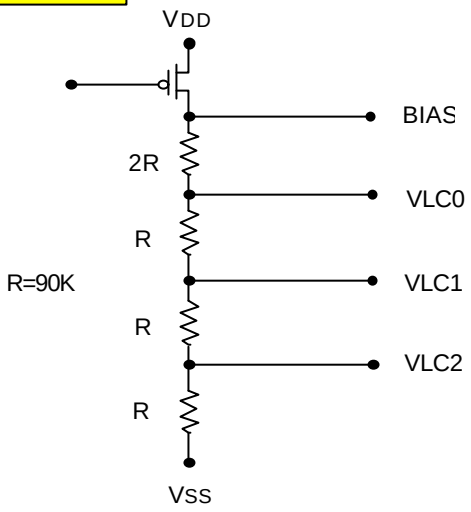
IP1



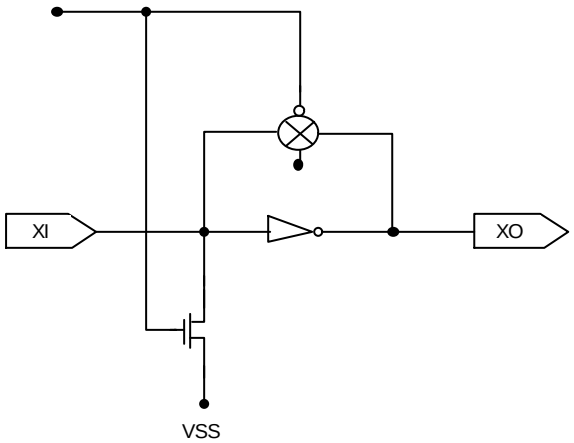
IP2



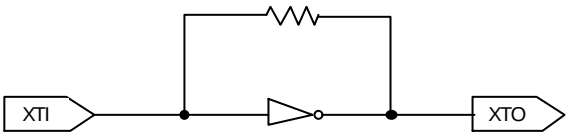
VLC



OSC1



OSC2



Absolute Maximum Ratings

(TA = 0℃ to 70℃, VDD = 5V ±10%, fx = 4.19MHz)

PARAMETER	SYMBOL	CONDITION	RATING		UNIT
Supply Voltage	V_{DD}	-	-0.3 to +7.0		V
Input Voltage	V_I	All I/O ports	-0.3 to V_{DD}+0.3		V
Output Voltage	V_O	-	-0.3 to V_{DD}+0.3		V
Output Current High	I_{OH}	One I/O port active	-15		mA
		All I/O ports active	-30		
Output Current Low	I_{OL}	One I/O port active	Peak Value	+30	mA
		-	RMS Value	+15	
		Total value for ports P1, P2, P3, P8	Peak Value	+100	
			RMS Value	+60	
		Total value for ports P0, P4, P5, P6	Peak Value	+100	
			RMS Value	+60	
Operating Temperature	T_A	-	-40 to +85		℃
Storage Temperature	T_{stg}	-	-55 to +125		℃

* RMS values are calculated as peak value x $\sqrt{Duty}$
* Exceeding beyond those listed values under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC Electrical Characteristics

(V_{SS} = 0, V_{DD} = 5V ±10%, T_A = 25°C, f_X = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION			LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT
High Level Input Voltage	V_{IH1}	Port 0,1 (Schmitt Input)			0.8 VDD	-	V_{DD}	V
	V_{IH2}	XI, XTI			VDD-0.5	-	V_{DD}	
	V_{IH3}	Port 2,3,4,5,6,8, RESETB, TEST			0.7 VDD	-	V_{DD}	
Low Level Input Voltage	V_{IL1}	Port 0,1 (Schmitt Input)			0	-	0.2 VDD	V
	V_{IL2}	XI, XTI			0	-	0.4	
	V_{IL3}	Port 2,3,4,5,6,8, RESETB, TEST			0	-	0.3 VDD	
High Level Output Voltage	V_{OH}	Port 0,1,2,3,6	(I_{OH} = - 5mA)		4.2	4.5	-	V
		Port 0,1,2,3,6	(I_{OH} = - 100uA)		4.6	4.9	-	
Low Level Output Voltage	V_{OL}	Port 4,5 (Open-Drain)	(I_{OL} = 10mA)		-	-	2	V
		Port 0,1,2,3,6	(I_{OL} = 10mA)		-	0.4	0.6	
		Port 0,1,2,3,6	(I_{OL} = 1mA)		-	0.1	0.3	
High Level Input Leakage Current	I_{IH}	Port 0,1,2,3,4,5,6,8 V_{PP} OEX, XTI, RESETB			-	1.2	3	uA
		XI			-	5	15	
Low Level Input Leakage Current	I_{IL}	Port 0,1,2,3,4,5,6,8 V_{PP} OEX, XTI, TEST			-	-1.2	-3	uA
		XI			-	-5	-15	
Supply Current	I_{DD1} (1)	Main Clock (XI) = 4.19MHz	Dynamic Mode	VDD = 5V ±10%	-	-	10	mA
			Idle Mode		-	-	5	

DC Electrical Characteristic

(VSS = 0, VDD = 5V ±10%, TA = 25℃, fx = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION			LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT
Supply Current	I_{DD2} (1)	Main Clock (XI) = 2MHz	Dynamic Mode	VDD = 3V ±10%	-	-	2	mA
			Idle Mode		-	-	1	
	I_{DD3} (2)	Sub Clock (XTI) = 32.768KHz	Dynamic Mode	VDD = 3V ±10%	-	-	1.5	
	I_{DD4} (2)		Idle Mode		-	-	15	uA
	I_{DD5}	Main Clock (XI) = 4.19MHz	Stop Mode	VDD = 5V ±10%	-	-	5	
					-	-	3	
Pull-up Resistor	R_{L1}	V_I = 0V, V_{DD} = 5V ±10% RESETB			20	-	60	Kohm
Pull-down Resistor	R_{L2}	V_I = 0V, V_{DD} = 5V ±10% TEST			10	-	30	

NOTES) :

(1) Data Include power consumption for subsystem clock oscillation.

(2) Main system clock oscillation stops and the subsystem clock is used.

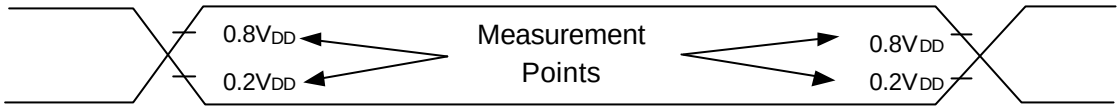
AC Electrical Characteristics

(TA = -40 o +85℃, VDD = 2.7 to 6.0V)

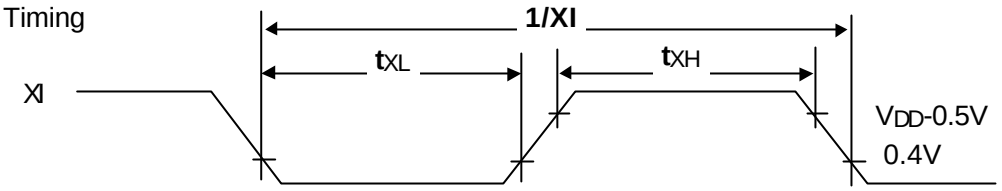
PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
Cycle Time	t_{CY}	Main system clock	V_{DD} = 4.5 to 6.0V		0.95	-	64	uS
			V_{DD} = 2.7 to 3.3V		3.8	-	64	uS
		Sub system clock			114	122	125	uS
TI0 Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0V			0	-	1	MHz
		V_{DD} = 2.7 to 3.3V			0	-	275	KHz
TI0 Input High, Low Level Width	t_{TIH}	V_{DD} = 4.5 to 6.0V			0.48	-	-	uS
	t_{TIL}	V_{DD} = 2.7 to 3.3V			1.8	-	-	uS
Interrupt Input High, Low Level Width		INT0			(1)	-	-	uS
	t_{INTH}	INT1, 2, 3			10	-	-	uS
	t_{INTL}	KS0 to KS7			10	-	-	uS
SCK Cycle Time	t_{KCY}	V_{DD} = 4.5 to 6.0V		Input	800	-	-	nS
				Output	1600	-	-	nS
		V_{DD} = 2.7 to 3.3V		Input	3200	-	-	nS
				Output	3800	-	-	nS
SCK High, Low Level Width	t_{KH}	V_{DD} = 4.5 to 6.0V		Input	400	-	-	nS
				Output	t_{KCY}/2~50	-	-	nS
	t_{KL}	V_{DD} = 2.7 to 3.3V		Input	1600	-	-	nS
				Output	t_{KCY}/2~150	-	-	nS
SI Set up Time to SCK High	t_{SIK}			Input	100	-	-	nS
				Output	150	-	-	nS
SI Hold Time to SCK High	t_{KSI}			Input	400	-	-	nS
				Output	400	-	-	nS
SCK to S0 Output Delay Time	t_{KSO}	V_{DD} = 4.5 to 6.0V		Input	-	-	300	nS
				Output	-	-	250	nS
		V_{DD} = 2.7 to 3.3V		Input	-	-	1000	nS
				Output	-	-	1000	nS
RESETB Low Level	t_{RSL}				10	-	-	uS

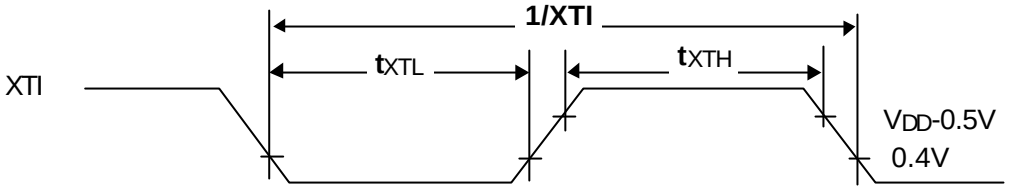
(1) 2tcy or 128/fx, depending on the setting of the interrupt mode register.

AC Timing Measurement Points (Except XI and XTI)

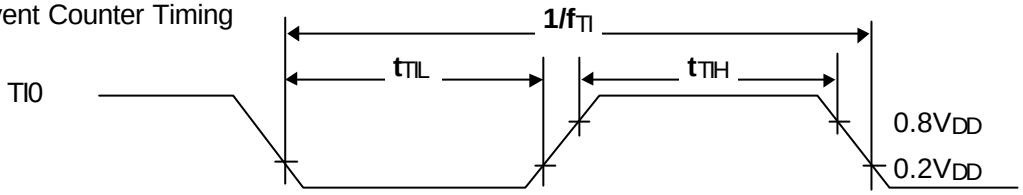


Clock Timing

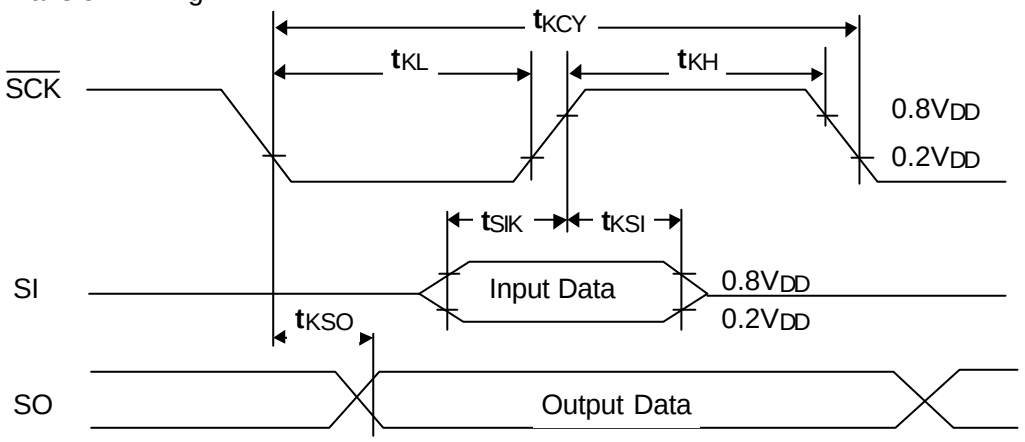




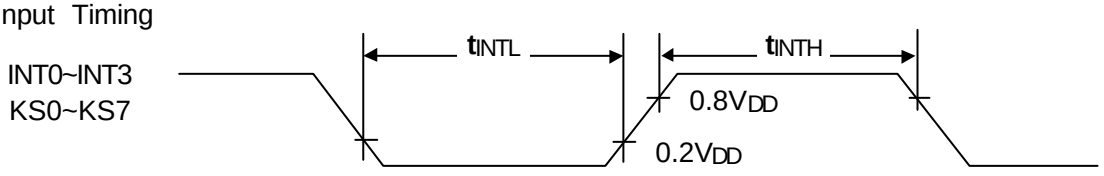
Timer Event Counter Timing



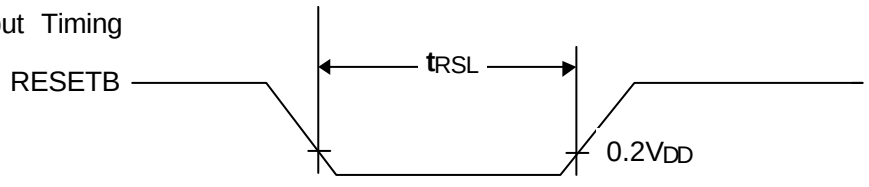
Serial Transfer Timing



Interrupt Input Timing



RESETB Input Timing



RAM Data Retention Characteristics (in STOP Mode)

(T_A = -40 to +85℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	V_{DDDR}		2.0	-	6.0	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 2.0V	-	0.1	10	uA
Release Signal Set Time	t_{SREL}		0	-	-	uS
Oscillation Stabilization Wait Time	t_{WAIT}	When released by RESETB	-	2^{17}/fx	-	mS
		When released by interrupt Signal	-	NOTE 1)	-	mS

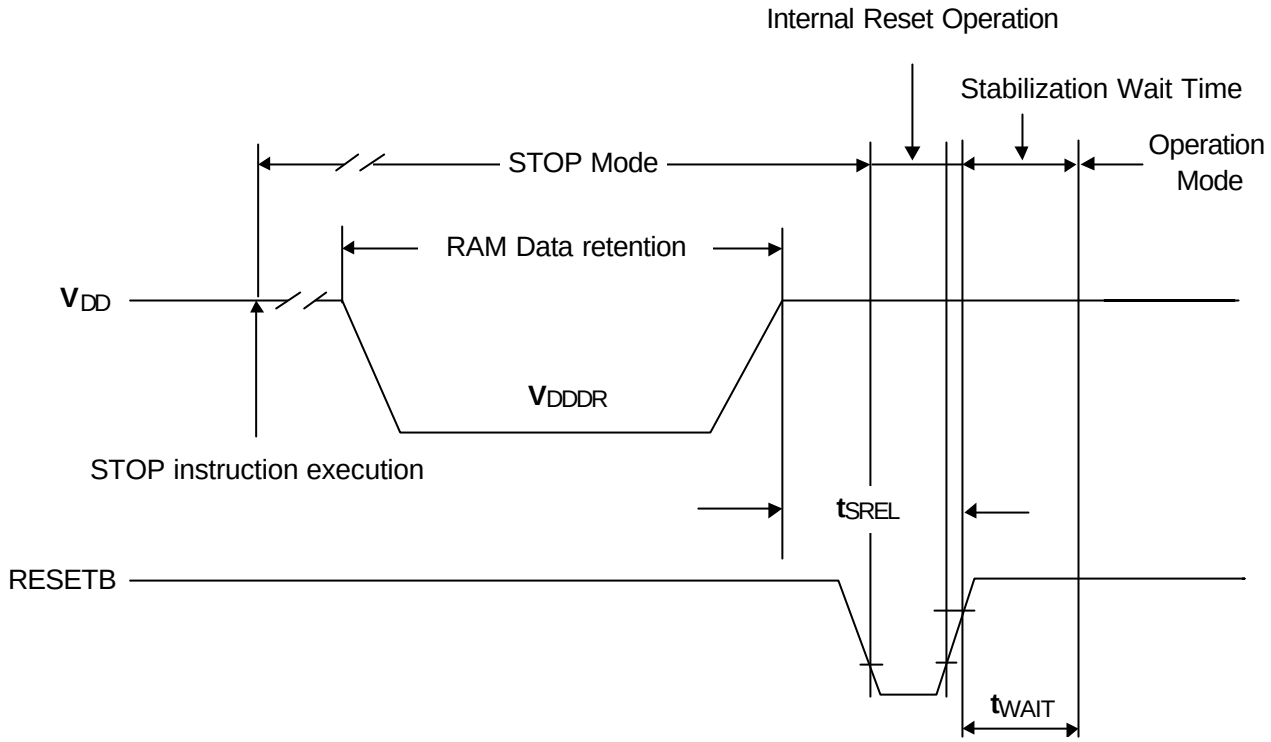
NOTE 1) Depends on the setting of the basic interval timer mode register.
(refer to the table below)

(fx = 4.19MHz)

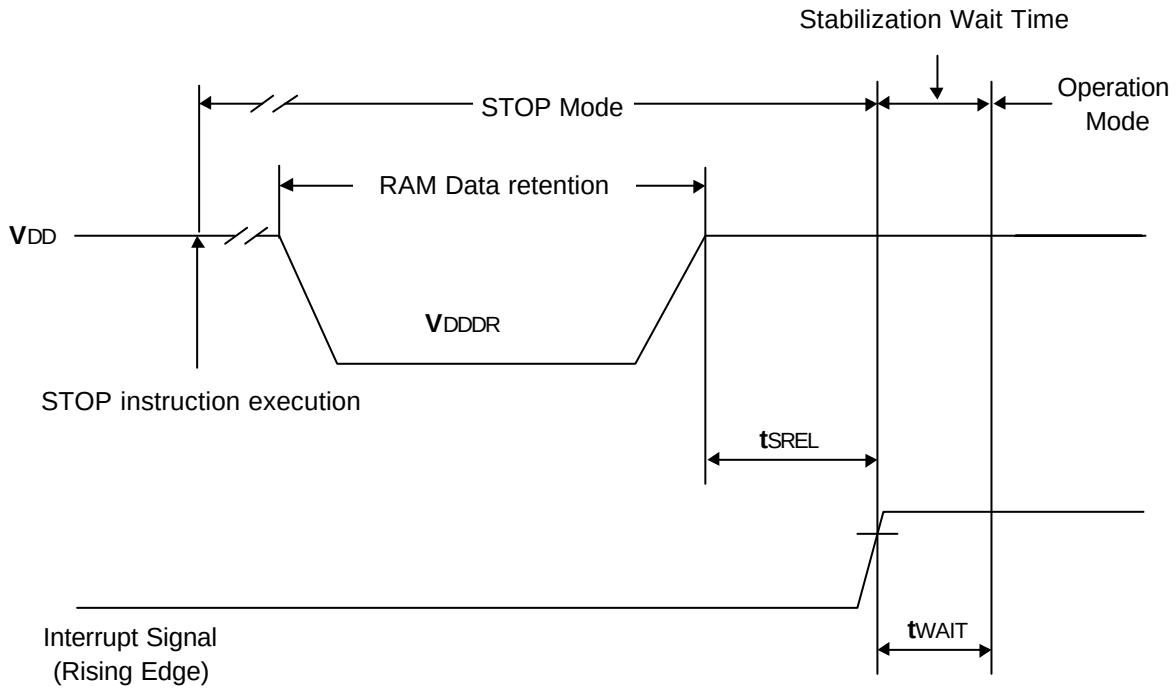
BMOD2	BMOD1	BMOD0	Oscillation Stabilization
0	0	0	2^{20}/fx (Approximately 250ms)
0	1	1	2^{17}/fx (Approximately 31.3ms)
1	0	0	2^{15}/fx (Approximately 7.82ms)
1	0	1	2^{13}/fx (Approximately 1.95ms)

RAM Data Retention Timing

When STOP mode is released by RESETB input



When STOP mode is released by interrupt signal



SD42P1008

Description

The SD42P1008 is a system evaluation LSI having a built in One-Time Programming circuit. A programming and verification for the internal EPROM is achieved by using a general EPROM programmer with an adapter socket.

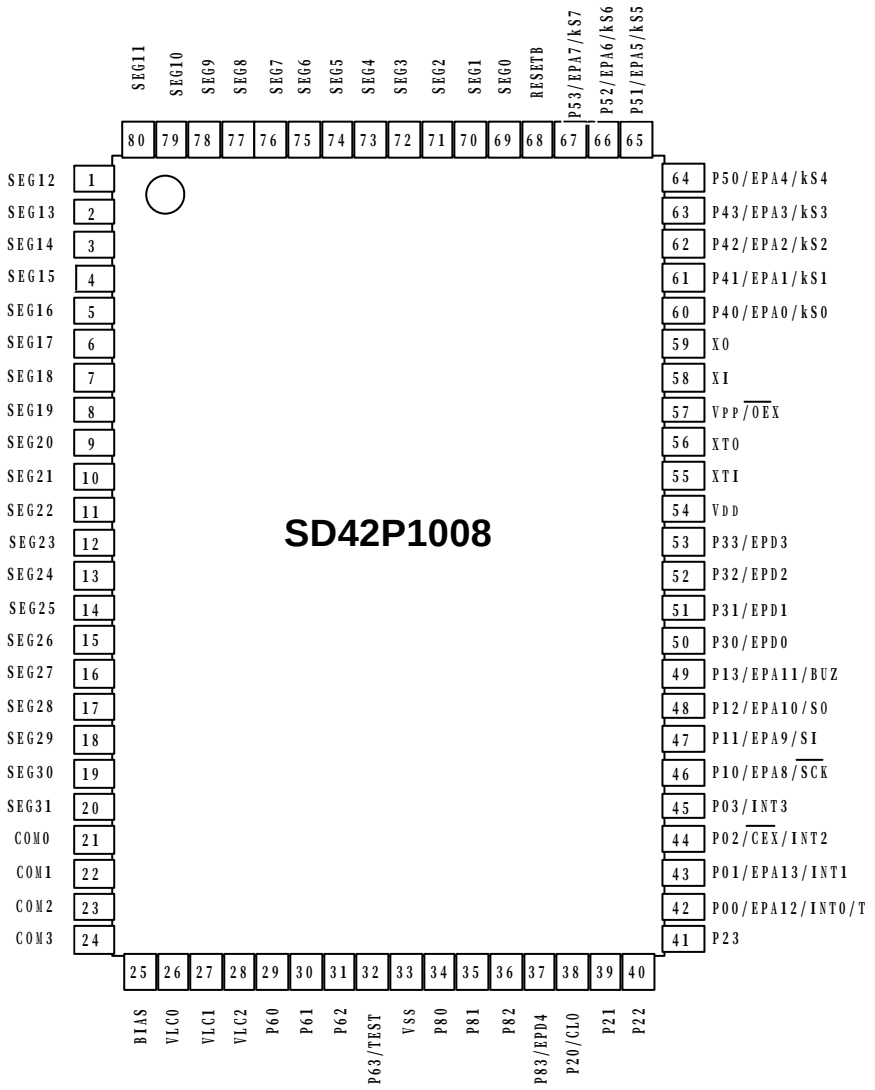
The function of this device is exactly same as the SD42C1008 with programming of the internal EPROM.

The SD42P1008 is the OTP version of the SD42C1008 with replacement of MASK ROM to EPROM as an internal ROM.

Ordering Information

Type NO.	Marking	Package Code
SD42P1008	SD42P1008	QFP-80

Pin Configuration



Device Operation

The operational modes of the SD42P1008 are listed in Table 1.

A single 5V power supply is required in the read mode.

All inputs are TTL levels except for VPP / $\overline{OEX}$.

V_{PP} = 12.5±0.5V

PINS / MODE	$\overline{CEX}$	V_{PP} / $\overline{OEX}$	V_{DD}	OUTPUT
READ	V_{IL}	V_{IL}	5.0V	D_{OUT}
PROGRAM	V_{IL}	V_{PP}	6.0V	D_{IN}
VERIFY	V_{IL}	V_{IL}	6.0V	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	6.0V	High Z

TABLE 1. Operating Modes

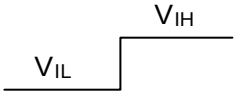
PIN NAME	MODE	
	EPROM MODE	USER MODE
TEST	V_{IL}	V_{IH}
RESETB	V_{IL}	

TABLE 2. The modes of SD42P1008

DC Programming Characteristics

PARAMETER	SYMBOL	TEST CONDITION	LIMIT		UNIT
			MIN.	MAX.	
Input Low Voltage	V_{IL}		-0.1	0.8	V
Input High Voltage	V_{IH}		2.0	V_{DD}	V
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	-	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = -400uA	2.4	-	V
Quick-pulse Programming	V_{PP}		12.5	13.0	V
Quick-pulse Programming	V_{DD}		6.0	6.5	V

Package Dimension

[UNIT : Millimeter]