βt121

Monolithic CMOS Triple 8-Bit VIDEODAC

The βt121 is a triple 8-bit VIDEODAC designed specifically for high-performance, high-resolution color graphics.

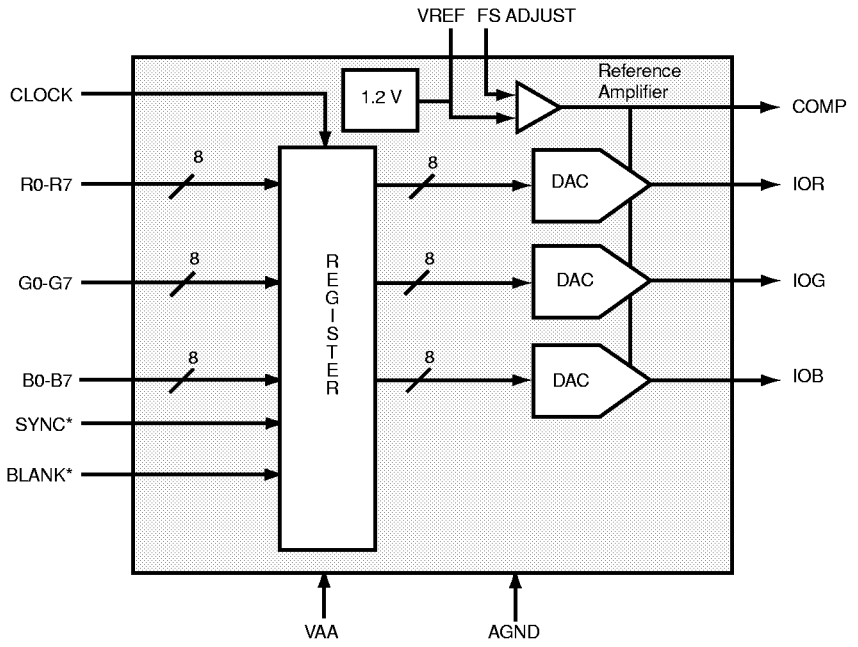
This device offers a higher level of integration than previous VIDEODAC designs. Included is an on-chip voltage reference to simplify use of the device.

The βt121 generates RS-343A-compatible video signals into a doubly-terminated 75 Ω load, and RS-170-compatible video signals into a singly-terminated 75 Ω load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

Product Features

- 80, 50 MHz Operation
- Triple 8-bit D/A Converters
- Optional Internal Voltage Reference
- RS-343A-Compatible Outputs
- TTL-Compatible Inputs
- +5 V CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 600 mW

Functional Block Diagram



Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Circuit Description

As illustrated in the functional block diagram, the Bt121 contains three 8-bit D/A converters, input registers, and a reference amplifier.

On the rising edge of CLOCK, 24 bits of color information (R0–R7, G0–G7, and B0–B7) are latched into the device and presented to the three 8-bit D/A converters.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as illustrated in Figure 1. Table 1 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt121 use a segmented architecture in which bit currents are routed to either the output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by use of identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt121 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

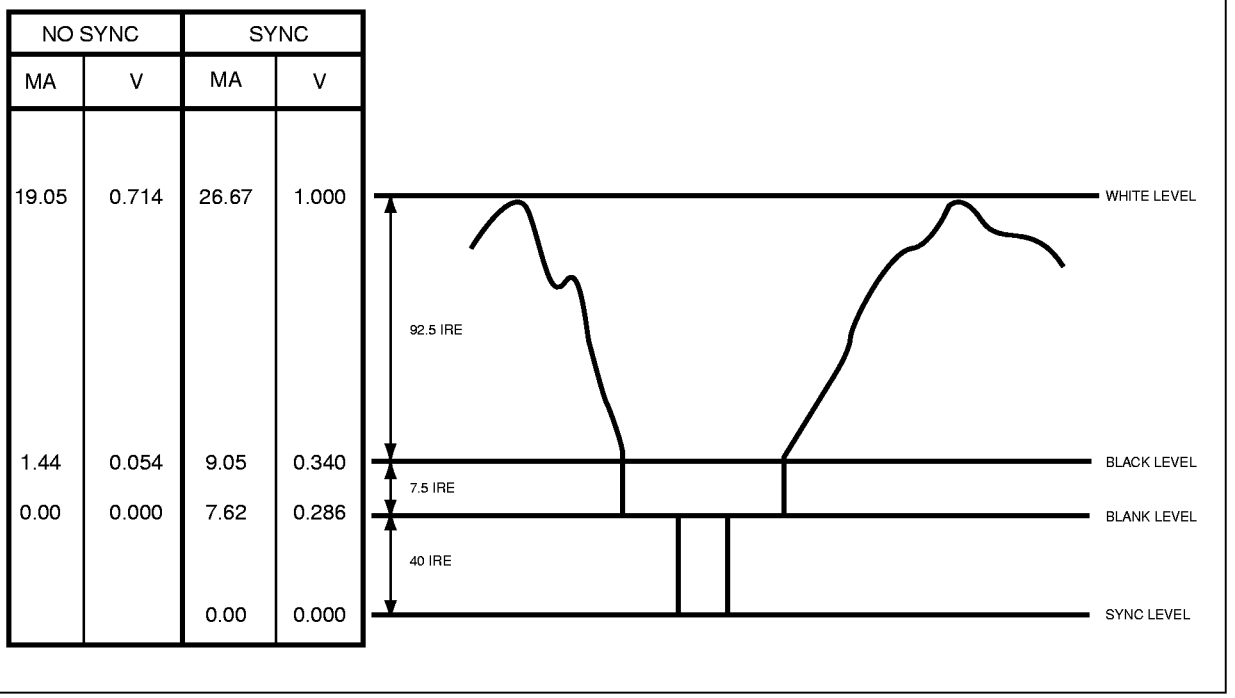
ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Figure 1. Composite Video Output Waveforms



Note: 75 Ω doubly-terminated load, RSET ~ 143 Ω, and VREF = 1.23 V. RS-343A levels and tolerances are assumed on all levels.

Table 1. Video Output Truth Table

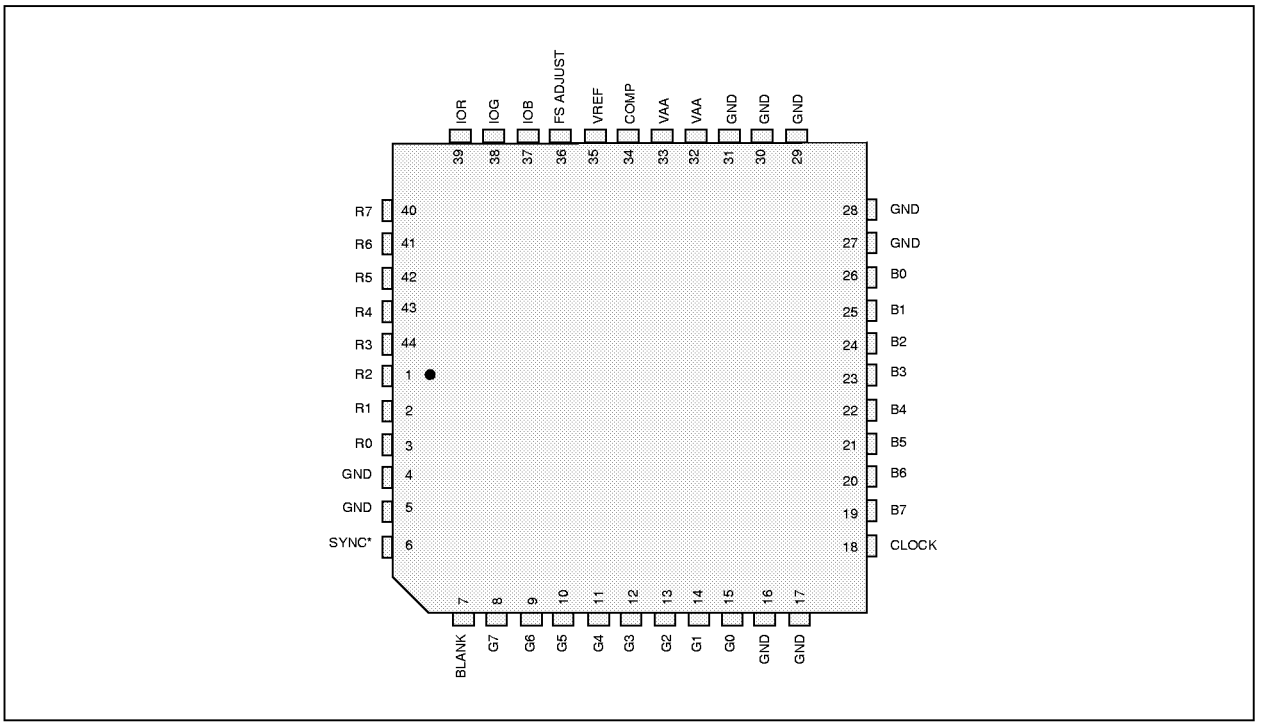
Description	Iout (mA)	SYNC	BLANK	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA-SYNC	data+1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK-SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75 Ω a doubly-terminated load, SETUP = 7.5 IRE. VREF = 1.23 V and RSET ~ 143 Ω.

Table 2. Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOR, IOG, and IOB outputs to the blanking level, as detailed in Table 1. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0–R7, G0–G7, and B0–B7 inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOR, IOG, IOB outputs (see Figure 1). SYNC* does not override any other control or data input, as shown in Table 1; therefore, SYNC* should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
R0–R7, G0–07, B0–B7	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least-significant data bits. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable (see Figure 3 and Figure 4 in the PC Board Layout Considerations section). All outputs, whether used or not, should have the same output load.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 1). The IRE relationships are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOR, IOG and IOB is: RSET (Ω) = K * VREF (V) /IO (mA) Where; K = 2,295 with SYNC*= 0 K = 3,195 with SYNC*= 1
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor in series with a resistor should be connected between this pin and the nearest VAA pin (Figure 3 and Figure 4) for optimum settling time. Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to the PC Board Layout Considerations section for critical layout criteria.
VREF	Voltage reference input. If an external voltage reference is used (Figure 4), it must supply this input with a 1.2 V (typical) reference. A 0.1 µF ceramic capacitor must always be used to decouple this input to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When the internal reference is used, this pin should not drive any external circuitry, except the decoupling capacitor (Figure 3).
GND	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.
VAA	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.

Figure 2. Pin Diagram



PC Board Considerations

The layout should be optimized for lowest noise on the Bt121 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated VIDEODAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt121 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt121 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3 and Figure 4. This bead should be located within 3 inches of the Bt121. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the VAA pins to GND. For operations above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figure 3 and Figure 4 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

To optimize the settling time of the Bt121, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 15 Ω however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time. An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

The COMP pin and series resistor must also be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. The COMP capacitor must be as close as physically possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Use of short, wide traces will also minimize lead inductance.

To reduce low-frequency supply noise a larger COMP capacitor value may be required.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Digital Signal Interconnect

The digital inputs to the Bt121 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt121 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the VIDEODAC. A parallel termination of 220 Ω to VCC and 330 Ω to the ground will provide a Thevenin equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

Analog Signal Interconnect

The Bt121 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt121 to minimize reflections. Unused analog outputs should be connected to GND.

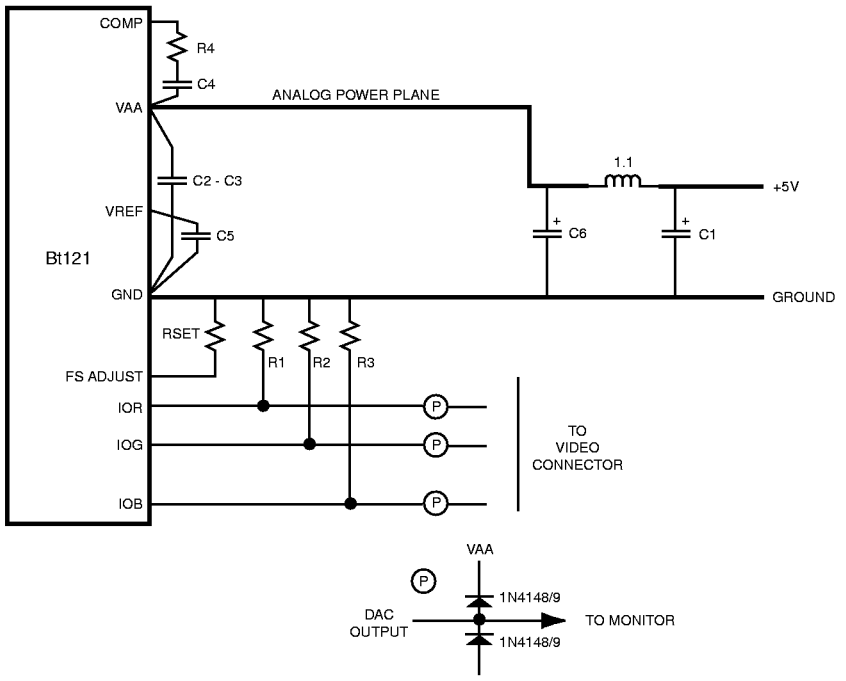
Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt121 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figure 3 and Figure 4 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

Figure 3. Typical Connection Diagram (Internal Reference)



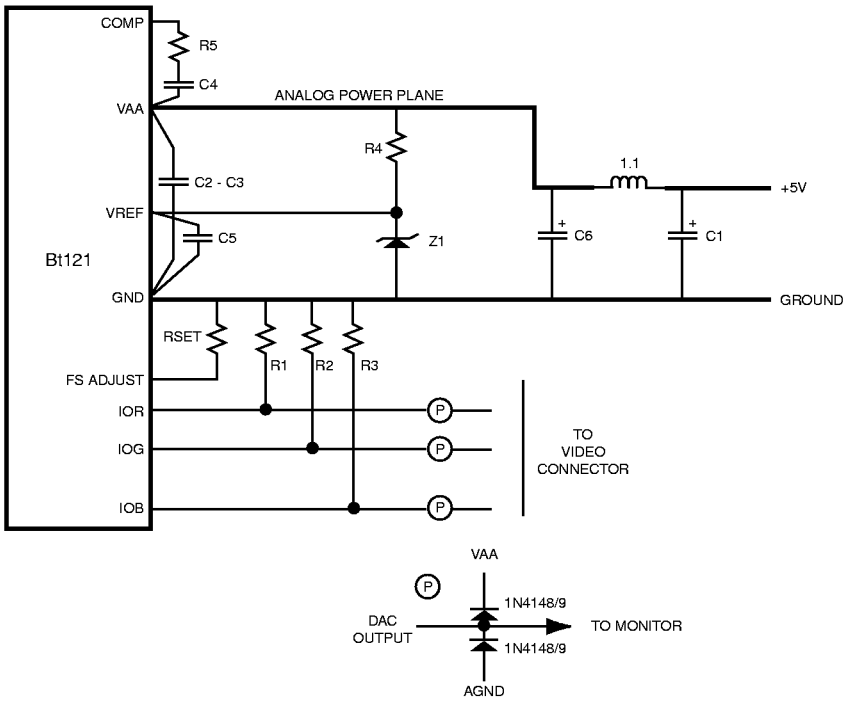
Note: Each set of VAA and GND pins must be separately decoupled.

Table 3. Typical Connection Parts List (Internal Reference)

Location	Description	Vendor Part Number
C1	33 µF tantalum capacitor	Mallory CSR13F336KM
C2, C3, C4, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	15 Ω 1% metal film resistor	Dale CMF-55C
RSET	143 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt121.

Figure 4. Typical Connection Diagram (External Reference)



Note: Each set of VAA and GND pins must be separately decoupled.

Table 4. Typical Connection Parts List (External Reference)

Location	Description	Vendor Part Number
C1	33 µF tantalum capacitor	Mallory CSR13F336KM
C2, C3, C4, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	
R5	15 Ω 1% metal film resistor	Dale CMF-55C
RSET	143 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt121.

Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply 80,66 MHz Parts 50, 35 MHz Parts	VAA	 4.75 4.5	 5.00 5.00	 5.25 5.5	 V V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
External Reference Voltage	VREF	1.11	1.235	1.36	V
FS ADJUST Resistor	RSET		143		Ω

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on Any Signal Pin[1]		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature Storage Temperature Junction Temperature	TA TS TJ	-55 -65		+125 +150 +150	°C °C °C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Notes: (1) This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the absolute maximum ratings (especially relative to VAA or between VAA pins) can induce destructive latchup.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error					
External Reference				±5	%Gray Scale
Internal Reference				±10	%Gray Scale
Monotonicity					
Coding			guaranteed		Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA +0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current	IIH			1	µA
Input Low Current	IIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Output					
Output High Voltage (IOH = —400 pA)	VOH	2.4			V
Output Low Voltage (IOL = 400 pA)	VOL			0.4	V
Output Capacitance	CDOUT			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Sync Level on IOR, IOG, IOB		6.29	7.62	7.94	mA
LSB Size			69.72		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	-0.5		+1.4	V
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT =0 mA)	COUT		30		pF
Internal VREF Voltage Range	INTVREF	1.08	1.2	1.32	V
Internal VREF Output Current	IVREF			10	µA
Power Supply Rejection Ratio[1] (COMP=0.01 µf, f=1 kHz)	PSRR		0.2	0.5	% / % ΔVAA

Notes: (1) Guaranteed by characterization, not tested.

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, RSET = 143 (1, and VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

When the internal voltage reference is being used, RSET may require adjustment to meet these limits.

Table 8. AC Characteristics

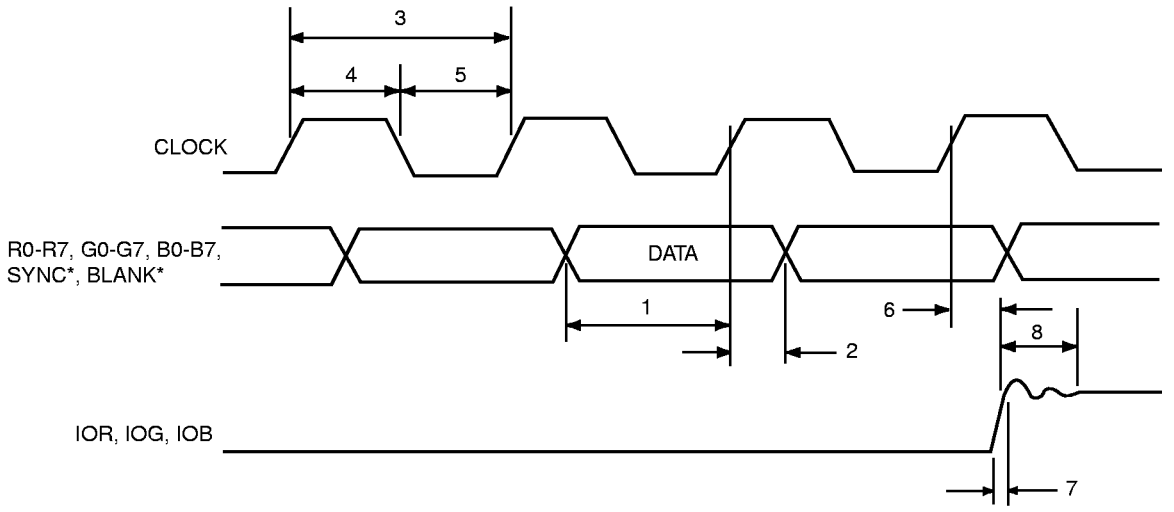
		80 MHz Devices			50 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Clock Rate	Fmax			80			50	MHz
Data and Control Setup Time	1	3			3			ns
Data and Control Hold Time	2	3			3			ns
Clock Cycle Time	3	12.5			20			ns
Clock Pulse Width High Time	4	4			7			ns
Clock Pulse Width Low Time	5	4			7			ns
Analog Output Delay	6			30			30	ns
Analog Output Rise/Fall Time	7		3			3		ns
Analog Output Settling Time	8		12.5			15.5		ns
Clock and Data Feedthrough[1]			-30			-30		dB
Glitch Impulse			75			75		pV - sec
DAC-to-DAC Crosstalk			-23			-23		dB
Analog Output Skew			0	3		0	3	ns
Pipeline Delay		2	2	2	2	2	2	Clock
VAA Supply Current[2]	IAA		95	110		95	110	mA

Notes: (1) Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2x clock rate.

(2) At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

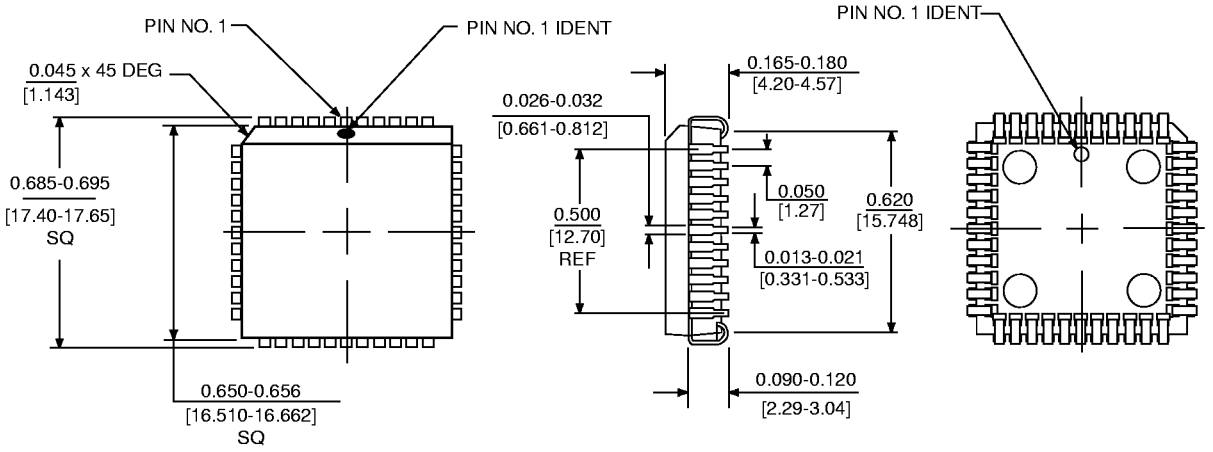
Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 143 Ω and VREF = 1.235 V. TTL input values are 0–3 V with input rise/fall times ≤4 ns, measured between the 10-percent and 90-percent points. Timing reference points at 50 percent for inputs and outputs. Analog output load ≤10 pF and SENSE* output load ≤50 pF. See timing notes in Figure 5. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Figure 5. Input/Output Timing



Notes:
1. Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.
2. Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.
3. Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Figure 6. Package Drawing – 44-Pin Plastic J-Lead (PLCC)



Note: Unless otherwise specified:
1. Dimensions are in inches [millimeters]
2. Tolerances are: .xxx ±0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt121KPJ80	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt121KPJ50	50 MHz	44-pin Plastic J-Lead	0° to +70° C

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