Low Power 14-Bit, 400ksps Sampling ADC Converter with Serial I/O

January 1999

FEATURES

- **Single Supply 5V or ±5V Operation**
- **Sample Rate: 400ksps**
- **±1.25LSB INL and ±1LSB DNL Max**
- **Power Dissipation: 20mW (Typ)**
- **Serial Data Output**
- No Missing Codes Over Temperature
- Power Shutdown: Nap and Sleep
- External or Internal Reference
- Differential High Impedance Analog Input
- Input Range: 0V to 4.096V or ±2.048V
- 82dB S/(N + D) and 95dB THD at Nyquist
- 16-Pin Narrow SSOP Package

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing
- Isolated Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Instrumentation

DESCRIPTION

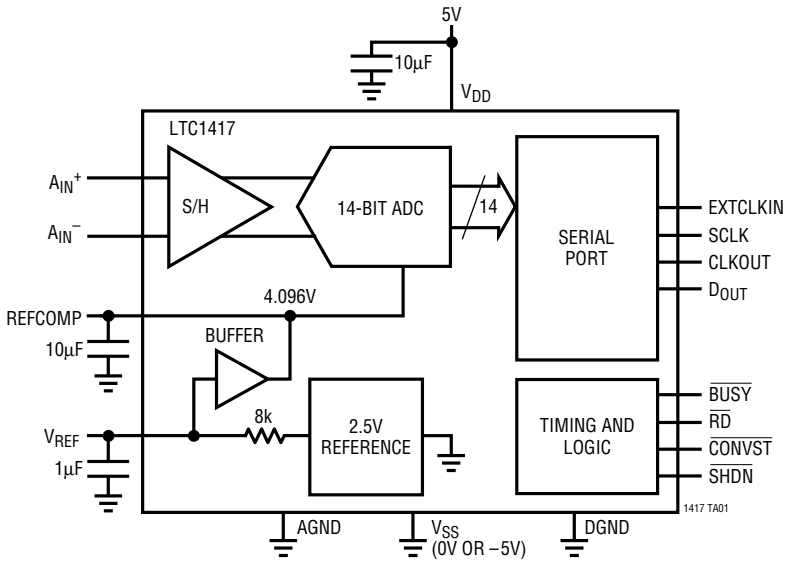
The LTC®1417 is a low power, 400ksps, 14-bit A/D converter. This versatile device can operate from a single 5V or ±5V supplies. An onboard high performance sample-and-hold, a precision reference and internal trimming minimize external circuitry requirements. The low 20mW power dissipation is made even more attractive with two user-selectable power shutdown modes.

The LTC1417 converts 0V to 4.096V unipolar inputs from a single 5V supply and ±2.048V bipolar inputs from ±5V supplies. DC specs include ± 1.25LSB INL, ±1LSB DNL and no missing codes over temperature. Outstanding AC performance includes 82dB S/(N + D) and 95dB THD at the Nyquist input frequency of 200kHz.

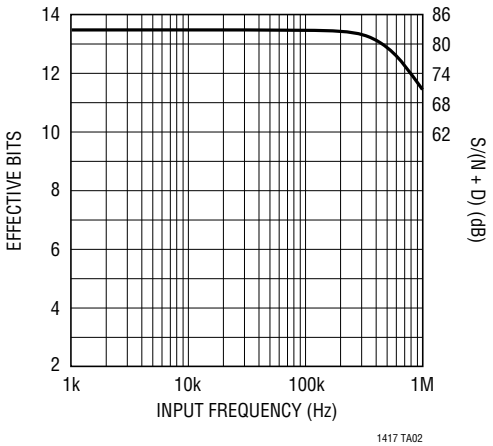
The internal clock is trimmed for 2µs maximum conversion time. The clock automatically synchronizes to each sample command, eliminating problems with asynchronous clock noise found in competitive devices. A separate convert start input and a data ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

400kHz, 14-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

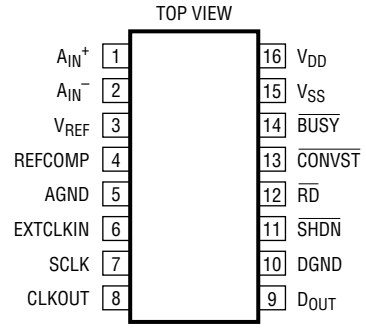


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS})
  Bipolar Operation Only ..... –6V to GND
Total Supply Voltage (V_{DD} to V_{SS})
  Bipolar Operation Only 12V
Analog Input Voltage (Note 3)
  Unipolar Operation .....–0.3V to (V_{DD} + 0.3V)
  Bipolar Operation..... (V_{SS} – 0.3) to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4)
  Unipolar Operation ..... –0.3V to 10V
  Bipolar Operation.....(V_{SS} – 0.3V) to 10V
Digital Output Voltage
  Unipolar Operation ..... –0.3 to (V_{DD} + 0.3V)
  Bipolar Operation.....(V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Power Dissipation..... 500mW
Operating Temperature Range
  LTC1417C..... 0°C to 70°C
  LTC1417I..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD (NARROW) PLASTIC SSOP

T_{JMAX} = 110°C, θ_{JA} = 95°C/W

ORDER PART NUMBER	GN PART MARKING
LTC1417ACGN LTC1417CGN LTC1417AIGN LTC1417IGN	1417A 1417 1417AI 1417I

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1417 MIN	LTC1417 TYP	LTC1417 MAX	LTC1417A MIN	LTC1417A TYP	LTC1417A MAX	UNITS
Resolution (No Missing Codes)		●	13			14			Bits
Integral Linearity Error	(Note 7)	●		±0.8	±2		±0.5	±1.25	LSB
Differential Linearity Error		●		±0.7	±1.5		±0.35	±1	LSB
Offset Error	External Reference (Note 8)	●		±5	±20		±2	±10	LSB
Full-Scale Error	Internal Reference			±10	±60		±20	±60	LSB
	External Reference = 2.5V			±5	±30		±5	±15	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0, Internal Reference, Commercial			±15			±10		ppm/°C
	$I_{OUT(REF)}$ = 0, Internal Reference, Industrial						±20		ppm/°C
	$I_{OUT(REF)}$ = 0, External Reference			±5			±1		ppm/°C

ANALOG INPUT

(Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V (Unipolar)	●		0 to 4.096		V
		4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –4.75V (Bipolar)	●		±2.048		V
I_{IN}	Analog Input Leakage Current	$\overline{CONVST}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode)			14		pF
		During Conversions (Hold Mode)			3		pF

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ACQ}	Sample-and-Hold Acquisition Time		●		150	500	ns
t_{AP}	Sample-and-Hold Aperture Time				–1.5		ns
t_{jitter}	Sample-and-Hold Aperture Time Jitter				5		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	$0V < (A_{IN}^+ = A_{IN}^-) < 4.096V$ (Unipolar) $-2.048V < (A_{IN}^+ = A_{IN}^-) < 2.048V$ (Bipolar)			65 65		dB dB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	100kHz Input Signal 200kHz Input Signal	●	79	82 82		dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, First Five Harmonics 200kHz Input Signal, First Five Harmonics	●	–85	–95 –95		dB dB
SFDR	Spurious Noise Dynamic Range	200kHz Input Signal	●		95		dB
IMD	Intermodulation Distortion	f_{IN1} = 90kHz, f_{IN2} = 100kHz			–90		dB
	Full Power Bandwidth				10		MHz
	Full Linear Bandwidth	S/(N + D) ≥ 77dB			0.8		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0, Commercial I_{OUT} = 0, Industrial			±10 ±20		ppm/°C ppm/°C
V_{REF} Line Regulation	$4.75V \le V_{DD} \le 5.25V$ $-5.25V \le V_{SS} \le -4.75V$			0.05 0.05		LSB/V LSB/V
V_{REF} Output Resistance	$0.1mA \le \lvert I_{OUT} \rvert \le 0.1mA$			8		kΩ

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				1.4		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V, I_O = –10µA V_{DD} = 4.75V, I_O = –200µA	 ●	 4.0	4.74		V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V, I_O = 160µA V_{DD} = 4.75V, I_O = –1.6mA	 ●		0.05 0.10	 0.4	V V
I_{OZ}	High-Z Output Leakage D_{OUT}, CLKOUT	V_{OUT} = 0V to V_{DD}, $\overline{RD}$ High	●			±10	µA
C_{OZ}	High-Z Output Capacitance D_{OUT}, CLKOUT	$\overline{RD}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage (Notes 10, 11)			4.75		5.25	V
V_{SS}	Negative Supply Voltage (Note 10)	Bipolar Only (V_{SS} = 0V for Unipolar)		–4.75		–5.25	V
I_{DD}	Positive Supply Current	Unipolar, $\overline{RD}$ High (Note 5)	●		4.0	5.5	mA
		Bipolar, $\overline{RD}$ High (Note 5)	●		4.3	6.0	mA
	Nap Mode	$\overline{SHDN}$ = 0V, $\overline{RD}$ = 0V			750		µA
	Sleep Mode	SHDN = 0V, $\overline{RD}$ = 5V			0.1		µA
I_{SS}	Negative Supply Current	Bipolar, $\overline{RD}$ High (Note 5)	●		2.0	2.8	mA
	Nap Mode	$\overline{SHDN}$ = 0V, $\overline{RD}$ = 0V			0.7		µA
	Sleep Mode	$\overline{SHDN}$ = 0V, $\overline{RD}$ = 5V			1.5		nA
P_{DIS}	Power Dissipation	Unipolar	●		20.0	27.5	mW
		Bipolar	●		31.5	44	mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	400			kHz
t_{CONV}	Conversion Time		●		1.8	2.25	µs
t_{ACQ}	Acquisition Time		●		150	500	ns
$t_{ACQ} + t_{CONV}$	Acquisition Plus Conversion Time		●		2.1	2.5	µs
t_1	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time from Nap Mode	(Note 10)			500		ns
t_2	$\overline{CONVST}$ Low Time	(Notes 10, 11)	●	40			ns
t_3	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF	●		35	70	ns
t_4	Data Ready Before $\overline{BUSY}\uparrow$	C_L = 25pF	●	7	12		ns
t_5	Delay Between Conversions	(Note 10)	●	250			ns
t_6	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$		●	–5			ns
t_7	Data Access Time After $\overline{RD}\downarrow$	C_L = 25pF			15	30	ns
			●			40	ns
		C_L = 100pF			20	40	ns
			●			55	ns
t_8	Bus Relinquish Time		●			35	ns
t_9	$\overline{RD}$ Low Time		●	t_7			ns
t_{10}	$\overline{CONVST}$ High Time		●	40			ns
t_{11}	Delay Time, SCLK↓ to D_{OUT} Valid	C_L = 25pF	●		15	40	ns
t_{12}	Time from Previous Data Remain Valid After SCLK↓	C_L = 25pF	●	5	10		ns
f_{SCLK}	Shift Clock Frequency		●	0		20	MHz
$f_{EXTCLKIN}$	External Conversion Clock Frequency		●	0.05		9	MHz
$t_{dEXTCLKIN}$	Delay Time, $\overline{CONVST}\downarrow$ to External Conversion Clock Input	(Note 9)	●			20	µs

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{H\ SCLK}$	SCLK High Time		●	40			ns
$t_{L\ SCLK}$	SCLK Low Time		●	40			ns
$t_{H\ EXTCLKIN}$	EXTCLKIN High Time		●	0.04		20	µs
$t_{L\ EXTCLKIN}$	EXTCLKIN Low Time		●	0.04		20	µs

The ● indicates specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA without latchup if the pin is driven below V_{SS} (ground for unipolar mode) or above V_{DD}.

Note 4: When these pin voltages are taken below V_{SS} they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, V_{SS} = –5V, f_{SAMPLE} = 400kHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended A_{IN}^+ input with A_{IN}^- grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

Note 11: The falling $\overline{CONVST}$ edge starts a conversion. If $\overline{CONVST}$ returns high at a critical point during the conversion it can create small errors. For best results ensure that $\overline{CONVST}$ returns high either within 625ns after conversion start or after $\overline{BUSY}$ rises.

PIN FUNCTIONS

A_{IN}^+ (Pin 1): Positive Analog Input.

A_{IN}^- (Pin 2): Negative Analog Input.

V_{REF} (Pin 3): 2.50V Reference Output. Bypass to AGND with 1µF.

REFCOMP (Pin 4): 4.096V Reference Output. Bypass to AGND using 10µF tantalum in parallel with 0.1µF ceramic.

AGND (Pin 5): Analog Ground.

EXTCLKIN (Pin 6): External Conversion Clock Input. A 5V input will enable the internal conversion clock.

SCLK (Pin 7): Data Clock Input.

CLKOUT (Pin 8): Conversion Clock Output.

D_{OUT} (Pin 9): Serial Data Output.

DGND (Pin 10): Digital Ground.

$\overline{SHDN}$ (Pin 11): Power Shutdown Input. Low selects shutdown. Shutdown mode selected by $\overline{RD}$. $\overline{RD}$ = 0 for nap mode and $\overline{RD}$ = 1 for sleep mode.

$\overline{RD}$ (Pin 22): Read Input. This enables the output drivers. $\overline{RD}$ also sets the shutdown mode when $\overline{SHDN}$ goes low. $\overline{RD}$ and $\overline{SHDN}$ low selects the quick wake-up nap mode, $\overline{RD}$ high and $\overline{SHDN}$ low selects sleep mode.

$\overline{CONVST}$ (Pin 13): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

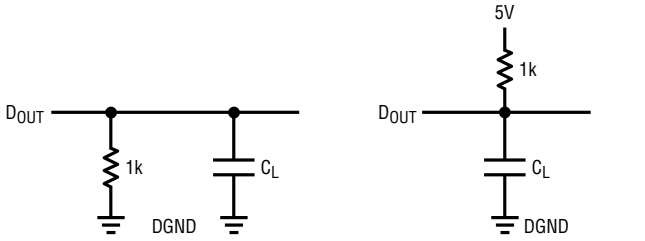
$\overline{BUSY}$ (Pin 14): The $\overline{BUSY}$ output shows the converter status. It is low when a conversion is in progress.

V_{SS} (Pin 15): Negative Supply, –5V for Bipolar Operation. Bypass to AGND using 10µF tantalum in parallel with 0.1µF ceramic. Analog ground for unipolar operation.

V_{DD} (Pin 16): 5V Positive Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

TEST CIRCUITS

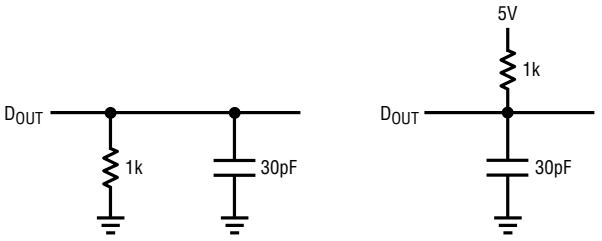
Load Circuits for Access Timing



A) HI-Z TO V_{OH} AND V_{OL} TO V_{OH} B) HI-Z TO V_{OL} AND V_{OH} TO V_{OL}

1417 TC01

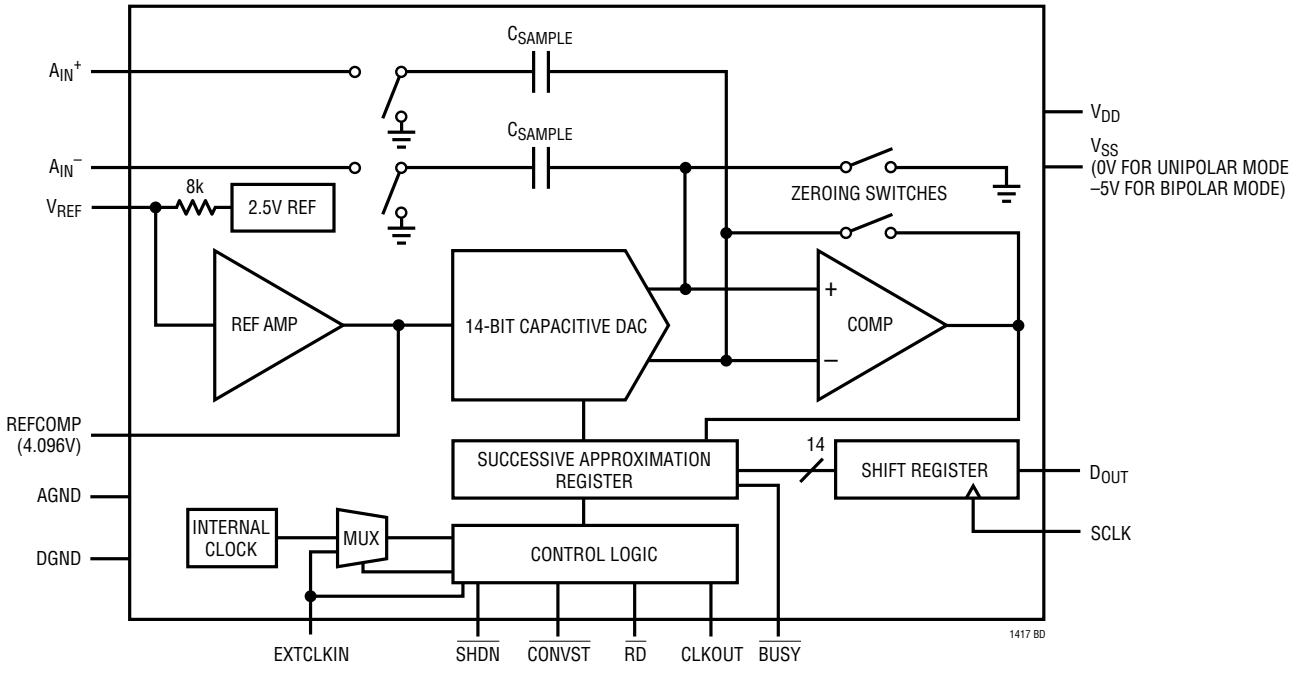
Load Circuits for Output Float Delay



A) V_{OH} TO HI-Z B) V_{OL} TO HI-Z

1417 TC02

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1417 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 14-bit serial output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs (please refer to Digital Interface section for the data format).

Conversion start is controlled by the $\overline{\text{CONVST}}$ input. At the start of the conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During the conversion, the internal differential 14-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN}^+ and A_{IN}^- inputs are connected to the sample-and-hold capacitors (C_{SAMPLE}) during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a minimum delay of 500ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal. During the convert phase the comparator zeroing switches open, putting the comparator into compare mode. The input switches the C_{SAMPLE} capacitors to ground, transferring the differential analog input charge onto the summing junction. This input charge is successively compared with the binary weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the differential DAC output balances the A_{IN}^+ and A_{IN}^- input charges. The SAR contents (a 14-bit data word) which represent the difference of A_{IN}^+ and A_{IN}^- are output through the serial pin D_{OUT}.

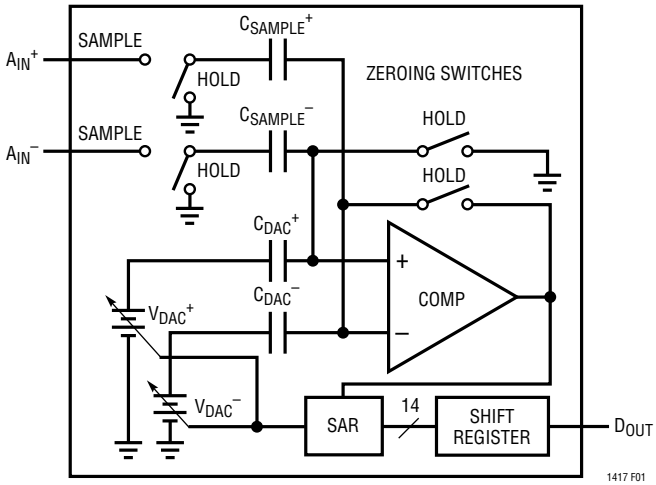


Figure 1. Simplified Block Diagram

APPLICATIONS INFORMATION

DRIVING THE ANALOG INPUT

The differential analog inputs of the LTC1417 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the A_{IN}^- input is grounded). The A_{IN}^+ and A_{IN}^- inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low then the LTC1417 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 2). For minimum acquisition time, with high source impedance, a buffer amplifier must be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts—500ns for full throughput rate.

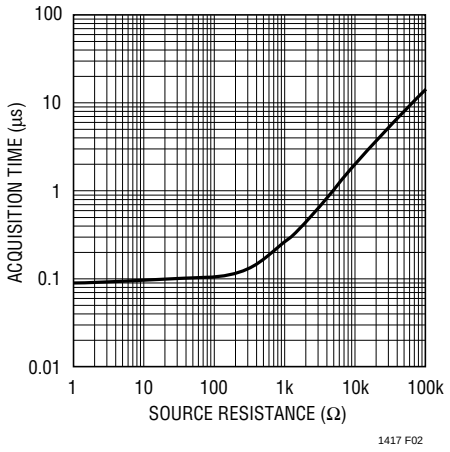


Figure 2. t_{ACQ} vs Source Resistance

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a closed-loop bandwidth of 10MHz, then the output impedance at 10MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 10MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

The best choice for an op amp to drive the LTC1417 will depend on the application. Generally, applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC1417. More detailed information is available in the Linear Technology Databooks and on the LinearView™ CD-ROM.

LT®1354: 12MHz, 400V/µs Op Amp. 1.25mA maximum supply current. Good AC and DC specifications. Suitable for dual supply application.

LT1357: 25MHz, 600V/µs Op Amp. 2.5mA maximum supply current. Good AC and DC specifications. Suitable for dual supply application.

LT1366/LT1367: Dual/Quad Precision Rail-to-Rail Input and Output Op Amps. 375µA supply current per amplifier. 1.8V to ±15V supplies. Low input offset voltage: 150µV. Good for low power and single supply applications with sampling rates of 20ksps and under.

LT1498/LT1499: 10MHz, 6V/µs, Dual/Quad Rail-to-Rail Input and Output Op Amps. 1.7mA supply current per amplifier. 2.2V to ±15V supplies. Good AC performance, input noise voltage = 12nV/√Hz (typ).

LT1630/LT1631: 30MHz, 10V/µs, Dual/Quad Rail-to-Rail Input and Output Precision Op Amps. 3.5mA supply current per amplifier. 2.7V to ±15V supplies. Best AC performance, input noise voltage = 6nV/√Hz (typ), THD = –86dB at 100kHz.

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APPLICATIONS INFORMATION

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1417 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 10MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 3 shows a 2000pF capacitor from $+A_{IN}$ to ground and a 100Ω source resistor to limit the input bandwidth to 800kHz. The 2000pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Range

The ±2.048V and 0V to 4.096V input ranges of the LTC1417 are optimized for low noise and low distortion. Most op amps also perform well over these ranges, allowing direct coupling to the analog inputs and eliminating the need for special translation circuitry.

Some applications may require other input ranges. The LTC1417 differential inputs and reference circuitry can accommodate other input ranges often with little or no additional circuitry. The following sections describe the reference and input circuitry and how they affect the input range.

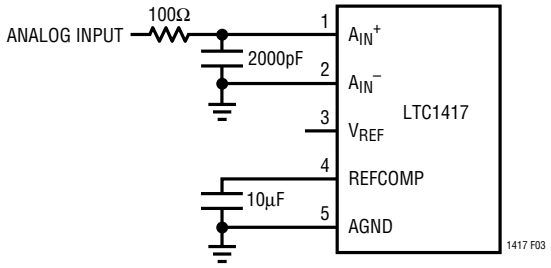

Figure 3. RC Input Filter

APPLICATIONS INFORMATION

INTERNAL REFERENCE

The LTC1417 has an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 2.500V. It is internally connected to a reference amplifier and is available at Pin 3. A 8k resistor is in series with the output so that it can be easily overdriven in applications where an external reference is required, see Figure 4. The reference amplifier compensation pin (REFCOMP, Pin 4) must be connected to a capacitor to ground. The reference is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF in parallel with a 0.1µF ceramic is recommended.

The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment. The reference should be kept in the range of 2.25V to 2.75V for specified linearity.

UNIPOLAR / BIPOLAR OPERATION AND ADJUSTMENT

Figure 5a shows the ideal input/output characteristics for the LTC1417. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, … FS – 1.5LSB). The output code is natural binary with 1LSB = FS/16384 = 4.096V/16384 = 250µV. Figure 5b shows the input/output transfer characteristics for the bipolar mode in two's complement format.

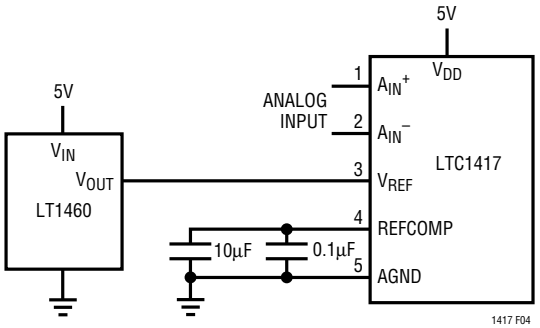

Figure 4. Using the LT1460 as an External Reference

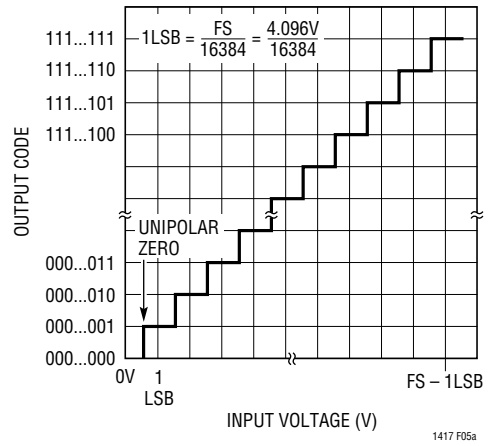

Figure 5a. LTC1417 Unipolar Transfer Characteristics

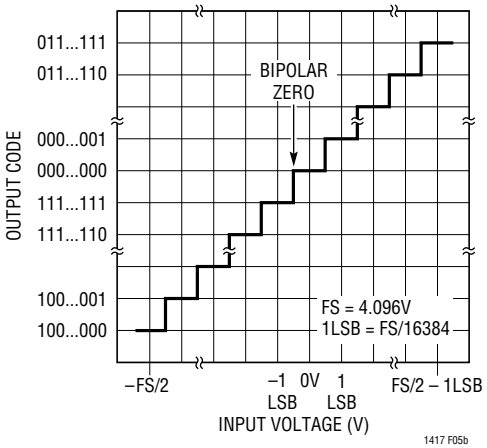

Figure 5b. LTC1417 Bipolar Transfer Characteristics

APPLICATIONS INFORMATION

Unipolar Offset and Full-Scale Error Adjustment

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figures 6a and 6b show the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error apply 125μV (i.e., 0.5LSB) at the input and adjust the offset at the A_{IN}^- input until the output code flickers between 0000 0000 0000 00 and 0000 0000 0000 01. For full-scale adjustment, an input voltage of 4.095625V (FS – 1.5LSBs) is applied to A_{IN}^+ and R2 is adjusted until the output code flickers between 1111 1111 1111 10 and 1111 1111 1111 11.

Bipolar Offset and Full-Scale Error Adjustment

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Again, bipolar offset error must be adjusted before full-scale error. Bipolar offset error adjustment is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error apply –125μV (i.e., –0.5LSB) at A_{IN}^+ and adjust the offset at the A_{IN}^- input until the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11. For full-scale adjustment, an input voltage of 2.047625V (FS – 1.5LSBs) is applied to A_{IN}^+ and R2 is adjusted until the output code flickers between 0111 1111 1111 10 and 0111 1111 1111 11.

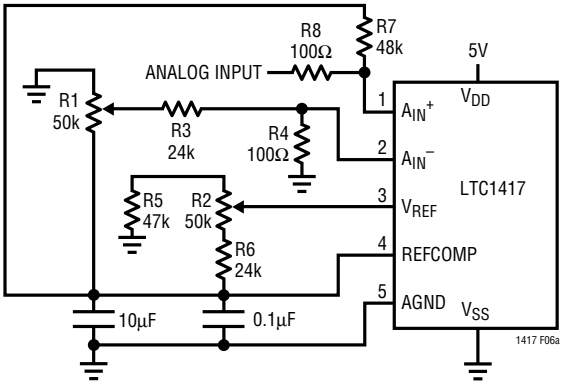

Figure 6a. Offset and Full-Scale Adjust Circuit If –5V Is Not Available

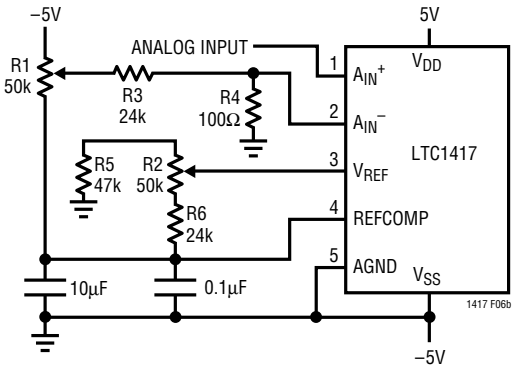

Figure 6b. Offset and Full-Scale Adjust Circuit If –5V Is Available

BOARD LAYOUT AND GROUNDING

To obtain the best performance from the LTC1417, a printed circuit board with ground plane is required. The ground plane under the ADC area should be as free of breaks and holes as possible, such that a low impedance path between all ADC grounds and all ADC decoupling capacitors is provided. It is critical to prevent digital noise from being coupled to the analog input, reference or analog power supply lines. Layout should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 5 (AGND) and Pin 10 (DGND) and all other analog grounds should be connected to this single analog ground plane. The REFCOMP bypass capacitor and the V_{DD} bypass capacitor should also be connected to this analog ground plane. No other digital grounds should be connected to this analog ground plane. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a wait state during conversion or by using three-state buffers to isolate the ADC data bus. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1417 has differential inputs to minimize noise coupling. Common mode noise on the A_{IN}^+ and A_{IN}^- leads will be rejected by the input CMRR. The A_{IN}^- input can be used as a ground sense for the A_{IN}^+ input; the LTC1417 will hold and convert the difference voltage between A_{IN}^+ and A_{IN}^-. The leads to A_{IN}^+ (Pin 1) and A_{IN}^- (Pin 2) should be kept as short as possible. In applications where this is not possible, the A_{IN}^+ and A_{IN}^- traces should be run side by side to equalize coupling.

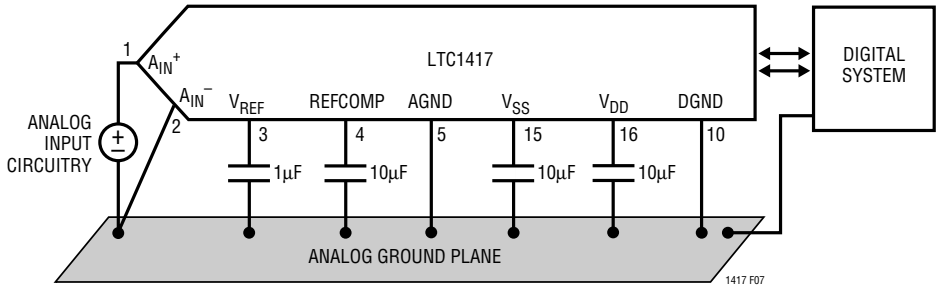

Figure 7. Power Supply Grounding Practice

APPLICATIONS INFORMATION

SUPPLY BYPASSING

High quality, low series resistance ceramic, 10µF bypass capacitors should be used at the V_{DD} and REFCOMP pins. Surface mount ceramic capacitors such as Murata GRM235Y5V106Z016 provide excellent bypassing in a small board space. Alternatively 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors can be used.

Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

DIGITAL INTERFACE

The LTC1417 operates in serial mode. The $\overline{RD}$ control input is common to all peripheral memory interfacing. Only four digital interface lines are required, SCLK, $\overline{CONVST}$, EXTCLKIN and D_{OUT}. SCLK, the serial data shift clock can be an external input or supplied by the LTC1417 internal clock.

Internal Clock

The ADC has an internal clock. Either the internal clock or an external clock may be used as the conversion clock (see Figure 9). The internal clock is factory trimmed to achieve a typical conversion time of 1.8µs and a maximum conversion time over the full operating temperature range of 2.5µs. No external adjustments are required, and with the guaranteed maximum acquisition time of 0.5µs, throughput performance of 400ksps is assured.

Power Shutdown

The LTC1417 provides two power shutdown modes, nap and sleep, to save power during inactive periods. The nap mode reduces the power by 80% and leaves only the digital logic and reference powered up. The wake-up time from nap to active is 500ns (see Figure 8). In sleep mode all bias currents are shut down and only leakage current remains—about 2µA. Wake-up time from sleep mode is much slower since the reference circuit must power up and settle to 0.005% for full 14-bit accuracy. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 4). The wake-up time is 30ms with the recommended 10µF capacitor. Shutdown is controlled by Pin 11 ($\overline{SHDN}$); the ADC is in shutdown when it is low. The shutdown mode is selected with Pin 12 ($\overline{RD}$); low selects nap, high selects sleep.

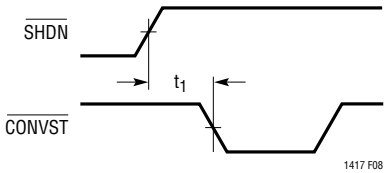

Figure 8. $\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing

Conversion Control

Conversion start is controlled by the $\overline{CONVST}$ input. A falling edge of $\overline{CONVST}$ pin will start a conversion. Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output. $\overline{BUSY}$ is low during a conversion.

Data Output

Output will be active when $\overline{RD}$ is low. A high $\overline{RD}$ will three-state the ouput. In unipolar mode (V_{SS} = 0V) the data will be in straight binary format (corresponding to the unipolar input range). In bipolar mode (V_{SS} = –5V), the data will be in two's complement format (corresponding to the bipolar input range).

Serial Output Mode

Conversions are started by a falling $\overline{CONVST}$ edge. After a conversion is completed and the output shift register has been updated, $\overline{BUSY}$ will go high and valid data will be available on D_{OUT} (Pin 9). This data can be clocked out either before the next conversion starts or it can be clocked out during the next conversion. To enable the serial data output buffer and shift clock, $\overline{RD}$ must be low.

APPLICATIONS INFORMATION

Figure 9 shows a function block diagram of the LTC1417. There are two pieces to this circuitry: the conversion clock selection circuit (EXTCLKIN and CLKOUT) and the serial port (SCLK, D_{OUT} and $\overline{RD}$).

Conversion Clock Selection

In Figure 9, the conversion clock controls the internal ADC operation. The conversion clock can be either internal or external. By connecting EXTCLKIN high, the internal clock is selected. This clock generates 16 clock cycles which feed into the SAR for each conversion.

To select an external conversion clock, apply an external conversion clock to EXTCLKIN (Pin 6). (When an external shift clock (SCLK) is used during a conversion, the SCLK should be used as the external conversion clock to avoid the noise generated by the asynchronous clocks. To maintain accuracy the external conversion clock frequency must be between 50kHz and 9MHz.) The SAR sends an end of conversion signal, $\overline{EOC}$, that gates the external conversion clock so that only 16 clock cycles can go into the SAR, even if the external clock, EXTCLKIN, contains more than 16 cycles.

When $\overline{RD}$ is low, these 16 cycles of conversion clock (whether internally or externally generated) will appear on CLKOUT during each conversion and then CLKOUT will remain low until the next conversion. If desired, CLKOUT can be used as a master clock to drive the serial port. Because CLKOUT is running during the conversion, it is important to avoid excessive loading that can cause large supply transients and create noise. For the best performance, limit CLKOUT loading to 20pF.

Serial Port

The serial port in Figure 9 is made up of a 16-bit shift register and a three-state output buffer that are controlled by two inputs: SCLK and $\overline{RD}$. The serial port has one output, D_{OUT}, that provides the serial output data.

The SCLK is used to clock the shift register. Data may be clocked out with the internal conversion clock operating as a master by connecting CLKOUT (Pin 8) to SCLK (Pin 7) or with an external data clock applied to SCLK. The minimum number of SCLK cycles required to trans-

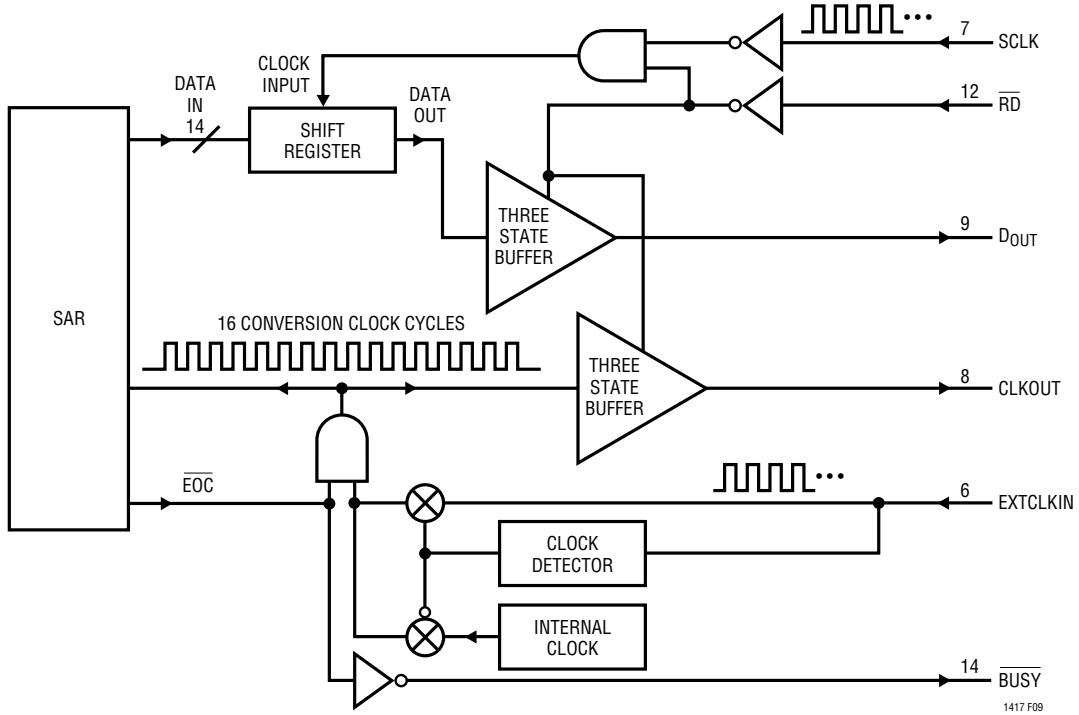

Figure 9. Functional Block Diagram

APPLICATIONS INFORMATION

fer a data word is 14. Normally, SCLK contains 16 clock cycles for a word length of 16 bits; 14 bits with MSB first, followed by two trailing zeros.

A logic high on $\overline{RD}$ disables SCLK and three-states D_{OUT}. In case of using a continuous SCLK, $\overline{RD}$ can be controlled to limit the number of shift clocks to the desired number (i.e., 16 cycles) and to three-state D_{OUT} after the data transfer.

In power shutdown mode ($\overline{SHDN}$ = low), a high $\overline{RD}$ selects sleep mode while a low $\overline{RD}$ selects nap mode.

D_{OUT} outputs the serial data; 14 bits, MSB first, on the falling edge of each SCLK (see Figures 10 and 11). If 16 SCLKs are provided, the 14 data bits will be followed by two zeros. The MSB (D13) will be valid on the first rising and the first falling edge of the SCLK. D12 will be valid on the second rising and the second falling edge as will all the remaining bits. The data may be captured on either edge. The largest hold time margin is achieved if data is captured on the rising edge of SCLK.

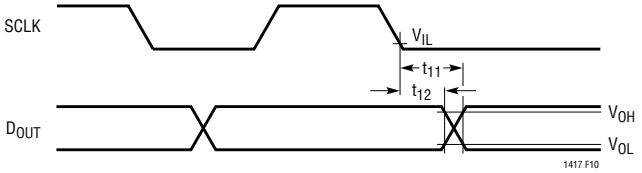

Figure 10. SCLK to D_{OUT} Delay

$\overline{BUSY}$ gives the end of conversion indication. When the LTC1417 is configured as a master serial device, $\overline{BUSY}$ can be used as a framing pulse and to three-state the serial port after transferring the serial output data by tying it to the $\overline{RD}$ pin.

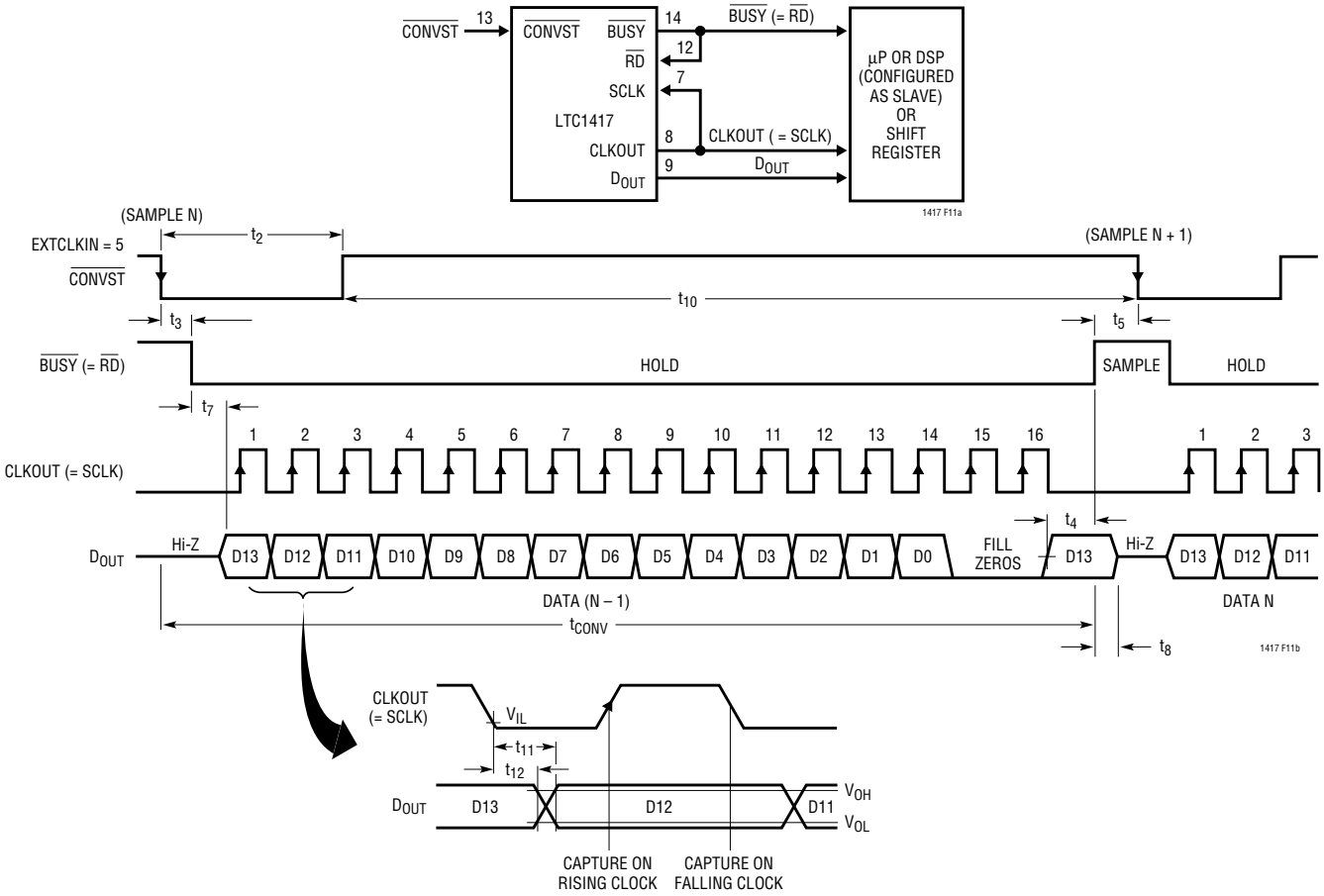

Figure 11. Internal Conversion Clock Selected. Data Transferred During Conversion Using the ADC Clock Output as a Master Shift Clock (SCLK Driven from CLKOUT)

APPLICATIONS INFORMATION

Figures 11 to 14 show several serial modes of operation, demonstrating the flexibility of the LTC1417 serial port.

Serial Data Output During a Conversion

Using Internal Conversion Clock for Conversion and Data Transfer. Figure 11 shows data from the previous conversion being clocked out during the conversion with the LTC1417 internal clock providing both the conversion clock and the SCLK. The internal clock has been optimized for the fastest conversion time, consequently this mode can provide the best overall speed performance. To select an internal conversion clock, tie EXTCLKIN (Pin 6) high. The internal clock appears on CLKOUT (Pin 8) which can be tied to SCLK (Pin 7) to supply the SCLK.

Using External Clock for Conversion and Data Transfer. In Figure 12, data from the previous conversion is output during the conversion with an external clock providing both the conversion clock and the shift clock. To select an external conversion clock, apply the clock to EXTCLKIN. The same clock is also applied to SCLK to provide a data shift clock. To maintain accuracy the conversion clock frequency must be between 50kHz and 9MHz.

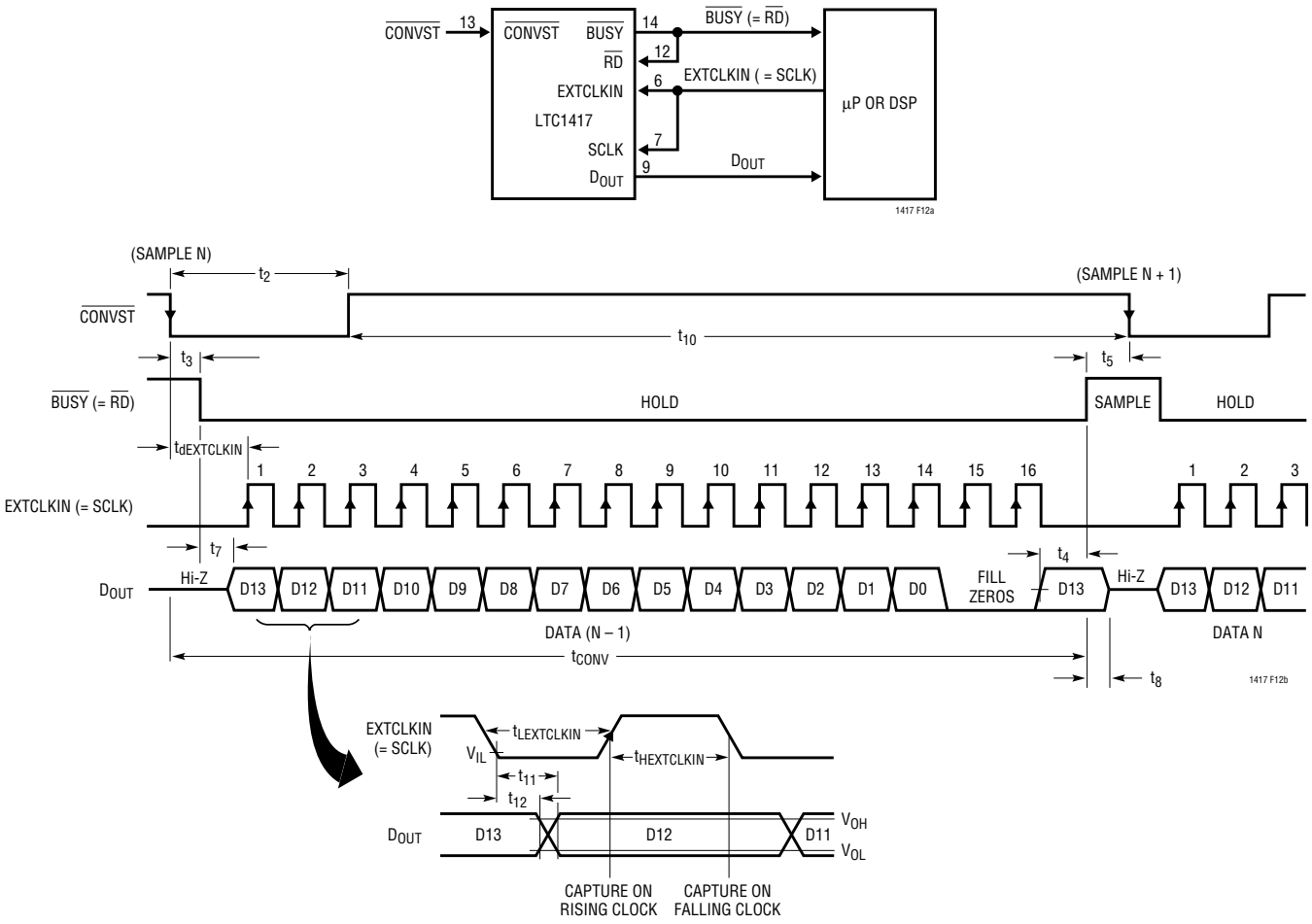

Figure 12. External Conversion Clock Selected. Data Transferred During Conversion Using the External Clock (External Clock Drives Both EXTCLKIN and SCLK)

APPLICATIONS INFORMATION

It is not recommended to clock data with an external clock during a conversion that is running on an internal clock because the asynchronous clocks may create noise.

Serial Data Output After a Conversion

Using Internal Conversion Clock and External Data Clock. In this mode, data is output after the end of each conversion but before the next conversion is started (Figure 13). The internal clock is used as the conversion clock and an external clock is used for the SCLK. This mode is useful in applications where the processor acts as a master serial device. This mode is SPI and MICROWIRE™ compatible. It also allows operation when the SCLK frequency is very low (less than 30kHz). To select the internal conversion clock tie EXTCLKIN high. The external SCLK is applied to SCLK. $\overline{RD}$ can be used to gate the external SCLK, such that data will clock only after $\overline{RD}$ goes low and to three-state D_{OUT} after data transfer. If more than 16 SCLKs are provided, more zeros will be filled in after the data word indefinitely.

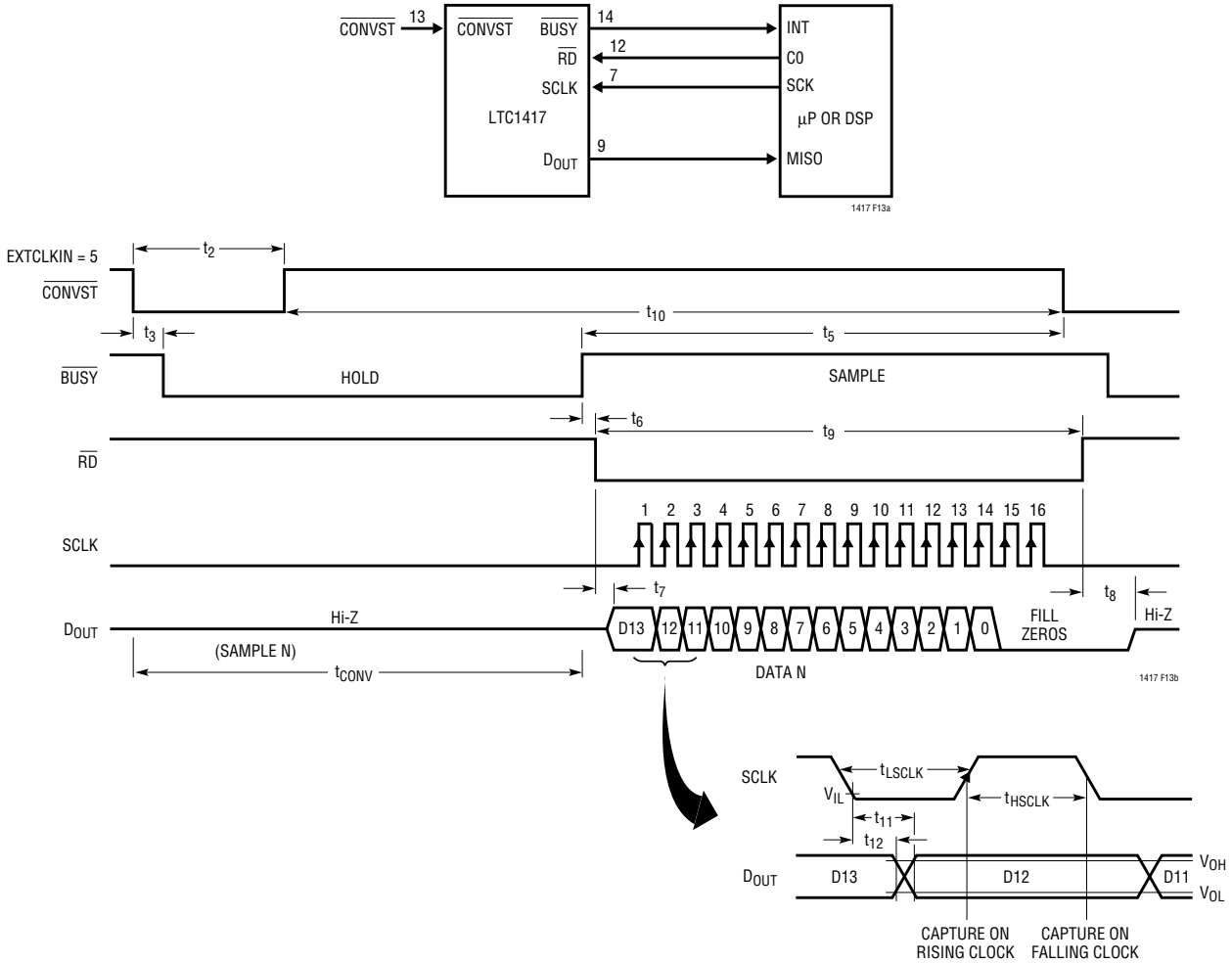

Figure 13. Internal Conversion Clock Selected. Data Transferred After Conversion Using an External SCLK. BUSY↑ Indicates End of Conversion

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APPLICATIONS INFORMATION

Using External Conversion Clock and External Data Clock. In Figure 14, data is also output after each conversion is completed and before the next conversion is started. An external clock is used for the conversion clock and either another or the same external clock is used for the SCLK. This mode is identical to Figure 13 except that an external clock is used for the conversion. This mode allows the user to synchronize the A/D conversion to an external clock either to have precise control of the internal bit test timing or to provide a precise conversion time. As in Figure 13, this mode works when the SCLK frequency is very low (less than 30kHz). However, the external conversion clock must be between 30kHz and 9MHz to maintain accuracy. If more than 16 SCLKs are provided, more zeros will be filled in after the data word indefinitely. To select the external conversion clock, apply an external conversion clock to EXTCLKIN. The external SCLK is applied to SCLK. $\overline{RD}$ can be used to gate the external SCLK such that data will clock only after $\overline{RD}$ goes low.

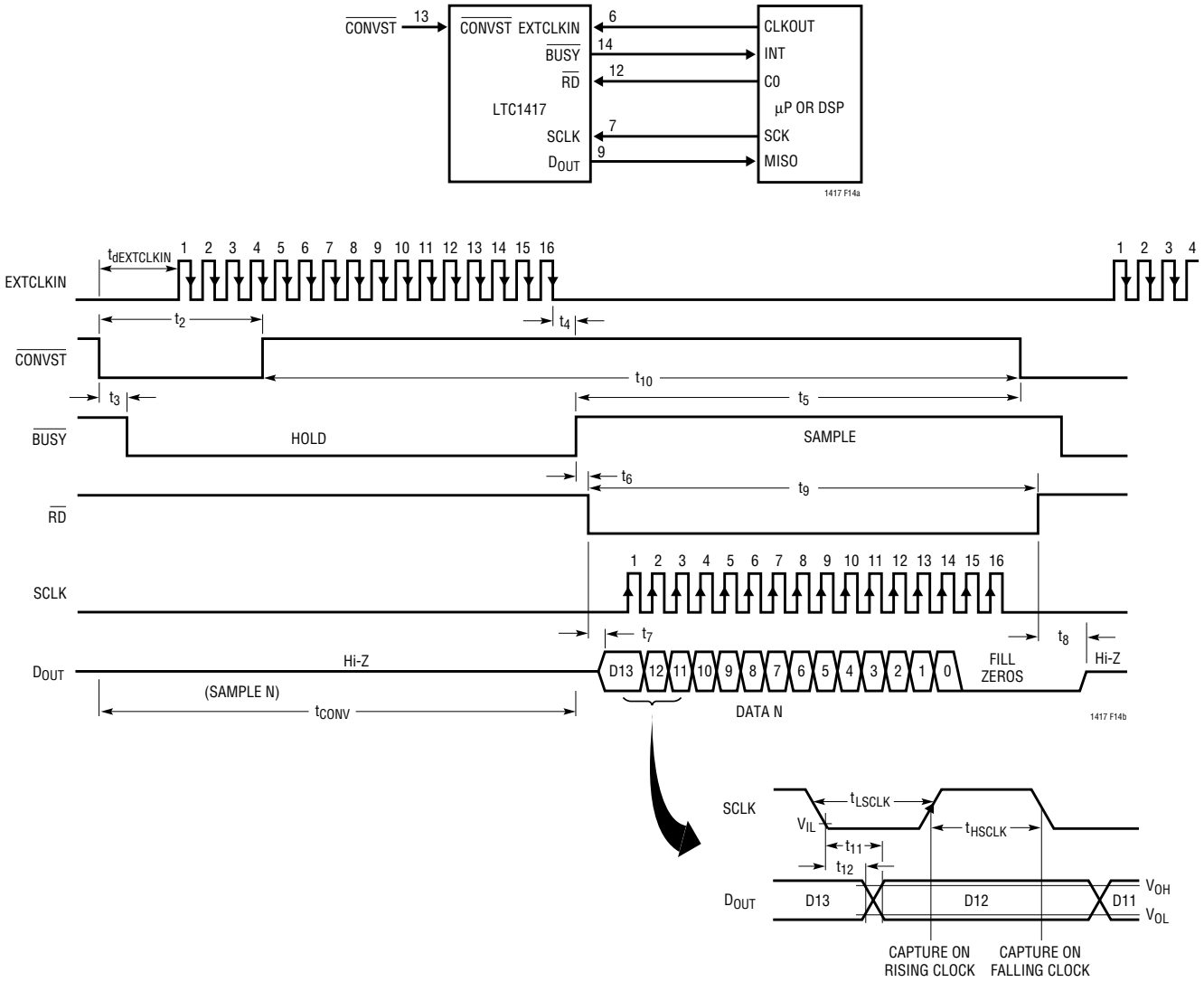
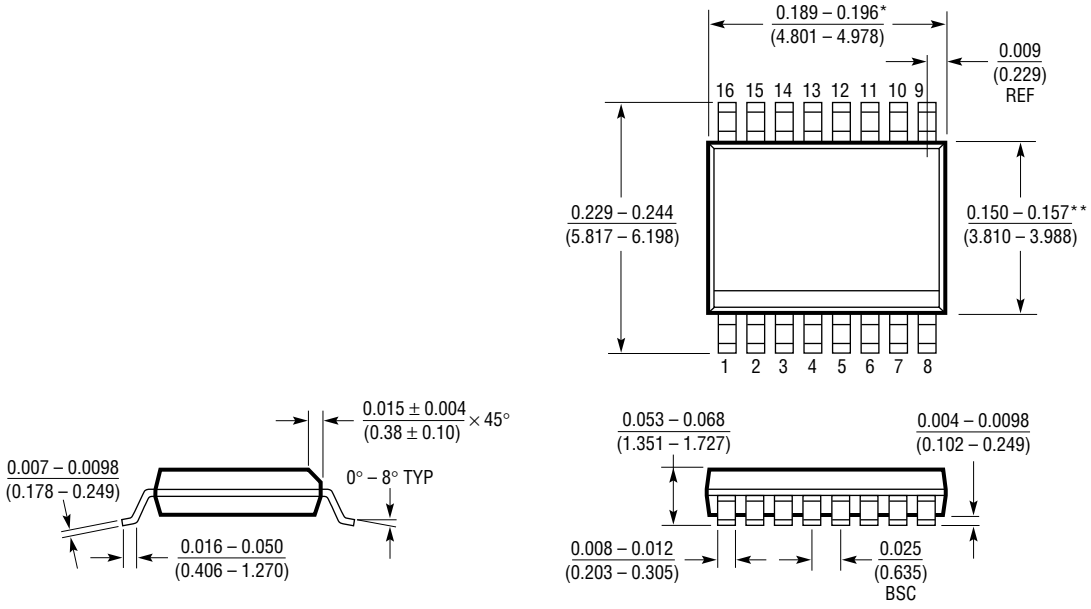


Figure 14. External Conversion Clock Selected. Data Transferred After Conversion Using an External SCLK. $\overline{BUSY}\uparrow$ Indicates End of Conversion

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



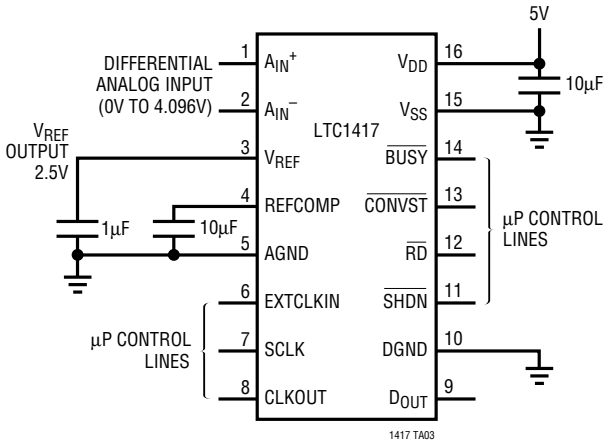
* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0398

TYPICAL APPLICATION

Single 5V Supply, 400kHz, 14-Bit Sampling A/D Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC1274/LTC1277	Low Power, 12-Bit, 100ksps ADCs with Parallel Output	10mW Power Dissipation, Parallel/Byte Interface
LTC1412	12-Bit, 3Msps Sampling ADC with Parallel Output	Best Dynamic Performance, SINAD = 72dB at Nyquist
LTC1415	Single 5V, 12-Bit, 1.25Msps ADC with Parallel Output	55mW Power Dissipation, 72dB SINAD
LTC1416	Low Power, 14-Bit, 400ksps ADC with Parallel Output	70mW Power Dissipation, 80.5dB SINAD
LTC1418	Low Power, 14-Bit, 200ksps ADC with Parallel and Serial I/O	True 14-Bit Linearity, 81.5dB, SINAD, 15mW Dissipation
LTC1419	Low Power, 14-Bit, 800ksps ADC with Parallel Output	True 14-Bit Linearity, 81.5dB SINAD, 150mW Dissipaton
LTC1604	16-Bit, 333ksps Sampling ADC with Parallel Output	±2.5V Input, 90dB SINAD, 100dB THD
LTC1605	Single 5V, 16-Bit, 100ksps ADC with Parallel Output	Low Power, ±10V Inputs, Parallel/Byte Interface
DACs		
LTC1595	16-Bit CMOS Mulitplying DAC in SO-8	±1LSB Max INL/DNL, 1nV • sec Glitch, DAC8043 Upgrade
LTC1596	16-Bit CMOS Mulitplying DAC	±1LSB Max INL/DNL, DAC8143/AD7543 Upgrade
Reference		
LT1019-2.5	Precision Bandgap Reference	0.05% Max, 5ppm/°C Max

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