PM7350

S/UNI-DUPLEX™

S/UNI-DUPLEX

Dual Serial Link, PHY Multiplexer

DEVICE ERRATA

RELEASED

Issue 4: May 2001

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PMC-1990883 (R4)

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Contacting PMC-Sierra

PMC-Sierra
8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000
Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Technical Support: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

Revision History

Issue No.	Issue Date	Details of Change
Issue 4	May, 2001	Added the sequence of device register initialization. Minor wording changes related to the transition to a new template.
Issue 3	August, 2000	Updated for Production Release. Added back to back transfer mode functional discrepancy.
Issue 2	December, 1999	Added information about new Revision B slave mode. Updated mechanical dimensions for Revision B 4-layer substrate. Updated timing reference jitter specification. Corrected part number information. Listed Revision B fixes to Revision A functional discrepancies.
Issue 1	July ,1999	

Contents

1 Introduction

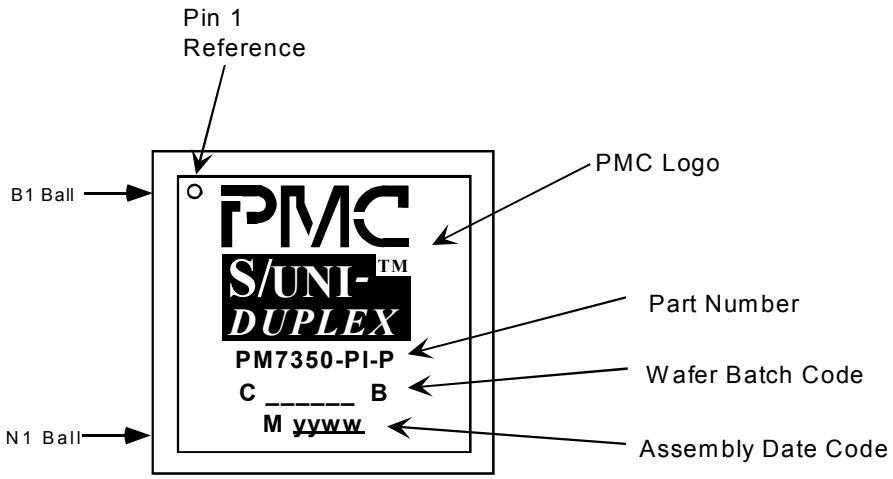
In this document:

- Section 2 lists the known functional errata for Revision B of the PM7350 S/UNI-DUPLEX only.
- Section 3 lists the documentation errors found in Issue 5 of the PM7350 S/UNI-DUPLEX Datasheet.

1.1 Device Identification

The information contained in this document applies to Revision B of the PM7350 S/UNI-DUPLEX only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device.

Figure 1 - PM7350 S/UNI-DUPLEX Branding Format



Not to Scale

1.2 References

- PMC-1980581, PM7350 S/UNI-DUPLEX Dual Serial Link, PHY Multiplexer Datasheet, Issue 5, April 2000.
- PMC-1981025, S/UNI-VORTEX and S/UNI-DUPLEX Technical Overview, Issue 2, June 1999.

2 Device Functional Deficiency List

This section lists the known functional deficiencies for Rev B of the S/UNI-DUPLEX as of the publication of this document. For each deficiency, the known workaround and the operating constraints, with and without the workaround, are also described.

Please report any functional discrepancies not covered in this document to PMC-Sierra.

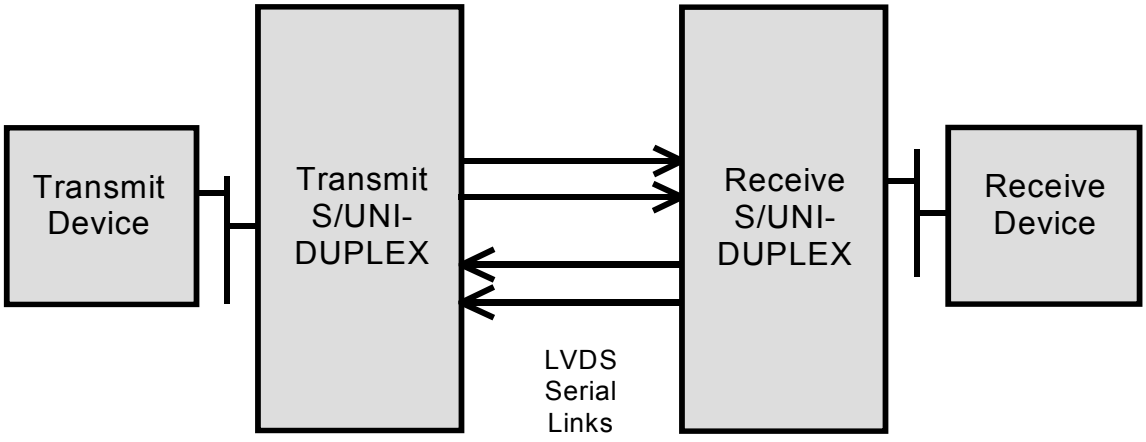
2.1 Low Data Throughput in Back-to-Back Mode

- *S/UNI-VORTEX & S/UNI-DUPLEX Technical Overview*, Section 4.2.2.
- *S/UNI-DUPLEX Dual Serial Link, PHY Multiplexer Datasheet*, Sections 9.3, 9.4 and 12.3.

2.1.1 Description

When using two S/UNI-DUPLEXs "back-to-back" as a UTOPIA serializer, the backpressure mechanism may limit the data throughput to no more than one half of the theoretical maximum throughput of the LVDS link[1].

In order to understand the root cause and resolution of this behavior, it is important to understand the backpressure mechanism used by the S/UNI-DUPLEX. The simplified configuration shown in the diagram below will be used for this discussion. In this case it is assumed that there is only one active logical channel being used.



[1] *S/UNI-DUPLEX Dual Serial Link, PHY Multiplexer Datasheet*, Section 12.3.

The high speed serial interface (LVDS) links utilize a cell-based data structure which consists of the ATM user data and a system prepend[2]. Included in this system prepend is per-PHY flow control information which enables the S/UNI-DUPLEX to implement a backpressure mechanism. The S/UNI-DUPLEX uses backpressure to control cell flow and prevent cell loss due to bursts in traffic from a PHY on a logical channel. Backpressure information is sampled and sent every second LVDS cell, i.e., one LVDS cell contains backpressure information for 16 logical channels while the next LVDS cell contains backpressure information for the remaining 16 logical channels. Cells are sent continuously over the LVDS link. If no user cells are available to be sent, idle cells are inserted in their place to carry the backpressure information. These idle cells are discarded at the receiving S/UNI-DUPLEX.

On the LVDS receive interface, the S/UNI-DUPLEX has a four cell FIFO per channel and asserts backpressure if there are two or more cells in this FIFO[3]. Because backpressure information for a specific logical channel is sent every second cell, the FIFO must accommodate up to two additional cells which may be sent before the transmit S/UNI-DUPLEX receives and responds to the backpressure information. Without this two cell headroom, cells could be lost due to FIFO overflow. The transmit S/UNI-DUPLEX cannot resume sending cells on the logical channel until the backpressure is cleared. During this time, the transmit S/UNI-DUPLEX will send idle cells over the LVDS link[4]. When the receive S/UNI-DUPLEX FIFO contains less than two cells, the backpressure status is de-asserted and sent to the transmit S/UNI-DUPLEX which can then resume sending cells.

It is important to note that when the first payload byte of a cell received from the LVDS bit stream is written into the FIFO, the FIFO cell position is considered filled. When the last byte of a cell transferred to the bus is read from the FIFO, the FIFO cell position is considered empty. Therefore, if a cell is being written into the FIFO from the LVDS link at the same time another cell is being read out of the FIFO via the Utopia bus, the FIFO is considered “near full” and backpressure is asserted. Even if a cell is read out of the FIFO immediately following the transmission of the backpressure information, the backpressure status cannot not be updated for two LVDS cell times. After this delay, the transmit S/UNI-DUPLEX is permitted to start sending cells again. Depending on the relative phase and frequency of cells being written into the FIFO (i.e. the cell rate on the LVDS link) and cells being read out of the FIFO (i.e. the cell rate of the PHY device receiving the cells via the UTOPIA bus interface), the backpressure status could continue to alternate between asserted and cleared indefinitely. This would result in only one half of the LVDS link bandwidth being utilized by user cells with the remainder carrying idle cells.

[2] *S/UNI-DUPLEX Dual Serial Link, PHY Multiplexer Datasheet*, Section 9, Figure 9.

[3] *S/UNI-DUPLEX Dual Serial Link, PHY Multiplexer Datasheet*, Section 9.4.1.

[4] In the case described there is only one active logical channel. If there is more than one active channel, the S/UNI-DUPLEX will simply send cells from another channel instead.

2.1.2 Workaround

This backpressure cycling can be modified by increasing the "FIFO near-full" threshold level from 2 to 3 via the undocumented Receive Channel FIFO Ready Level (Register 0x3F). Changing this fill level does not increase the total number of cells in the FIFO – it still remains at four cells. Therefore, by increasing the FIFO full level to 3 the headroom in the FIFO is reduced from two cells to one cell. As mentioned previously, this could result in FIFO overflow if the receiving device does not drain at least one cell from the FIFO in the time it takes the LVDS link to write in the two cells that may arrive due to the backpressure latency.

2.1.3 Performance With/Without Workaround

You must exercise caution before changing the Rx Ready Level. It is important to understand both the desired throughput of the transmit logical channel and the receive device characteristics before overwriting the default value of 2 cells. Since the behavior described only occurs in very specific circumstances, **it is strongly recommended that this register not be used without prior consultation with your local PMC-Sierra Field Applications Engineer.**

In order to better understand the effect of changing the FIFO Ready threshold, let's examine three different scenarios.

Scenario 1

In this scenario no device attached to the receive S/UNI-DUPLEX is capable of receiving cells at a rate greater than one half of the available LVDS bandwidth[5]. In this case the backpressure cycling described above has no negative impact on data throughput since, in the worst case, there will always be at least one half of the LVDS bandwidth available for user cells. Hence, there is no need to modify the Rx Ready Level. Indeed, changing the Rx Ready Level to assert backpressure after three cells may actually create problems. Recall that an additional two cells may be sent by the transmit S/UNI-DUPLEX before acting on the backpressure information. Since in this scenario the receive device is not draining the FIFO quickly enough, the second of these cells may arrive before the device has been able to remove a cell from the FIFO. FIFO overflow occurs and the cell is discarded. **Therefore the default Rx Ready Level of 2 cells is appropriate for one or more channels of low speed data.**

[5] The LVDS bandwidth available for user data is impacted by the system overhead, the cell format used on the link, and by the link rate itself. This is described in *S/UNI-VORTEX & S/UNI-DUPLEX Technical Overview*, Section 4.2.2.

Scenario 2

In this scenario there is a desire to have one logical channel operate at greater than one half of the available LVDS bandwidth because the receive device is capable of accepting all of the traffic presented by the receive S/UNI-DUPLEX up to the full available bandwidth of the LVDS link. In other words, the receive device can drain the FIFO at the maximum rate (which is determined by the speed of the UTOPIA bus). In this scenario, leaving the Rx Ready Level at the default value of 2 causes the on-off cycling of backpressure described previously. The worst case maximum throughput of a single logical channel will then drop to one-half the LVDS bandwidth, which will not satisfy the desired per channel throughput. In this scenario we recommend that the Rx Ready Level be changed to 3 cells. At a level of 3, the result is that backpressure will never be asserted because the receive device can always keep the FIFO level below the threshold. Hence no backpressure induced idle cells will be generated on the link. This allows full utilization of the available LVDS bandwidth up to the ability of the transmitting and receiving devices to keep the link full[6]. **Therefore, in this scenario changing the Rx Ready Level to 3 cells results in the desired throughput.**

Scenario 3

This scenario is similar to Scenario 2 because there is a desire to have one logical channel operate at greater than one half of the available LVDS bandwidth. However, in this case the receive device is **not** capable of consistently sinking all of the traffic presented to it by the receive S/UNI-DUPLEX. For example, the receive device may have a throughput limitation of 120 Mbit/s, which is less than the theoretical maximum available LVDS link bandwidth (assuming the transmitting device can keep the transmitting S/UNI-DUPLEX full). With an Rx Ready Level equal to 2, backpressure cycles off and on and the maximum per channel bandwidth is limited as discussed previously. Increasing the Rx Ready Level to 3 cells increases maximum throughput, but eventually the throughput difference between the transmitting device and the receiving device results in there being three cells present in the S/UNI-DUPLEX receive FIFO. Hence, backpressure is asserted, reducing instantaneous throughput and potentially resulting in a FIFO overflow as described in Scenario 1.

[6] As the desired logical channel speed approaches the maximum available bandwidth of the link it becomes increasingly important to consider the impact of system level constraints such as the Utopia bus polling times and cell transfer delays. Long term throughput differences between the transmitting device and the receive device may eventually require that the receive S/UNI-DUPLEX apply backpressure. In this case the user must account for the drop in available throughput due to the minimum of two IDLE cells inserted whenever backpressure is asserted.

2.2 Initialization of S/UNI-DUPLEX Registers

- PMC-1980581, *PM7350 S/UNI-DUPLEX Dual Serial Link, PHY Multiplexer Datasheet*

2.2.1 Description

Initialization of the S/UNI-DUPLEX registers in a sequential manner can put the device into an unknown state.

2.2.2 Workaround

The following precautions should be taken when initializing the S/UNI-DUPLEX registers:

- The Input/Output SCI-PHY/Any-PHY interface must be disabled before changing the interface configurations.
- The Rx Logical Channel FIFO must be held in RESET while changing the cell format or length.
- Disable the OCA[7] output by clearing the OCAEN bit before the SCI-PHY/Any-PHY interface master device[8] is enabled or activated. The OCA output is enabled after the master device is enabled.

Example

For example, the following sequence should be followed to write to the S/UNI-DUPLEX registers during initialization:

1. Software reset.
2. Do not write to register 0x0A. Leave it as default 0x00 or write 0x00.
3. Write 0x00 to registers 0x10, 0x11, 0x12, 0x13 (default is 0xFF).
4. Write the other register as specified by the application vector.
5. Write to register 0x10 as required by the application vector (0x11, 0x12, 0x13 remain at 0x00).
6. Write to register 0x0A as required by the application vector.

2.2.3 Performance with Workaround

If you take the precautions listed above, the S/UNI-DUPLEX will initialize normally.

[7] Output Cell Available signal.

[8] An example of a master device is the S/UNI-ATLAS ATM Layer device used in the DSLAM core card reference design.

2.2.4 Performance without Workaround

If you initialize the S/UNI-DUPLEX without taking the precautions listed above, it may enter an unknown state under some conditions.

3 Documentation Deficiency List

We are not aware of any documentation deficiencies at this time. Please report any documentation deficiencies not covered in this errata to PMC-Sierra.

Notes