Improved L-Band Down-Converter for DAB Receivers

Description

The U2730B-N is a monolithically integrated L-band down-converter circuit fabricated in TEMIC Semiconductors' advanced UHF5S technology. This IC is an improved version of the U2730B-B and covers all functions of an L-band downconverter in a DAB receiver. The device includes a gain controlled amplifier, a gain controlled mixer, an output buffer, a gain control block, a power save function for the analog part, an L-band oscillator and a complete frequency syntheziser unit. The frequency syntheziser block consists of a reference oscillator/ buffer, a reference divider, a RF divider, a tristate phase detector, a loop filter amplifier, a lock detector, a programmable charge pump, a test interface and a control interface.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Supply voltage: 8.5 V
- RF frequency range: 1400 MHz to 1550 MHz
- IF frequency range: 150 MHz to 250 MHz
- Enhanced IM3 rejection
- Overall gain control range: typ. 30 dB
- DSB noise figure: 9.5 dB
- Gain-controlled amplifier and L-band mixer
- Power-down function for the analog part
- On-chip gain-control circuitry
- On-chip VCO, typical frequency 1261.568 MHz
- Internal VCO can be overdriven by an external LO
- On-chip frequency synthesizer
  - Fixed LO divider factor: 2464
  - Nine reference divider factors selectable: 32, 33, 35, 36, 48, 49, 63, 64, 65
  - A reference oscillator (can be overdriven by an external reference signal
  - Tristate phase detector with programmable charge pump
  - De-activation of tuning output programmable
  - Lock-status indication
  - Test interface

Block Diagram

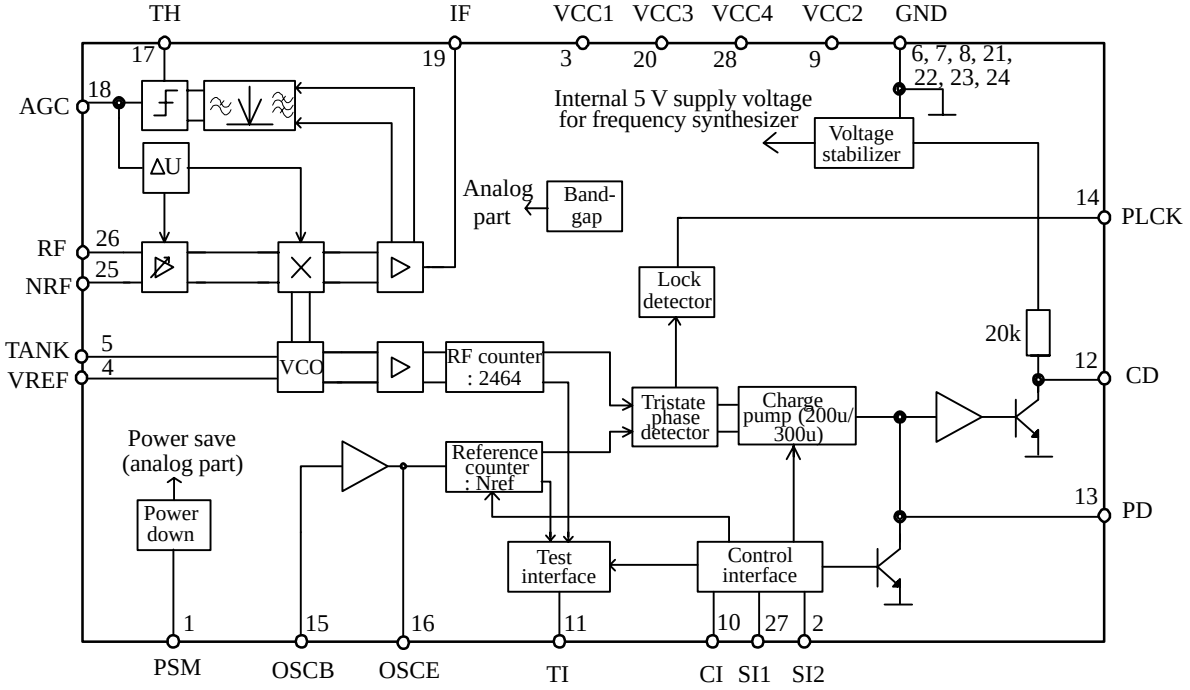


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2730B-NFS	SSO28	Tube
U2730B-NFSG1	SSO28	Taped and reeled according to IEC 286–3

Pin Description

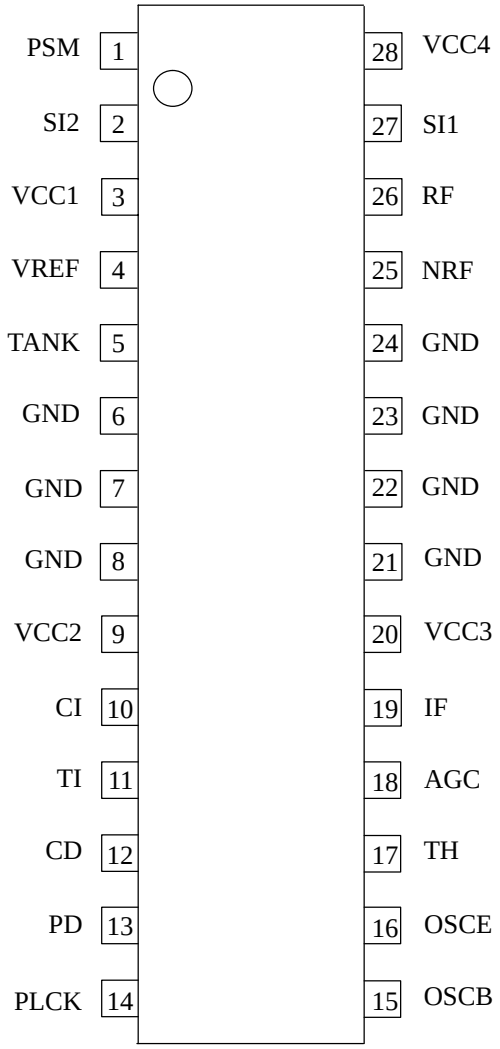


Figure 2. Pinning

Pin	Symbol	Function
1	PSM	Power save mode
2	SI2	Control input
3	VCC1	Supply voltage VCO
4	VREF	Reference pin of VCO
5	TANK	Tank pin of VCO
6, 7, 8, 21, 22, 23, 24	GND	Ground
9	VCC2	Supply voltage PLL
10	CI	Control input
11	TI	Test interface
12	CD	Active filter output
13	PD	Tristate charge pump output
14	PLCK	Lock-indication output (open collector)
15	OSCB	Input of internal oscillator/ buffer
16	OSCE	Output of internal oscillator/ buffer
17	TH	Threshold voltage of comparator
18	AGC	Charge-pump output of comparator, AGC input for amplifier and mixer
19	IF	Intermediate frequency output
20	VCC3	Supply voltage
25	NRF	RF input (inverted)
26	RF	RF input
27	SI1	Control input
28	VCC4	Supply voltage

Functional Description

The U2730B-N is an L-band down-converter circuit covering a gain controlled amplifier, a gain controlled mixer, an output buffer, a gain control circuitry, an L-band oscillator and a frequency synthesizer block. Designed for applications in an DAB receiver the purpose of this circuit is to down-convert incoming L-band signals in the frequency range between 1452 MHz and 1492 MHz to an IF frequency in the range between about 190 MHz and

230 MHz which can be handled by a subsequent DAB tuner. A block diagram of this circuit is shown in figure 1. A main different to the U2730B is an enhanced IM3 rejection. By varying the value of resistor R_{TH} a power threshold between about –33 dBm and –20 dBm at IF– port can be selected.

Gain-Controlled Amplifier

RF signals applied to the input Pin 'RF' are amplified by a gain-controlled amplifier. The complementary Pin NRF is not internally blocked, it is recommended to block this pin carefully by an external capacitor. The gain-control voltage is generated by an internal gain-control circuitry. The output signal of this amplifier is fed to a gain-controlled mixer.

Gain-Controlled Mixer and Output Buffer

The purpose of this mixer is to down-convert the L-band signal in the frequency range of 1452 MHz to 1492 MHz to an IF frequency in the range of about 190 MHz to 230 MHz. Like the amplifier, the gain of the mixer is controlled by the gain-control circuitry. The IF signal is buffered and filtered by a one-pole lowpass filter at a 3-dB frequency of about 500 MHz and then it is fed to the single-ended output Pin IF.

Gain-Control Circuitry

The purpose of the gain-control circuitry is to measure the signal power, to compare it with a certain power level and to generate control voltages for the gain-controlled amplifier and mixer. An equivalent circuit of this functional block is shown in figure 6.

In order to meet this functionality, the output signal of the buffer amplifier is weakly bandpass filtered (transition range about 60 MHz to 550 MHz), rectified, lowpass filtered and fed to a comparator whose threshold can be defined by an external resistor, R_{TH}, at Pin TH. By varying the value of this resistor, a power threshold of about –33 dBm to –20 dBm can be selected. In order to achieve a good intermodulation ratio, it is recommended to keep the power threshold below –25 dBm. An appropriate application is shown in figure 3. Depending on the selection made by the comparator, a charge pump charges or discharges a capacitor which is applied to the Pin AGC. By varying this capacitor, different time constants of the AGC loop can be realized. The voltage arising at the Pin AGC is used to control the gain setting of the gain-controlled amplifier and mixer. The voltage at Pin AGC is in the range of 5.75 V for maximum gain and 0.3 V for minimum gain. This voltage can be use to control a dual-gate GaAs-FET in front of the U2730B-N to archieve an extended AGC–range. By applying an external voltage to the Pin AGC, the internal AGC loop can be overdriven.

Voltage-Controlled Oscillator

A voltage-controlled oscillator supplies an LO signal to the mixer. An equivalent circuit of this oscillator is shown in figure 7. In the application circuits figures 7 and 8, a ceramic coaxial resonator is applied to the oscillator's Pins TANK and VREF. It should be noted that the Pin REF has to be blocked carefully. Figure 8 shows a different application where the oscillator is overdriven by an external oscillator. In any case, a DC path at a low impedance must be established between the Pins TANK and VREF. The output signal of the oscillator is fed to the LO divider block of the frequency synthesizer unit which locks the VCO's frequency on the frequency of a reference oscillator. Figure 12 shows the typical phase-noise performance of the oscillator in locked state.

Overall Properties of the Signal Path

The overall gain of this circuit amounts 24 dB, the gain-control range is about 30 dB. With a new AGC-concept in the amplifier and mixer the U2730B-N reach better intermodulation distance (DIM3) at higher IF output power levels.

Power Save Mode

In different to the U2730B-B the new version offers a power save function. For $V_{PSM} > 2$ V (Pin 1) the power consumption in the analog part (gain-controlled amplifier and mixer and gain-controlled circuitry) is reduced by 80%. The VCO and the PLL is not influenced by the power-down mode.

Frequency Synthesizer

The frequency synthesizer block consists of reference oscillator, a reference divider, an LO divider in order to divide the frequency of the internal oscillator, a tri–state phase detector, a lock detector, a programmable charge pump, a loop filter amplifier, a control interface and a test interface. The control interface is accessed by three control Pins 'CI', 'SI1' and 'SI2'. The test interface provides test signals which represent output signals of the reference and the LO divider.

The purpose of this unit is to lock the frequency f_{VCO} of the internal VCO on the frequency f_{ref} of the reference signal applied to the input Pin OSCB a phase-locked loop according to the following relation:

$$f_{VCO} = SF \times f_{ref} / SF_{ref}$$

where: SF = 2464,

SF_{ref} scaling factor of reference divider according to table 1

Table 1. Scaling factors of the reference frequency

Voltage at Pin SI1	Voltage at Pin SI2	SF_{ref}	Reference Oscillator Frequency
GND	OPEN	36	18.432 MHz
GND	VCC	33	
GND	GND	48	24.576 MHz
OPEN	OPEN	65	
OPEN	VCC	63	
OPEN	GND	64	32.768 MHz
VCC	OPEN	35	17.920 MHZ
VCC	VCC	32	16.384 MHz
VCC	GND	49	

Reference Oscillator

An on-chip crystal oscillator generates the reference signal which is fed to the reference divider. By connecting a quartz crystal to the Pins OSCE, OSCB according to figure 10, this oscillator generates a highly stable reference signal. The U2731B (TEMIC Semiconductors one-chip front-end IC) offers the reference signal at Pin FREF. This reference signal (LC-filtered to suppress the harmonics) can be used to overdrive the oscillator. In this application (see figure 11) the reference signal has to be applied to the Pins OSCB and the Pin OSCE must be left open.

Reference Divider

Nine different scaling factors of the reference divider can be selected by different voltage settings at the input Pins SI1, SI2: 32, 33*, 35, 48, 49*, 65*, 64, 63*. The reference divider factors resulting in reference oscillator frequencies shown in table 1.

*) These scaling factors result in an output frequency of the reference divider of 512 kHz. If harmonics of the Bd. 3 VCO are falling in the L-band reception band, this spurious can influence the AGC of U2730B-N. That could be a problem for small incomming signals. In this case it is possible to switch the reference divider from n_{ref} to $n_{ref}+1$.

LO Divider

The LO divider is operated at the fixed division ratio 2464. Assuming the settings described in the section ‘Reference divider’, the oscillator’s frequency is controlled to be 1261.568 MHz in locked state and the output frequency of the RF divider is 512 kHz.

Phase Comparator, Charge Pump and Loop Filter

The tristate phase detector causes the charge pump to source or to sink current at the output Pin PD depending on the phase relation of its input signals which are provided by the reference and the RF divider respectively. By means of the control Pin CI, two different values of this current can be selected, and furthermore the charge-pump current can be switched off.

The input of the high-gain amplifier (output Pin CD) which is implemented in order to construct a loop filter, as shown in the application circuit, can be switched to GND by means of the control Pin CI (see table 2). In the application circuit figure 3, the loop filter is completed by connecting the Pins PD and CD by an appropriate RC network.

Lock Detector

An internal lock detector checks if the phase difference of the input signals of the phase detector is smaller than approximately 250 ns in seven subsequent comparisons. If a phase lock is detected, the open collector output Pin PLCK is set to HIGH. It should be noted that the output current of this pin must be limited by external circuitry as it is not limited internally. If the voltage at the control Pin CI is chosen to be half the supply voltage, or if this control pin is left open, the lock-detector function is de-activated and the logical value of the PLCK output is undefined.

Testinterface

If the input control Pin CI is left open (high impedance state), a test signal which monitors the output frequency of the reference divider appears at the output Pin TI.

In analogy to the reference divider a test signal which monitors the output frequency of the RF divider appears at the test interface output Pin TI if the input control Pin CI is connect to VCC/2.

Table 2. Control -interface (CI) settings

CI	PD	PLCK	TI
GND	200 µA	ok	–
Vs	300 µA	ok	–
VCC/2	0 µA	Undefined	RF divider
Open	Connected to GND	Undefined	Reference divider

Absolute Maximum Ratings

Parameters		Symbol	Value	Unit
Supply voltage	Pins 3, 9, 20 and 28	V_{CC}	–0.3 to +9.5	V
RF input voltage	Pins 25 and 26	V_{RF}	750	mV_{pp}
Voltage at Pin AGC	Pin 18	V_{AGC}	0.5 to 6	V
Voltage at Pin TH	Pin 17	V_{TH}	–0.3 to +4.0	V
Input voltage at Pin TANK (internal oscillator overdriven)	Pin 5	V_{TANK}	1	V_{pp}
Current at IF output	Pin 19	I_{IF}	4.0	mA
Reference input voltage (diff.)	Pin 15	OSCB	1	V_{pp}
Control input voltage	Pins 1, 2, 10 and 27	CI, SI1, SI2, PD	–0.3 to +9.5	V
PLCK output current	Pin 14	I_{PLCK}	0.5	mA
PLCK output voltage	Pin 14	V_{PLCK}	–0.3 to +5.5	V
Junction temperature		T_j	125	°C
Storage temperature		T_{stg}	–40 to +125	°C

Operating Range

Parameter		Symbol	Value	Unit
Supply voltage	Pins 3, 9, 20 and 28	V_{CC}	8.00 to 9.35	V
Ambient temperature		T_{amb}	–40 to +85	°C

Thermal Resistance

Parameter		Symbol	Value	Unit
Junction ambient	SSO28 (mod.)	R_{thJA}	t.b.d.	K/W

Electrical Characteristics

Operating conditions: V_{CC} = 8.5 V, T_{amb} = 25°C, application circuit see figure 3, unless otherwise specified

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current (max. gain)	p_{RF} = –60 dBm, V_{PSM} < 0.5 V	$I_{S,MAX}$		40	48	mA
Supply current (min. gain)	p_{RF} = –10 dBm V_{PSM} < 0.5 V	$I_{S,MIN}$		41	50	mA
Supply current (power save mode)	p_{RF} = –10 dBm V_{PSM} > 2 V	$I_{S,PD}$		20	24	mA

Electrical Characteristics (continued)

Operating conditions: V_{CC} = 8.5 V, T_{amb} = 25°C, application circuit see figure 3, unless otherwise specified

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Amplifier mixer Pin 26 → 19						
Maximum conversion gain	p_{RF} = –60 dBm	$g_{c,max}$	20	24		dB
Minimum conversion gain	p_{RF} = –15 dBm	$g_{c,min}$		–8		dB
AGC range		Δg_c	28	32		dB
Third order 2 tone intermodulation ratio	$p_{RF1} + p_{RF2}$ = –10 dBm $p_{RF1} + p_{RF2}$ = –15 dBm	dim3	30 35	35 40		dB dB
DSB noise figure (50-Ω system)	Maximum gain Minimum gain	NF		10 30		dB dB
RF input Pin 26						
Frequency range		$f_{in,RF}$	1400		1550	MHz
Maximum input power	dim3 ≥ 20 dB	$p_{in,max,RF}$		–6		dBm
Input impedance		$Z_{in,RF}$		200 ‖ 1		Ω ‖ pF
IF output Pin 19						
Frequency range		$f_{out,IF}$	150		250	MHz
Output impedance		$Z_{out,IF}$		50		Ω
Voltage standing wave ratio		$VSWR_{IF}$		2.0		
Gain control						
Threshold adjustment	External resistor Pin 17	R_{TH}		100		kΩ
Charge pump current	p_{RF} = –10 dBm Pin 18 V_{agc} = 3.5 V	$I_{CP,P}$	75	100	125	µA
	p_{RF} = –60 dBm V_{agc} = 3.5 V	$I_{CP,N}$	–125	–100	–75	µA
Minimum gain control voltage	p_{RF} = –10 dBm Pin 18	V_{AGCmin}		0.1	0.6	V
Maximum gain control voltage	p_{RF} = –60 dBm Pin 18	V_{AGC}max	5.5	5.75		V
VCO Pin 5						
Frequency		f_{LO}	1000	1261.568	1500	MHz
Phase noise	1 kHz distance	L_{1kHz}		–75		dBc/Hz
Minimum input power	VCO overdriven, application circuit see figure 6	$p_{LO,MIN}$		–11		dBm
Maximum input power		$p_{LO,MAX}$		–5		dBm
Frequency synthesizer						
RF divide factor		SF		2464		
Reference divide factor	SI1 = GND, SI2 = GND SI1 = GND, SI2 = VCC SI1 = GND, SI2 = open SI1 = VCC, SI2 = GND SI1 = VCC, SI2 = VCC SI1 = VCC, SI2 = open SI1 = open, SI2 = GND SI1 = open, SI2 = VCC SI1 = open, SI2 = open	SF_{ref}		48 33 36 49 32 35 64 63 62		

Electrical Characteristics (continued)

Operating conditions: V_{CC} = 8.5 V, T_{amb} = 25°C, application circuit see figure 3, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Input frequency range		f_{ref}	5		50	MHz
Input sensitivity	Pin 15	V_{refs}			30	mV_{rms}
Maximum input signal	Pin 15	V_{refmax}		300		mV_{rms}
Input impedance	Single-ended	Z_{ref}		2.7k ‖ 2.5		kΩ ‖ pF
Phase detector						
Charge-pump current	Pin CI connected to GND Pin 13	I_{PD2}	160	200	240	µA
	Pin CI connected to VCC	I_{PD1}	240	300	360	µA
	Pin CI connected to V_{CC}/2	$I_{PD1,tri}$			100	nA
Output voltage PD	Pin CI open Pin 13	V_{PD}			0.3	V
Internal reference frequency		f_{PD}		512		kHz
Typical tuning voltage range	Pin 12	V_{tune}	0.3		5	V
Lock indication PLCK Pin 14						
Leakage current	V_{PLCK} = 5.5 V	I_{PLCK}			10	µA
Saturation voltage	I_{PLCK} = 0.25 mA	$V_{PLCK,sat}$			0.5	V
Control inputs SI Pins 2 and 27						
Input voltage	Pin connected to GND	V_L	0		0.1	V
	Pin open	V_M		open		
	Pin connected to V_{CC}	V_H	0.9		1	V
Control input CI Pin 10						
Input voltage	Pin connected to GND	V_L	0		0.1	V
	Pin connected to V_{CC}/2	V_M		0.5		V
	Pin open	V_{open}		open		
	Pin connected to V_{CC}	V_H	0.9		1	V
Test interface TI Pin 11						
Reference test frequency	Pin CI open	$f_{test,ref}$		512		kHz
LO test frequency	Pin CI = VCC/2	$f_{test,LO}$		512		kHz
Voltage swing	$R_{load} \geq 1$ MΩ, $C_{load} \leq$ 15 pF, Pin CI open or VCC/2	Vsw		400		mV_{pp}
Power-save mode PSM Pin 1						
	PSM not active	V_{PSM}			0.6	V
	PSM active	V_{PSM}	2.0			V

Example: reference divider factor = 35, f_{REF} = 17.92 MHz, charge-pump current = 200 µA

Gain Control Charateristics

Operating conditions: V_{CC} = 8.5 V, T_{amb} = 27°C, f_{RF} = 1490 MHz, F_{LO} = 1261.568 MHz

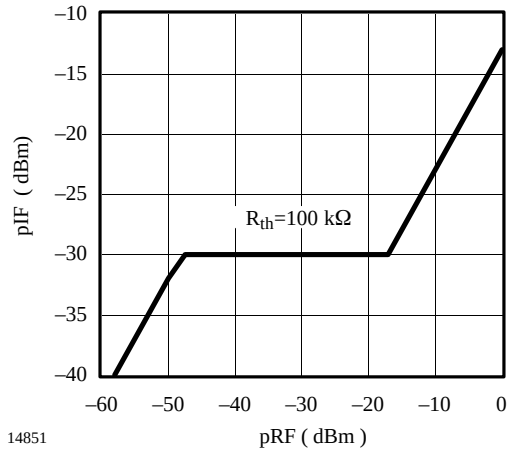


Figure 3. IF output power (Pin 19)

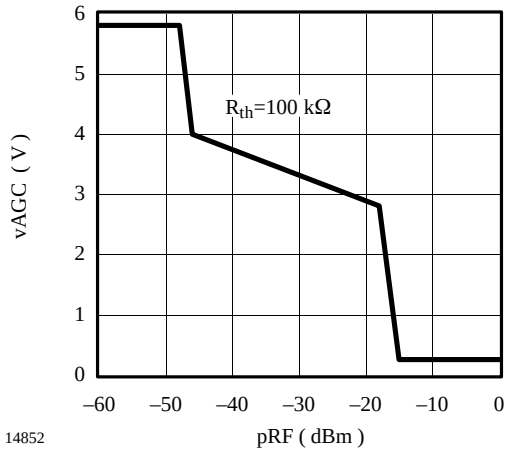


Figure 4. Gain control voltage (Pin 11)

Phase-Noise Performance

Measurement conditions: Values aquired at Pin 19 with HP 70000 spectrum analyzer. RF input (Pin 26) is blocked with 100 pF to GND. A low phase-noise signal generator (Marconi 2042) was taken as PLL reference.

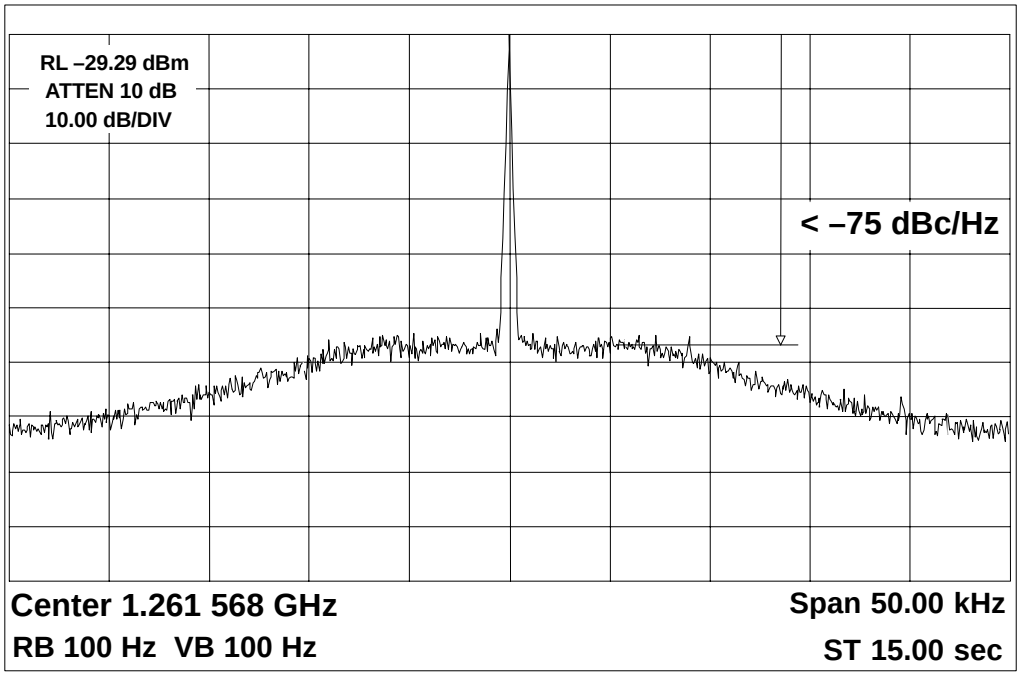


Figure 5. Phase noise performance
Operating conditions: f_{REF} = 17.92 MHz, –10dB, I_{PD} = 200µA

Equivalent Circuits

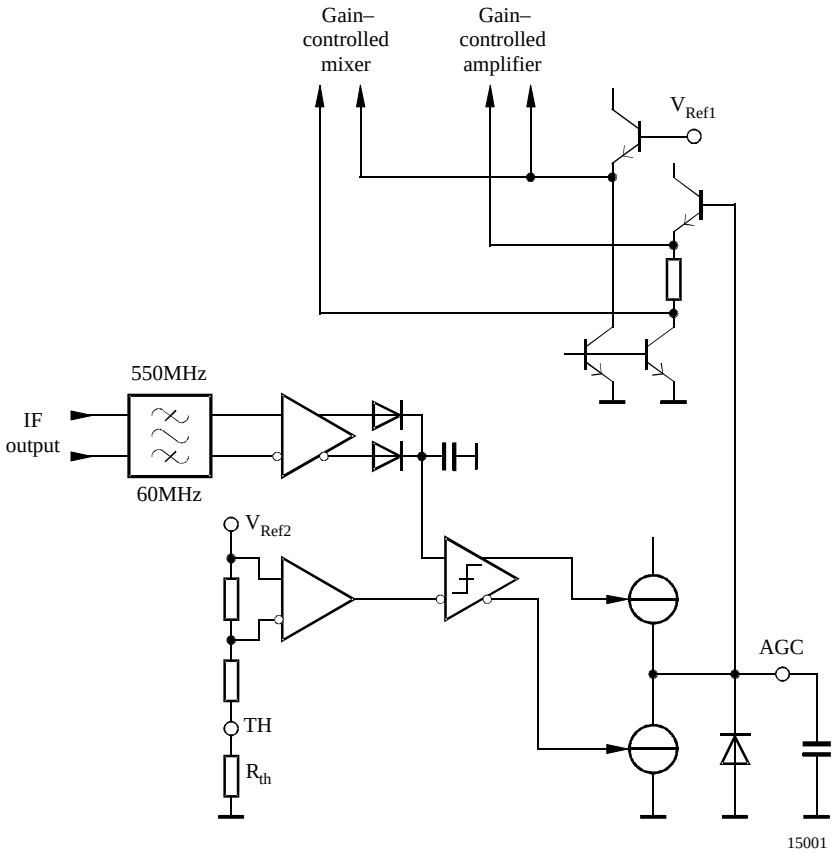
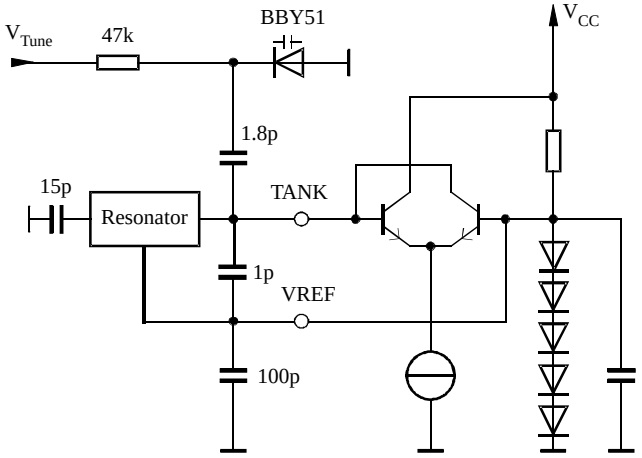


Figure 6. AGC contol circuit



Resonator: Ceramic coaxial resonator
Murata 3 x 3 mm, 1.6 GHz
DRR030 KE1R600TC

Figure 7. VCO circuit

Application Circuit

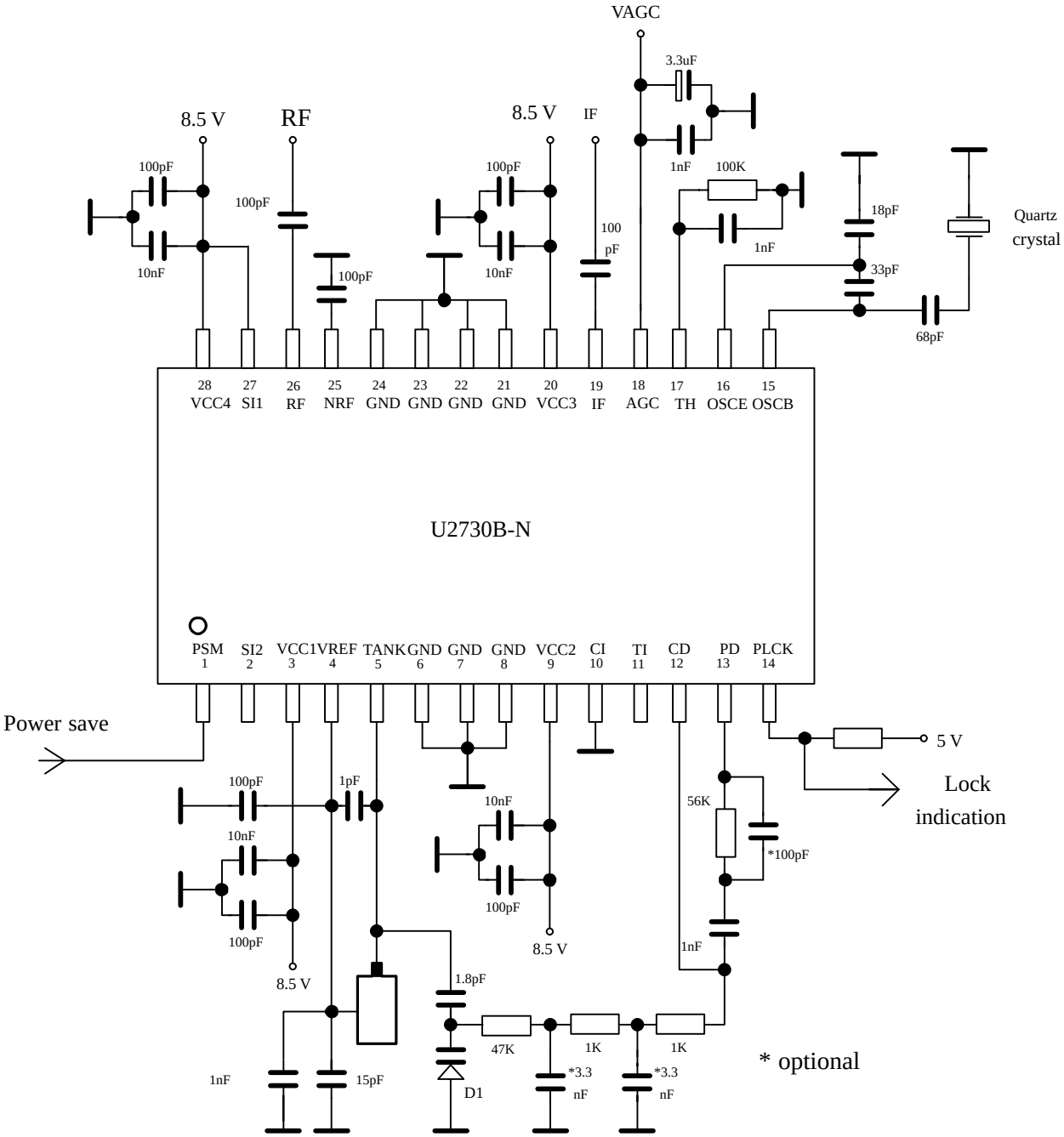


Figure 8. Application circuit

Application Circuit for External LO Signal

With an external LO signal it is possible to overdrive the VCO. In this case, the internal VCO acts as an LO buffer.

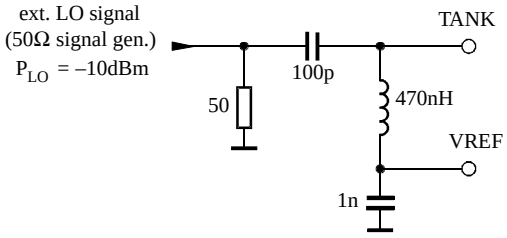


Figure 9. Application circuit for external LO signal

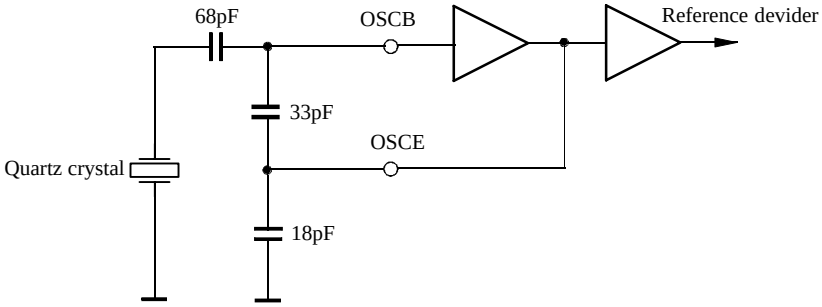


Figure 10. Reference oscillator operation

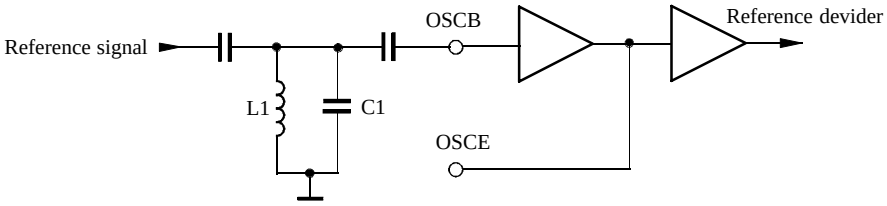
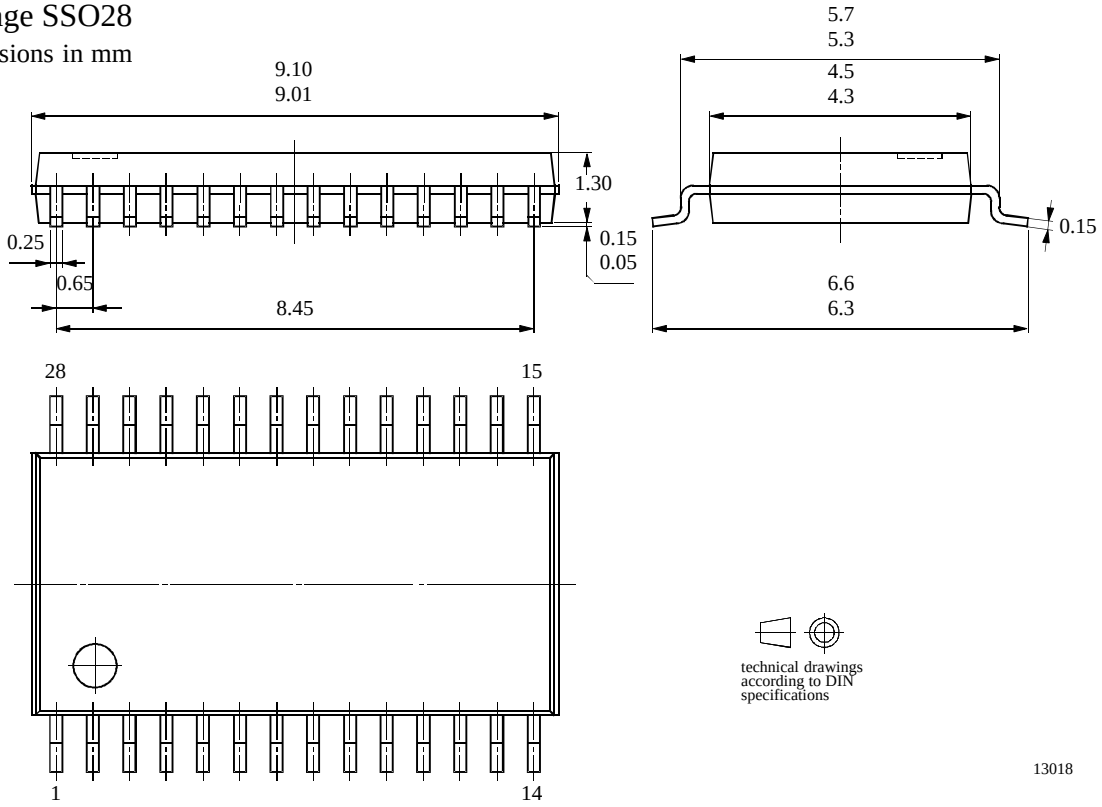


Figure 11. Reference oscillator overdriven

Package Information

Package SSO28
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.temic–semi.com

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