LINEAR TECHNOLOGY

Dual High Efficiency Step-Down Switching Regulator Controller

FEATURES

- **Dual Outputs: 3.3V and 5.0V**
- **Very High Efficiency: Over 95% Possible**
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over 3 Decades of Output Current
- Low Standby Current at Light Loads: 160μA/Output
- Independent Micropower Shutdown: $I_Q < 40$μA
- Wide V_{IN} Range: 4V to 16V
- Very Low Dropout Operation: 100% Duty Cycle
- Available in Narrow 16-Pin SOIC Package

APPLICATIONS

- Notebook and Palmtop Computers
- Battery-Operated Digital Devices
- Portable Instruments
- DC Power Distribution Systems

DESCRIPTION

The LTC1143 is a dual step-down switching regulator controller featuring automatic **Burst Mode**™ operation to maintain high efficiencies at low output currents. This device is composed of two separate regulator blocks, each driving an external power MOSFET at switching frequencies exceeding 400kHz using a constant off-time current mode architecture providing constant ripple current in the inductor.

The operating current level for both regulators is user-programmable via an external current sense resistor. Wide input supply range allows operation from 4V to 14V (16V maximum). Constant off-time architecture provides low dropout regulation limited only by the $R_{DS(ON)}$ of the external MOSFET and resistance of the inductor and current sense resistor.

The LTC1143 is ideal for applications requiring dual output voltages with high conversion efficiencies over a wide load current range in a small amount of board space.

Burst Mode is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION
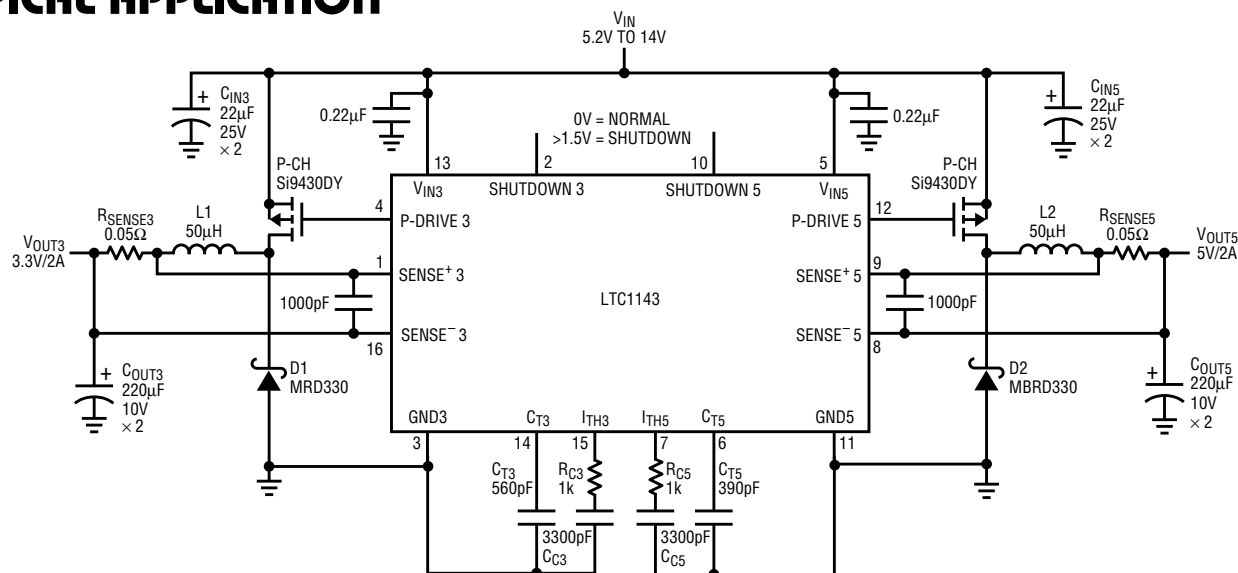
R_{SENSE3}, R_{SENSE5}: KRL SL-1/2-CI-0R050J
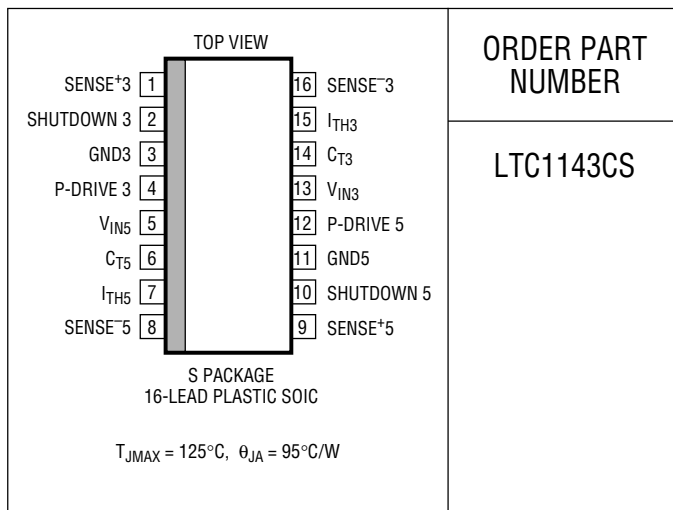L1: COILTRONICS CTX50-2-MP
L2: COILTRONICS CTX50-2-MP

NOTE: COMPONENTS OPTIMIZED FOR HIGHEST EFFICIENCY, NOT MINIMUM BOARD SPACE.

Figure 1. High Efficiency Dual 3.3V/5V

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ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pins 5,13) .... 16V to –0.3V
Continuous Output Current (Pins 4,12) 50mA
Sense Voltages (Pins 1, 8, 9, 16) .... 13V to –0.3V
Operating Ambient Temperature Range .... 0°C to 70°C
Extended Commercial
    Temperature Range .... –40°C to 85°C
Junction Temperature (Note 1) .... 125°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

SENSE$^+$3	1	16 SENSE$^-$3
SHUTDOWN 3	2	15 I$_{TH3}$
GND3	3	14 C$_{T3}$
P-DRIVE 3	4	13 V$_{IN3}$
V$_{IN5}$	5	12 P-DRIVE 5
C$_{T5}$	6	11 GND5
I$_{TH5}$	7	10 SHUTDOWN 5
SENSE$^-$5	8	9 SENSE$^+$5

S PACKAGE
16-LEAD PLASTIC SOIC

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART
NUMBER

LTC1143CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN3} = V_{IN5} = 10V, V_2 = V_{10} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS

V$_{OUT}$	Regulated Output Voltage
	  3.3V Output
	  5V Output
		V$_{IN3}$, V$_{IN5}$ = 9V
		  I$_{LOAD}$ = 700mA
		  I$_{LOAD}$ = 700mA
			●
			●
			●
				
				3.23
				4.90
					
					3.33
					5.05
						
						3.43
						5.20
							
							V
							V

ΔV$_{OUT}$	Output Voltage Line Regulation	V$_{IN3}$, V$_{IN5}$ = 7V to 12V, I$_{LOAD}$ = 50mA		–40	0	40	mV

ΔV$_{OUT}$	Output Voltage Load Regulation
	  3.3V Output
	  5V Output
		Figure 1 Circuit
		  5mA < I$_{LOAD}$ < 2.0A
		  5mA < I$_{LOAD}$ < 2.0A
			●
			●
					
					40
					60
						
						65
						100
							
							mV
							mV

ΔV$_{OUT}$	Output Ripple (Burst Mode)	I$_{LOAD}$ = 0A			50		mV$_{P-P}$

I$_5$, I$_{13}$	Input DC Supply Current (Note 2)
	  Normal Mode
	  Sleep Mode
	  Shutdown
		
		4V < V$_{IN3}$, V$_{IN5}$ < 12V
		4V < V$_{IN3}$ < 12V, 6V < V$_{IN5}$ < 12V
		V$_2$ = V$_{10}$ = 2.1V, 4V < V$_{IN3}$, V$_{IN5}$ < 12V
					
					1.6
					160
					10
						
						2.1
						230
						20
							
							mA
							µA
							µA

V$_1$ to V$_{16}$
 	
V$_8$ to V$_9$
	Current-Sense Threshold Voltage
	  3.3V Section
	
	  5V Section
		
		V$_{16}$ = V$_{OUT}$ + 100mV (Forced)
		V$_{16}$ = V$_{OUT}$ – 100mV (Forced)
		V$_8$ = V$_{OUT}$ + 100mV (Forced)
		V$_8$ = V$_{OUT}$ – 100mV (Forced)
			
			●
			
			●
				
				130
				
				130
					
					25
					150
					25
					150
						
						170
						
						170
							
							mV
							mV
							mV
							mV

V$_2$, V$_{10}$	Shutdown Pin Threshold			0.6	0.8	2	V
I$_2$, I$_{10}$	Shutdown Pin Input Current	0V < V$_{SHUTDOWN}$ = < 8V, V$_{IN3}$, V$_{IN5}$ = 16V			1.2	5	µA
I$_6$, I$_{14}$	C$_T$ Pin Discharge Current	V$_{OUT}$ in Regulation, V$_{SENSE-}$ = V$_{OUT}$ V$_{OUT}$ = 0V		50	70 2	90 10	µA µA
t$_{OFF}$	Off-Time (Note 3)	C$_T$ = 390pF, I$_{LOAD}$ = 700mA	●	4	5	6	µs
t$_r$, t$_f$	Driver Output Transition Times	C$_L$ = 3000pF (Pins 4, 12), V$_{IN}$ = 6V			100	200	ns

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ELECTRICAL CHARACTERISTICS $-40°C \leq T_A \leq 85°C$ (Note 4), $V_{IN3} = V_{IN5} = 10V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT}	Regulated Output Voltage	$V_{IN3}, V_{IN5} = 9V$				
	3.3V Output	$I_{LOAD} = 700mA$	3.17	3.33	3.4	V
	5V Output	$I_{LOAD} = 700mA$	4.85	5.05	5.2	V
I_5, I_{13}	Input DC Supply Current (Note 2)					
	Normal Mode	$4V < V_{IN3}, V_{IN5} < 12V$		1.6	2.4	mA
	Sleep Mode	$4V < V_{IN3}, V_{IN5} < 12V$		160	260	µA
	Shutdown	$V_2 = V_{10} = 2.1V, 4V < V_{IN3}, V_{IN5} < 12V$		10	22	µA
V_1 to V_{16}	Current Sense Threshold Voltage					
	3.3V Section	$V_{16} = V_{OUT} + 100mV$ (Forced)		25		mV
		$V_{16} = V_{OUT} - 100mV$ (Forced)	125	150	175	mV
V_8 to V_9	5V Section	$V_8 = V_{OUT} + 100mV$ (Forced)		25		mV
		$V_8 = V_{OUT} - 100mV$ (Forced)	125	150	175	mV
V_2, V_{10}	Shutdown Pin Threshold		0.55	0.8	2	V
t_{OFF}	Off-Time (Note 3)	$C_T = 390pF$, $I_{LOAD} = 700mA$	3.8	5	6	µs

The ● denotes specifications which apply over the operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

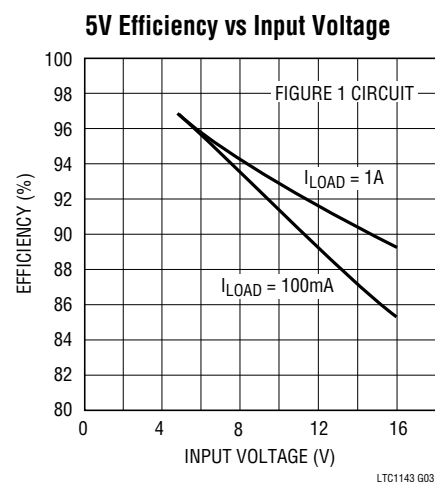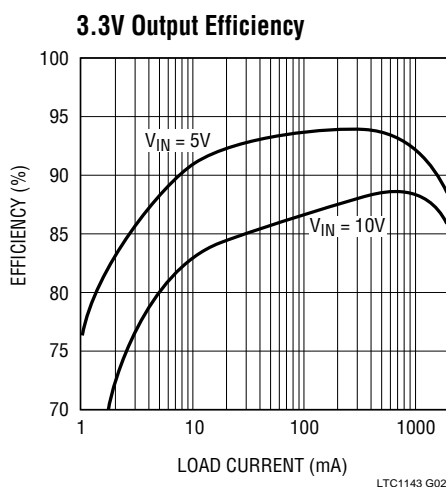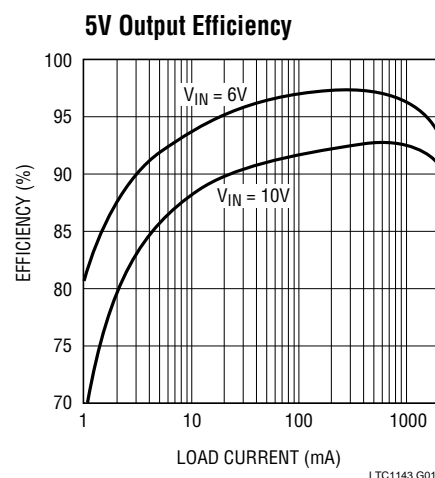LTC1143CS: $T_J = T_A + (P_D \times 120°C/W)$

Note 2: This supply current is for one regulator block. Total supply current is the sum of pin 5 and pin 13 currents. Dynamic supply current

is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 3: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.
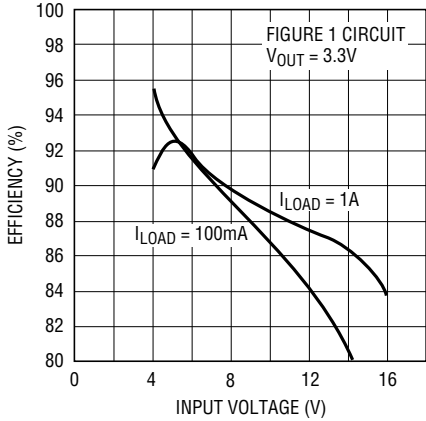
Note 4: The LTC1143 is not tested and quality assurance sampled at $-40°C$ to $85°C$. These specifications are guaranteed by design and/or correlation.
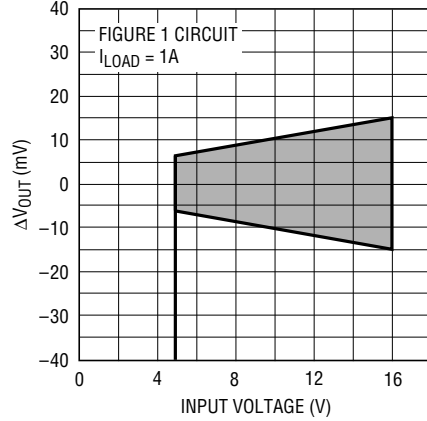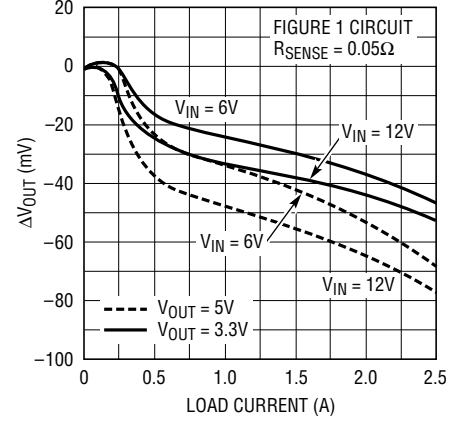
TYPICAL PERFORMANCE CHARACTERISTICS

5V Output Efficiency

LTC1143 G01

3.3V Output Efficiency

LTC1143 G02

5V Efficiency vs Input Voltage

LTC1143 G03

TYPICAL PERFORMANCE CHARACTERISTICS

3.3V Efficiency vs Input Voltage

LTC1143 G04

Line Regulation

LTC1143 G05

Load Regulation

LTC1143 G06

DC Supply Current

LTC1143 • G07
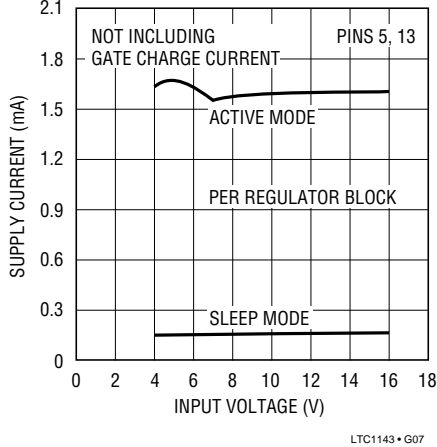
Supply Current in Shutdown

LTC1143 G08
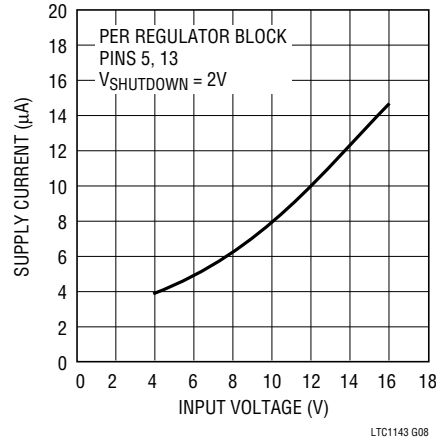
Operating Frequency vs $V_{IN} - V_{OUT}$

LTC1143 G09
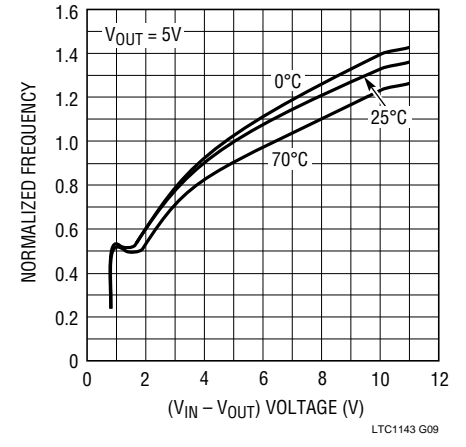
Gate Charge Supply Current

LTC1143 G10

Off-Time vs V_{OUT}

LTC1143 G11

Current Sense Threshold Voltage

LTC1143 G12
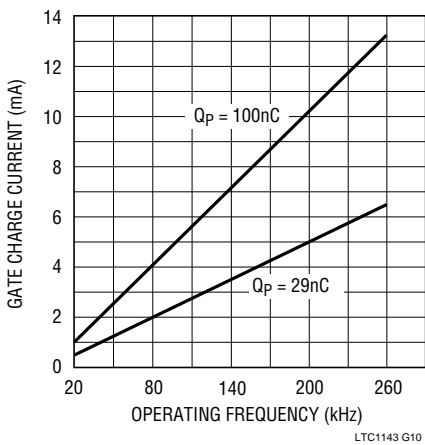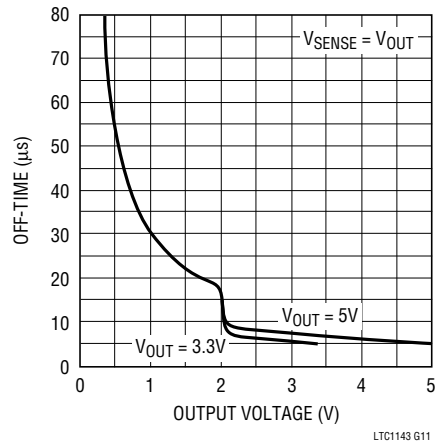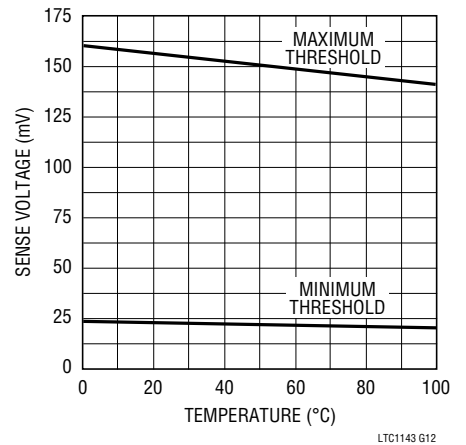
PIN FUNCTIONS

SENSE+3 (Pin 1): The (+) Input to the 3.3V Section Current Comparator. A built in offset between pins 1 and 16 in conjunction with $R_{SENSE\,3}$ sets the current trip threshold for the 3.3V section.

SHUTDOWN 3 (Pin 2): When grounded, the 3.3V section operates normally. Pulling pin 2 high holds the MOSFET off and puts the 3.3V section in micropower shutdown mode. Requires CMOS logic level signal with t_r, $t_f < 1\mu s$. Do not "float" pin 2.

GND3 (Pin 3): 3.3V Section Ground. Two independent ground lines must be routed separately from other grounds to: 1) the (–) terminal of the 3.3V section output capacitor, and 2) the cathode of the Schottky diode D1 and (–) terminal of C_{IN3} (See Figures 1 and 9).

P-DRIVE 3 (Pin 4): High Current Drive for Top P-Channel MOSFET, 3.3V Section. Voltage swing at this pin is from V_{IN3} to ground.

V$_{IN5}$ (Pin 5): Supply Pin, 5V Section. Must be closely decoupled to 5V power ground pin 11.

C$_{T5}$ (Pin 6): External capacitor C_{T5} from pin 6 to ground sets the operating frequency for the 5V section. (The actual frequency is also dependent upon the input voltage.)

I$_{TH5}$ (Pin 7): Gain Amplifier Decoupling Point, 5V Section. The 5V section current comparator threshold increases with the pin 7 voltage.

SENSE– 5 (Pin 8): Connects to internal resistive divider which sets the output voltage for the 5V section. Pin 8 is also the (–) input for the current comparator on the 5V section.

SENSE+ 5 (Pin 9): The (+) Input to the 5V Section Current Comparator. A built-in offset between pins 9 and 8 in conjunction with $R_{SENSE\,5}$ sets the current trip threshold for the 5V section.

SHUTDOWN 5 (Pin 10): When grounded, the 5V section operates normally. Pulling pin 10 high holds the 5V section MOSFET off and puts the 5V section in micropower shutdown mode. Requires CMOS logic level signal with t_r, $t_f < 1\mu s$. Do not "float" pin 10.

GND5 (Pin 11): 5V Section Ground. Two independent ground lines must be routed separately from other grounds to: 1) the (–) terminal of the 5V section output capacitor, and 2) the cathode of the Schottky diode D2 and (–) terminal of C_{IN5} (See Figures 1 and 9).

P-DRIVE 5 (Pin 12): High Current Drive for Top P-Channel MOSFET, 5V Section. Voltage swing at this pin is from V_{IN5} to ground.

V$_{IN3}$ (Pin 13): Supply Pin, 3.3V Section. Must be closely decoupled to 3.3V power ground pin 3.

C$_{T3}$ (Pin 14): External capacitor C_{T3} from pin 14 to ground sets the operating frequency for the 3.3V section. (The actual frequency is also dependent upon the input voltage.)

I$_{TH3}$ (Pin 15): Gain Amplifier Decoupling Point, 3.3V Section. The 3.3V section current comparator threshold increases with the pin 15 voltage.

SENSE– 3 (Pin 16): Connects to internal resistive divider which sets the output voltage for the 3.3V section. Pin 16 is also the (–) input for the current comparator on the 3.3V section.

FUNCTIONAL DIAGRAM

Only one regulator block shown. Pin numbers are for 3.3V (5V) sections.
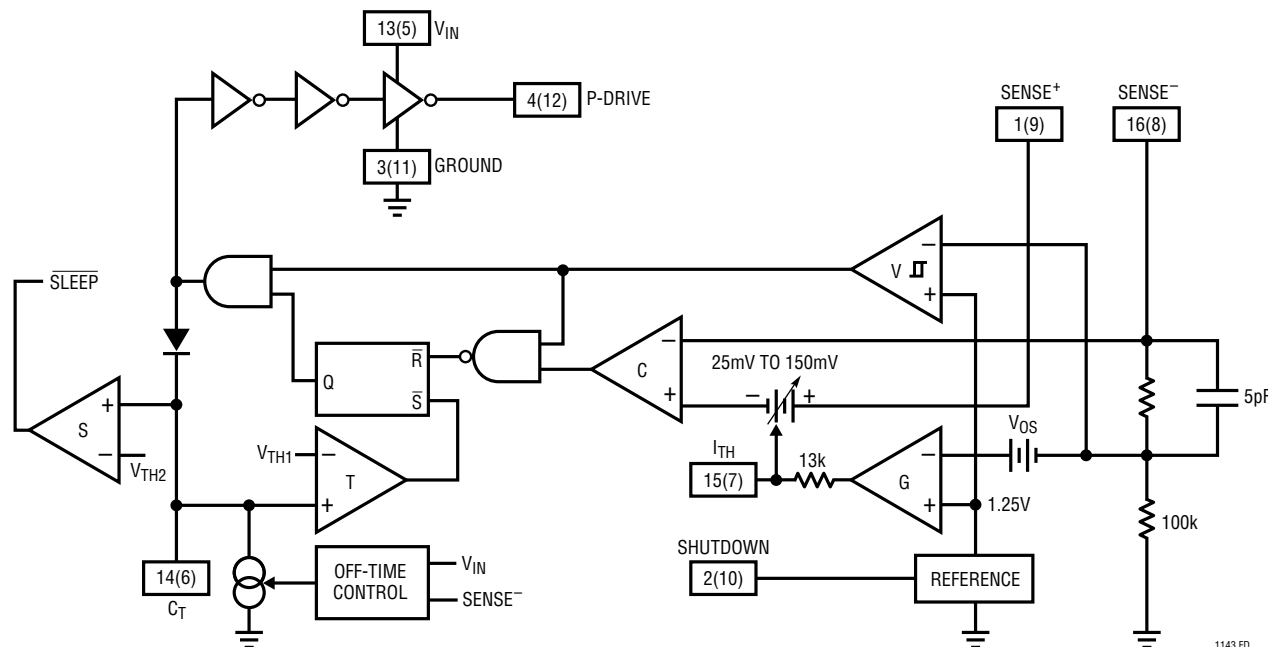
OPERATION   Refer to Functional Diagram and Figure 1.

The LTC1143 consists of two individual regulator blocks each using current mode, constant off-time architectures to switch an external power MOSFET. The two regulators are internally set to provide output voltages of 3.3V and 5V. Operating frequency is individually set on each section by external capacitors at the timing capacitor pins 6 and 14.

The output voltage is sensed by an internal voltage divider connected to Sense⁻ pin 16 (8). A voltage comparator V and a gain block G compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1143 automatically switches between two modes of operation, burst and continuous. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between pins 1 (9) and 16 (8) connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-drive output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor connected to pin 14 (6) is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage [measured by pin 16 (8)] to model the inductor current, which decays at a rate which is also proportional to the output voltage.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the P-drive output to go low turning the P-channel MOSFET back on. The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage [pin 15 (7)] to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal sleep line to go low.

The circuit now enters sleep mode with the power MOSFET turned off. In sleep mode a majority of the circuitry is

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OPERATION   *Refer to Functional Diagram and Figure 1*

turned off, dropping the quiescent current from 1.6mA to 160µA (for one regulator block). The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and the process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset (V_{OS}) is incorporated in the gain stage. This prevents the current compara-

tor threshold from increasing until the output voltage has dropped below a minimum threshold.

Using constant off-time architecture the operating frequency is a function of the input voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 1.5V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle), providing extremely low dropout operation.

APPLICATIONS INFORMATION

The basic LTC1143 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFET and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. Since the 3.3V and 5V sections are identical, the process of component selection is the same for both sections. The circuit shown in Figure 1 can be configured for operation up to an input voltage of 16V.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1143 current comparators have a threshold range which extends from a minimum of 25mV/R_{SENSE} to a maximum of 150mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE}. (See C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1143 and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

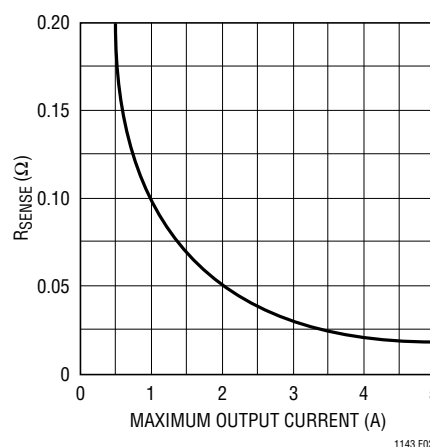A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2.

Figure 2. Selecting R_{SENSE}

The load current below which Burst Mode operation commences, I_{BURST}, and the peak short circuit current, $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

The LTC1143 automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

APPLICATIONS INFORMATION

L and C_T Selection for Operating Frequency

Each regulator section of LTC1143 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the P-channel MOSFET switch turns on the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{1}{1.3 \times 10^4 \times f} \left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D} \right)$$

Where V_D is the drop across the diode.

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.
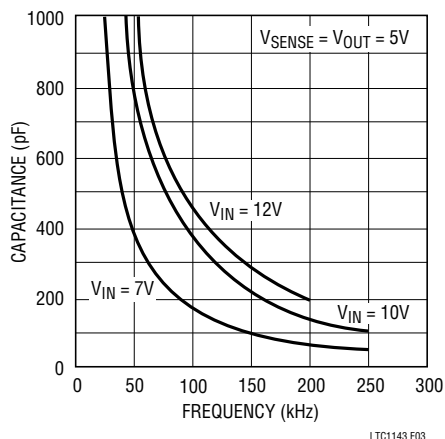

Figure 3. Timing Capacitor Value

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency of the circuit in Figure 1 is given by:

$$f = \frac{1}{t_{OFF}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T \times \left(\frac{V_{REG}}{V_{OUT}} \right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus $V_{REG}/V_{OUT} = 1$ in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input to output voltage differential drops below 1.5V for a particular section, the LTC1143 reduces t_{OFF} in that section by increasing the discharge current in C_T. This prevents audible operation prior to dropout.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than $25mV/R_{SENSE}$ of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used the inductor current will become discontinuous before the LTC1143 enters Burst Mode operation. A consequence of this is that the LTC1143 will delay entering Burst Mode operation and efficiency will be degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. The highest efficiency will be obtained using Ferrite, Kool Mµ® or Molypermalloy (MPP) cores. Lower cost powdered iron cores provide suitable performance, but cut efficiency by 3% to 7%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation.

Kool Mµ is a registered trademark of Magnetics, Inc.

APPLICATIONS INFORMATION

Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered. Do not allow the core to saturate!

Kool Mμ (from Magnetics, Inc.) is a very good, low loss core material for toroids with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (> 200 kHz) switching frequencies but quite a bit more expensive. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available from Coiltronics and Beckman Industrial Corporation which do not increase the height significantly.

Power MOSFET Selection

An external power MOSFET must be selected for use with each section of the LTC1143. The main selection criteria for the power MOSFETs are the threshold voltage $V_{GS(TH)}$ and on resistance $R_{DS(ON)}$.

The minimum input voltage determines whether a standard threshold or logic-level threshold MOSFET must be used. For $V_{IN} > 8V$, standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. If V_{IN} is expected to drop below 8V, logic-level threshold MOSFETs ($V_{GS(TH)} < 2.5V$) are strongly recommended. When logic-level MOSFETs are used, the LTC1143 supply voltage must be less than the absolute maximum V_{GS} ratings for the MOSFET.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the two MOSFETs. When the LTC1143 is operating in continuous mode, the simplifying assumption can be made that either the MOSFET or Schottky diode is always conducting the average load current. The duty cycles for the MOSFET and diode are given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Schottky Diode Duty Cycle} = \frac{(V_{IN} - V_{OUT} + V_D)}{V_{IN}}$$

From the duty cycles the required $R_{DS(ON)}$ for each MOSFET can be derived:

$$\text{P-Ch } R_{DS(ON)} = \frac{V_{IN} \times P_P}{V_{OUT} \times I_{MAX}^2 \times (1 + \delta_P)}$$

where P_P is the allowable power dissipation and δ_P is the temperature dependencies of $R_{DS(ON)}$. P_P will be determined by efficiency and/or thermal requirements (see Efficiency Considerations). $(1+d)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs. temperature curve, but $\delta = 0.007/°C$ can be used as an approximation for low voltage MOSFETs.

Output Diode Selection (D1, D2)

The Schottky diodes D1 and D2 shown in Figure 1 conduct during the off-time. It is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

The most stressful condition for the output diode is under short circuit ($V_{OUT}=0$). Under this condition the diode must safely handle $I_{SC(PK)}$ at close to 100% duty cycle. Under normal load conditions the average current conducted by the diode is:

$$I_{DIODE} = \frac{(V_{IN} - V_{OUT} + V_D)}{V_{IN}}(I_{LOAD})$$

Remember to keep lead lengths short and observe proper grounding (see Board Layout Checklist) to avoid ringing and increased dissipation.

The forward voltage drop allowable in the diode is calculated from the maximum short circuit current as:

$$V_F \approx \frac{P_D}{I_{SC(PK)}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements (see Efficiency Considerations).

APPLICATIONS INFORMATION

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question. An additional 0.1µF to 1µF ceramic capacitor is also required on each V_{IN} line (pin 5, pin 13) for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1143:*

C_{OUT} required ESR < 2R_{SENSE}

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$ the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon and United Chemicon, should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available

from Sanyo has the lowest ESR size/ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be parallel to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, (2) AVX 100µF/10V (P/N TPSD 107K010) could be used. Consult the manufacturer for other specific recommendations.
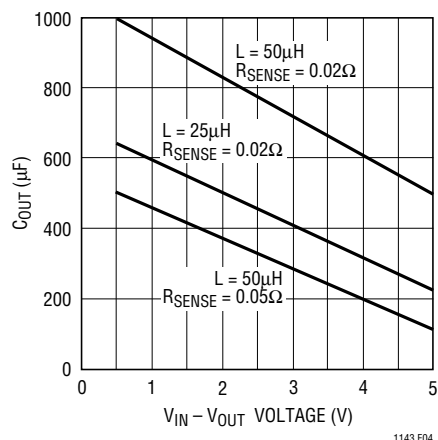

Figure 4. Minimum Value of C_{OUT}

At low supply voltages a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1143 would normally be in continuous operation. The output remains in regulation at all times.

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Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The pin 15(7) external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT} causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \times C_{LOAD}$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

   %Efficiency = 100% − (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power. (For high efficiency circuits only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1143 circuits:

   1) LTC1143 DC bias current

   2) MOSFET gate charge current
   3) I^2R losses
   4) Voltage drop of the Schottky diode.

1) The DC supply current is the current which flows into V_{IN} (pin 13 for the 3.3V section, pin 5 for the 5V section) less the gate charge current. For $V_{IN} = 10V$ the LTC1143 DC supply current for each section is 160µA for no load, and increases proportionally with load up to a constant 1.6mA after the LTC1143 has entered continuous mode. Because the DC bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN}=10V the DC bias losses are generally less than 1% for load currents over 30mA. However at very low load currents the DC bias current accounts for nearly all of the loss.

2) MOSFET gate charge current results from switching the gate capacitance of the power MOSFET. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f(Q_P)$. The typical gate charge for a 125mΩ P-channel power MOSFET is 40nC. This results in $I_{GATECHG} = 4mA$ in 100kHz continuous operation, for a 2% to 3% typical mid-current loss with $V_{IN} = 10V$.

Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using a larger MOSFET than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3) I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the P-channel MOSFET and Schottky diode. The MOSFET $R_{DS(ON)}$ multiplied by the P-channel duty cycle can be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if the $R_{DS(ON)} = 0.1Ω$, $R_L = 0.15Ω$, and $R_{SENSE} = 0.05Ω$, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 10% as the output

APPLICATIONS INFORMATION

current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.

4) The Schottky diode is a major source of power loss at high currents and gets worse at high input voltages. The diode loss is calculated by multiplying the forward voltage drop times the Schottky diode duty cycle multiplied by the load current. For example, assuming a duty cycle of 50% with a Schottky diode forward voltage drop of 0.4V, the loss increases from 0.5% to 8% as the load current increases from 0.5A to 2A. If Schotky diode losses routinely exceed 5% consider using the synchronously switched LTC1142.

Figure 5 shows how the efficiency losses in one section of a typical LTC1143 regulator end up being apportioned. The gate charge loss is responsible for the majority of the efficiency lost in the mid-current region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to unacceptable levels. With Burst Mode operation, the DC supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected, the I^2R losses and Schottky diode loss dominate at high load currents.
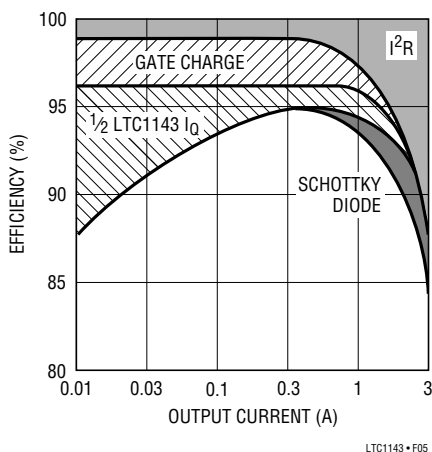

Figure 5. Efficiency Loss

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, and inductor core losses, generally account for less than 2% total additional loss.

Design Example

As a design example, assume V_{IN} = 12V(nominal), 5V section, I_{MAX} = 2A, and f = 200kHz, R_{SENSE}, C_T, and L can immediately be calculated:

R_{SENSE5} = 100mV / 2 = 0.05Ω

t_{OFF} = (1/200kHz) $\times$ [1 – (5/12)] = 2.92μs

C_{T5} = 2.92μs/(1.3 $\times$ 10^4) = 220pF

$L2_{MIN}$ = 5.1 $\times$ 10^5 $\times$ 0.05Ω $\times$ 220pF $\times$ 5V = 28μH

Assume that the MOSFET dissipation is to be limited to P_P = 250mW.

If T_A = 50°C and the thermal resistance of the MOSFET is 50°C/W, then the junction temperatures will be 63°C and $\delta_P = \delta_N$ = 0.007(63-25) = 0.27. The required $R_{DS(ON)}$ for the MOSFET can now be calculated:

$$\text{P-Ch } R_{DS(ON)} = \frac{12(0.25)}{5(2)^2 \ (1.27)} = 0.12\Omega$$

The P-channel requirement can be met by a Si9430DY. Note that the most stringent requirement for the Schottky diode is with V_{OUT} = 0 (i.e. short circuit). During a continuous short circuit, the worst case Schottky diode dissipation rises to:

$$P_D = I_{SC(AVG)} \times V_D \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

With the 0.05Ω sense resistor $I_{SC(AVG)}$ = 2A will result, increasing the 0.4V Schottky diode dissipation to 0.8W.

C_{IN} will require an RMS current rating of at least 1A at temperature, and C_{OUT} will require an ESR of 0.05Ω for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. At lower input voltages the operating frequency will decrease and the P-channel will be conducting most of the time causing its power dissipation to increase. At $V_{IN(MIN)}$ = 7V, the frequency shifts to 49kHz and the P-channel power dissipation increases to 435mW. Check to assure the maximum temperature of the P-channel is not exceeded.

APPLICATIONS INFORMATION

Troubleshooting Hints

Since efficiency is critical to LTC1143 applications it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the timing capacitor pin 14 and pin 6.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 7a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 7b.

If pin 14 or pin 6 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.
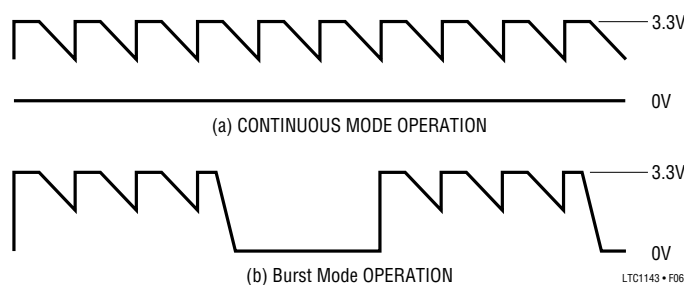

(a) CONTINUOUS MODE OPERATION

(b) Burst Mode OPERATION

Figure 7. C_T Waveforms

Auxiliary Windings—Suppressing Burst Mode Operation

The LTC1143 being a nonsynchronous switch has the normal limitation that the power drawn from the inductor primary winding must not be less than twice the power drawn from the auxiliary windings. (With synchronous switching, using the LTC1142, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.)

Burst Mode operation can be suppressed at low output currents with a simple external network which cancels the 25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from

certain types of inductors in high current ($I_{OUT} > 5A$) applications when they are lightly loaded.

An external offset is put in series with the Sense⁻ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 8. Two 100Ω resistors are inserted in series with the sense leads from the sense resistor.
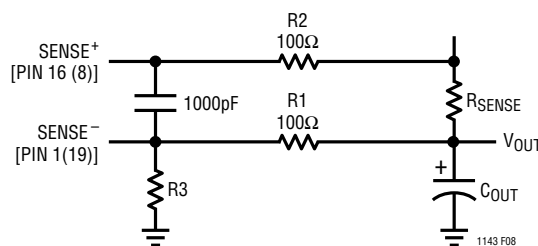

Figure 8. Suppression of Burst Mode Operation

With the addition of R3 a current is generated though R1 causing an offset of:

$$V_{OFFSET} = V_{OUT} \times \left(\frac{R1}{R1 + R3}\right)$$

If $V_{OFFSET} > 25mV$, the built-in offset will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be lower:

$$R_{SENSE} \approx \frac{75mV}{I_{MAX}}$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across pins 1 (16) and 9 (8).

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1143. These items are also illustrated graphically in the layout diagram of Figure 9. In general each block

APPLICATIONS INFORMATION

should be self-contained with little cross coupling for best performance. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC1143 ground pin 3 (11) must return separately to: a) the power, and b) the signal grounds. The power ground returns to the anode of the Schottky diode and (–) plate of C_{IN}, which should have as short lead lengths as possible. The signal ground (b) connects to the (–) plate of C_{OUT}.

2) Does the LTC1143 Sense⁻ pin 16 (8) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}?

3) Are the Sense⁻ and Sense⁺ leads routed together with minimum PC trace spacing? The 1000pF capacitor

between pins 1 (9) and 16 (8) should be as close as possible to the LTC1143.

4) Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? This capacitor provides the AC current to the P-Channel MOSFET.

5) Is the V_{IN} decoupling capacitor (1μF, 0.1μF) connected closely between pin 13 (5) and ground pin 3 (11)? This capacitor carries the MOSFET driver peak currents.

6) Are the Shutdown pins 2 and 10 actively pulled to ground during normal operation? Both shutdown pins are high impedance and must not be allowed to float. Both pins can be driven by the same external signal if needed.
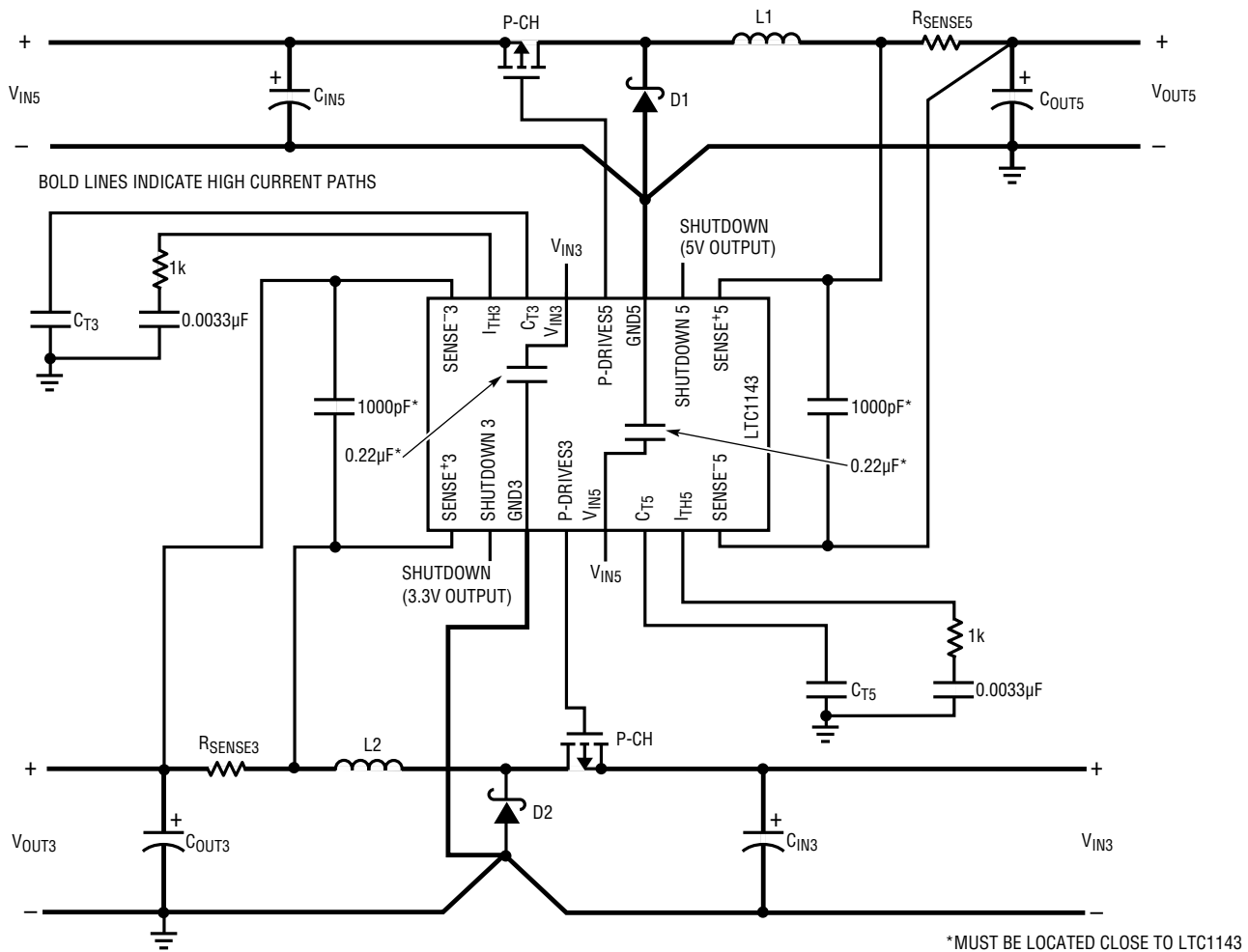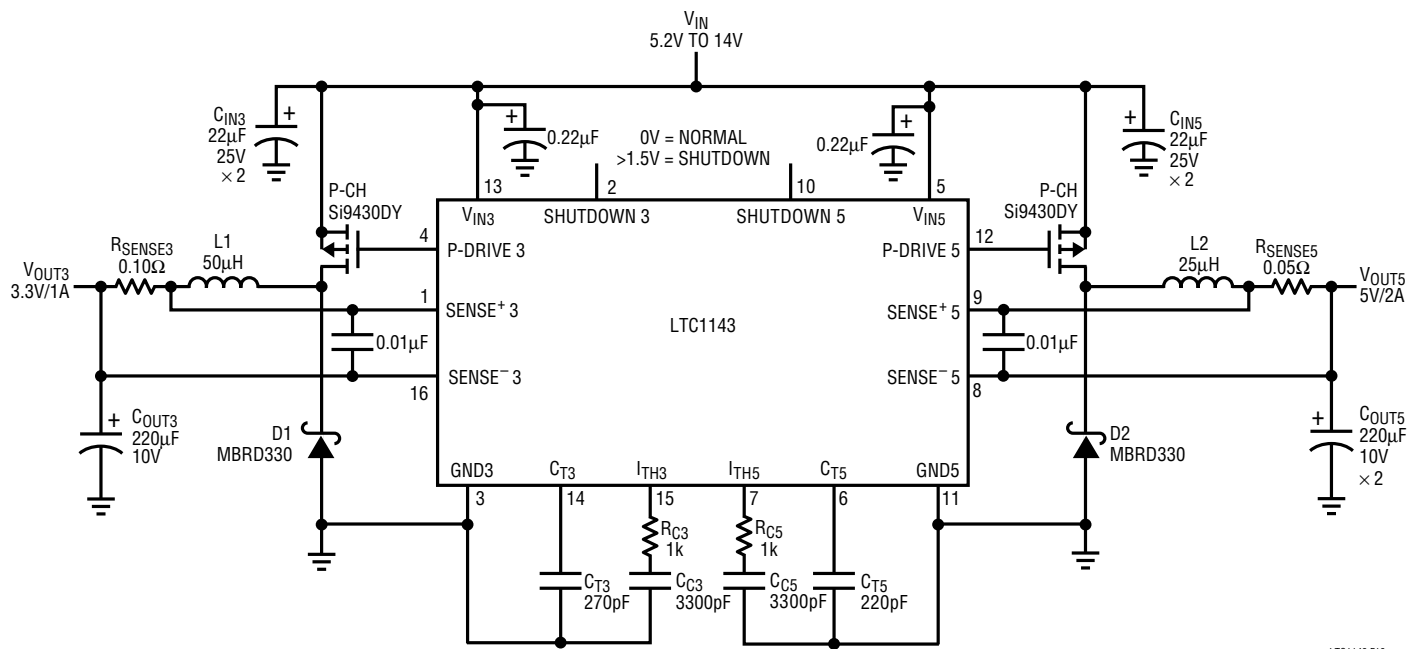

Figure 9. LTC1143 Layout Diagram (see Board Layout Checklist)
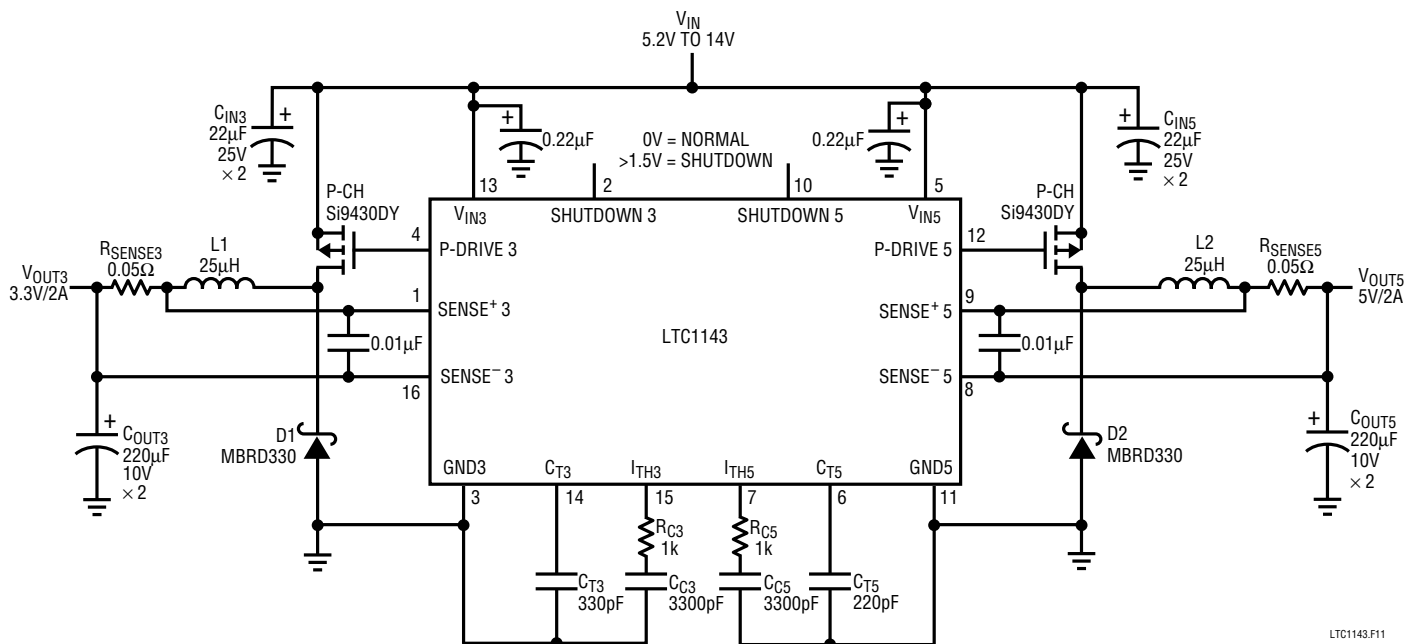
1143 F09

TYPICAL APPLICATIONS

R_{SENSE3}: IRC LR2512-01-OR100G
R_{SENSE5}: IRC LR2512-01-ORO50G

C_{IN3}, C_{IN5}: AVX (TA) TPSD226K025R0200
C_{OUT3}, C_{OUT5}: AVX (TA) TPSE227K010R0080

L2: COILTRONICS CTX50-4
L2: COILTRONICS CTX25-4

Figure 10. All Surface Mount Dual 5V/2A, 3.3V/1A Converter

R_{SENSE3}: KRL SL-1/2-C1-0R050J
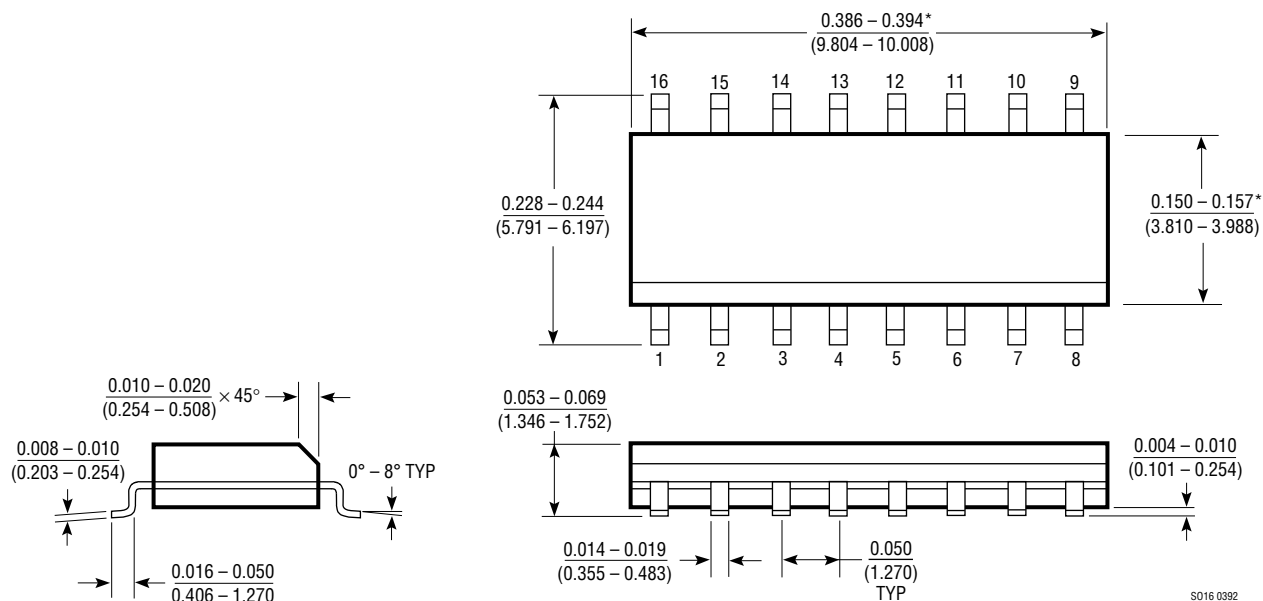R_{SENSE5}: KRL SL-1/2-C1-0R050J

C_{IN3}, C_{IN5}: AVX (TA) TPSD226K025R0200
C_{OUT3}, C_{OUT5}: AVX (TA) TPSE227K010R0080

L1: COILTRONICS CTX25-4
L2: COILTRONICS CTX25-4

Figure 11. All Surface Mount Dual 5V/2A, 3.3V/2A Converter

LTC1143

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

S16 Package
16-Lead Plastic SOIC

$$0.386 - 0.394*$$
$$(9.804 - 10.008)$$

16 15 14 13 12 11 10 9

$$0.228 - 0.244$$
$$(5.791 - 6.197)$$

$$0.150 - 0.157*$$
$$(3.810 - 3.988)$$

1 2 3 4 5 6 7 8

$$0.010 - 0.020$$
$$(0.254 - 0.508)$$ × 45°

$$0.008 - 0.010$$
$$(0.203 - 0.254)$$

0° – 8° TYP

$$0.016 - 0.050$$
$$0.406 - 1.270$$

$$0.053 - 0.069$$
$$(1.346 - 1.752)$$

$$0.004 - 0.010$$
$$(0.101 - 0.254)$$

$$0.014 - 0.019$$
$$(0.355 - 0.483)$$

$$0.050$$
$$(1.270)$$
TYP

SO16 0392

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).