PM73122

AAL1GATOR-32

REVISION A DEVICE ERRATA

PRELIMINARY

ISSUE 4: MAY 2001

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	April 2000	Document created.
2	May 2000	Added errata for SBI interrupt register reads, cell loss due to internal loopback FIFO overflows, MVIP-90 (2.8-2.10) and document clarification on SBI operation.
3	October 2000	Added errata for Non-DBCES Idle Detection, REF_VAL_ENABLE Feature for Minimizing CDV, UTOPIA Registers - Read Timing Violation, HS_GEN_DS3_AIS Does Not Cause T_COND_CELL_CNT to Increment, Bit-Count-Integrity Through Underrun, SBI Initialization Sequence and Updates to Documentation regarding SBI configuration. Added description for C1FP_ADD pin and TWO_C1FP_EN control bit.

Issue No.	Issue Date	Details of Change
4	May 2001	Corrected errata 2.5 LOW_CDV Queue Does Not Activate/Deactivate Correctly. Steps 1 to 6 removed; (a) – (f) kept. Changed errata "When RDB/CSB is Asserted 50 ns Beyond ACKB Certain SBI Interrupt Register Read Cycles Result in Corrupt Data" to read "...15 ns Beyond ACKB" instead of "…50 ns Beyond ACKB." Added errata for "Detection of Misaligned H-MVIP Sync Pulse Can Be Missed in a Certain Condition" Added errata for "Only After an Underrun Condition, the Value of the First Pointer Received is Not Verified for an Out of Range Condition or a Dummy Pointer Value" Added errata for "INSBI/EXSBI Depth Check Interrupts" Clarified errata title. Changed from "Exiting DS3/E3 UDT Loopback…" to "Exiting UDF_HS Loopback…" Added documentation clarification for "Exiting UDF_HS Loopback Mode Requires That High Speed Queue Be Reset", "SPE Activation Must Occur After Tributaries are Enabled", "INSBI RAM Register Description Correction", "EXSBI RAM Register Description Correction", "INSBI/EXSBI Depth Check Interrupt Status Registers Provide SBI Trib Number, Not Link Number", "Clarification of R_SN_CONFIG Word Format – For Fast SNP The First Cell Received Will Always be Dropped" and "Correction in "Out of Band Signaling Idle Detection" Description" Clarified the loopback description for the errata: "RATM_CLK Must be Present even when Debugging Hardware" Clarified errata: "SBI Initialization Sequence." Added errata describing the addition of SHIFT_CAS, C1FP_ADD and BUSMASTER features to devices *after* Revision A or B.

CONTENTS

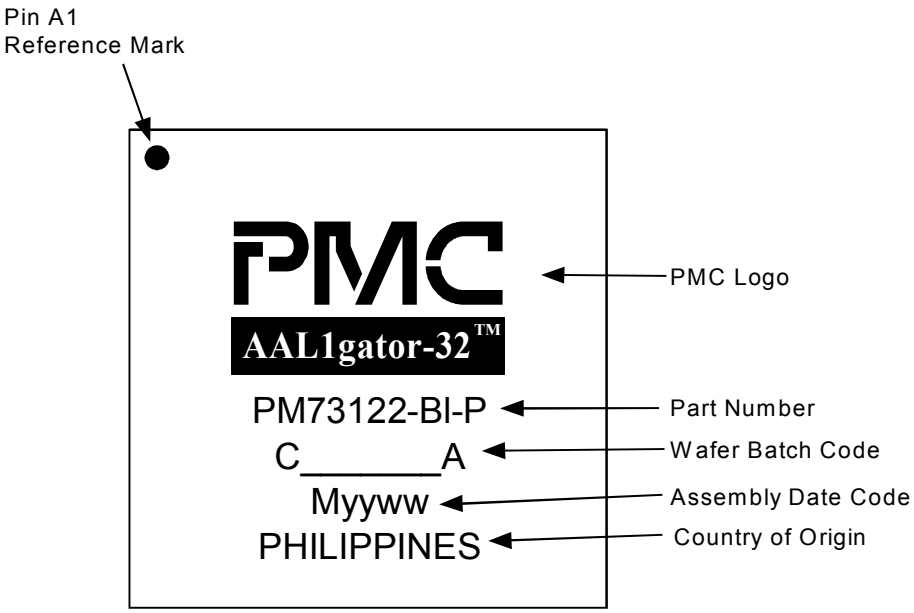
1 INTRODUCTION

This document lists the known functional errata for revision A of the PM73122 AAL1gator-32 as of the publication date of this document. This document also contains corrections and clarifications, if any, for the AAL1gator-32 Datasheet. Please refer to PMC's product web-page at www.pmc-sierra.com to check for the latest errata.

1.1 Device Identification

The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1). The PM73122 AAL1gator-32 Revision A is packaged in a 352-pin Super Enhanced Ball Grid Array (SBGA) package.

Figure 1. PM73122 AAL1gator-32 Branding Format.



1.2 Reference:

1. PMC-1981419 AAL1gator-32 Datasheet, Issue 5.

2 AAL1GATOR-32 REVISION A FUNCTIONAL DEFICIENCY LIST

This section lists the known functional deficiencies for Revision A of the AAL1gator-32 (as of the publication date of this document). For each deficiency, the known workaround is described as well as a comparison of the performance of the device with the workaround and without the workaround implemented.

Please report any functional deficiencies not covered in this document to PMC-Sierra.

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2.1 Limited Dynamic Bandwidth CES and Non-DBCES Idle Detection

2.1.1 Description

Dynamic Bandwidth CES (DBCES) and Non-DBCES Idle Detection are techniques used by the AAL1gator-32 to remove timeslots from the AAL1 structure when those timeslots are detected to be inactive. The result is a savings in network bandwidth as compared to the constant bit rate generated using AAL1 CES without DBCES.

The AAL1gator is designed to support DBCES which is compliant to the ATM Forum standard AF-VTOA-0085.000 Dynamic Bandwidth Circuit Emulation Service (DBCES). The second method, Non-DBCES Idle Detection, is proprietary.

With DBCES, when an inactive state is detected in a specific time slot, the time slot is dropped from the next ATM structure and the bandwidth it was using may be reutilized for other services.

With Non-DBCES Idle Detection, cells are transmitted when *any* of the timeslots are active. Cells are not transmitted when *all* of the constituent time slots are inactive.

There are limitations with DBCES and Non-DBCES Idle Detection. It is recommended not to use these features with Rev A AAL1gator-32.

2.1.2 Workarounds:

Don't enable DBCES or Non-DBCES Idle Detection. The AAL1gator-32 operates normally as per ATM Forum's CES Specification.

2.1.3 Performance with workaround:

The AAL1gator-32 operates normally as per ATM Forum's CES Specification.

2.1.4 Performance without workaround:

The use of DBCES and non-DBCES Idle Detection is not recommended.

2.2 Robust Sequence Number Processing Feature is not Functional

2.2.1 Description

The AAL1gator-32 is designed to support two algorithms for Sequence Number Processing (SNP): Fast Sequence Number Processing and Robust Sequence Number Processing. The Fast Sequence Number Processing feature is available in the current revision, Rev A, and functions exactly as in the PM73121 AAL1gator-II device. Robust Sequence Number Processing is not functional.

2.2.2 Workarounds:

Use Fast Sequence Number Processing, not Robust Sequence Number Processing.

2.2.3 Performance with workaround:

Fast Sequence Number Processing functions exactly as in the PM73121 AAL1gator-II device.

2.2.4 Performance without workaround:

Not applicable.

2.3 Runt Cells Can Cause Cell Errors when in Multi-Port Mode

2.3.1 Description

In the ATM-to-Line Interface direction of the AAL1gator's UTOPIA interface, a four cell deep UTOPIA FIFO is used to buffer cells for delivery to the internal AAL1 processors. In addition, each AAL1 processor is preceded with an eight cell deep AAL1 PROCESSOR FIFO.

During normal operation there may be situations where cell streams targeted to a given internal AAL1 processer may be clumped together. If the AAL1 PROCESSOR FIFO backs up into the UTOPIA FIFO, then a head-of-line blocking problem can exist (i.e. cells targeted to other AAL1 processors are blocked because of the full condition of the UTOPIA FIFO). To alleviate such a situation, the ATM-to-Line Interface direction can be configured in Multi-Port Mode which makes the AAL1gator-32 appear as four separate PHYs each with its own unique address. The bottom two bits of the address indicate which of the four internal AAL1 processors is targeted to receive the cell. When polling any of the AAL1 processor addresses, a full indication will be given when any of the AAL1 PROCESSOR FIFOs reaches a half full state (room for four more cells). This will always allow room for any cells that may still be queued in the four cell FIFO and thus head-of-line blocking is prevented.

In Multi-Port Mode, if a runt cell is received, the port on the AAL1gator-32 which has the runt cell will indicate it is unavailable. Cells sent to other ports of that AAL1gator-32 will be dropped.

A runt cell is an erroneously truncated ATM cell of less than 53 bytes. This should not be normally present on the UTOPIA bus and only results when there is a violation of the UTOPIA protocol.

2.3.2 Workarounds:

1. Don't use Multi-Port Mode.

2. Use Multi-Port Mode and, upon an AAL1gator receiving a runt cell, force the UTOPIA master to send a cell to another device before it continues to send cells to the AAL1gator-32 that received the runt cell error.

2.3.3 Performance with workaround:

1. Functions normally. AAL1gator-32 responds to single address.

2. Functions normally. Each of the four A1SPs within the AAL1gator-32 responds to a unique address.

2.3.4 Performance without workaround:

1. Not applicable.

2. The AAL1gator-32 that received the runt cell error will continue to indicate it is unavailable and cells sent to other ports of that AAL1gator-32 will be dropped.

2.4 Adaptive Clock Recovery Mode - Underrun Status Could Be Missed

2.4.1 Description

The External Clock Control (ECC) Interface plays out (transmits) Adaptive Status information on a line basis which, when using the Adaptive Clock Recovery scheme in Unstructured Data Format (UDF) mode, enables an external decision to made about altering the line clock frequency. The adaptive output data is the averaged relative buffer depth in units of bytes. If the adaptive weighting is set to 0 this value becomes the raw buffer depth in units of bytes (see the AAL1gator-32 Datasheet for details).

When using the Adaptive Clock Recovery scheme in Unstructured Data Format (UDF) mode, it is possible that an underrun status could be missed. If all four A1SPs have adaptive status to play out, it is possible that a change in underrun status for a line will not make it to the external clock control port. Note that underrun status will still be indicated via an interrupt.

2.4.2 Workarounds:

None.

2.4.3 Performance without workaround:

It is possible that a change in underrun status for a line will not make it to the external clock control port. The underrun status will still be indicated via an interrupt.

2.5 LOW_CDV Queue Does Not Activate/Deactivate Correctly

2.5.1 Description

For Unstructured Data Format (UDF) lines there is a LOW_CDV bit which can be set in the LIN_STR_MODE memory register which will cause cells to be scheduled every 47 bytes instead of every frame. This eliminates the CDV caused by the scheduler. This mode can only be used in UDF-ML mode when BYTES_PER_CELL is 47. In High Speed mode cells are always scheduled every 47 bytes which assumes that partial cells are never used in HS mode.

If a queue is "added" to the ADDQ_FIFO and LOW_CDV is set, data errors may result. In addition, if a queue is deactivated by clearing the TX_ACTIVE bit when LOW_CDV is set, the CSD can enter a lock condition.

2.5.2 Workarounds:

1. Don't use LOW_CDV mode (this is an optional mode, only valid for unstructured connections).

2. Software workaround in Beta Release 1.0. This software workaround will be implemented in the AAL1gator-32 Beta Release 1.0 Software Driver which will make this deficiency virtually non-existent to the application. The workaround is described below to serve as a reference.

Beta Release 1.0 Software Workaround Description: Bring the connection up and down with LOW_CDV off and SUPPRESS_XMT set. Set LOW_CDV after connection is up but before sending cells.

Activate a LOW_CDV queue by doing the following:
a) When activating line initialize LOW_CDV in LIN_STR_MODE memory register to "0"
b) Configure queue with SUPPRESS_XMT=1 in TRANSMIT_CONFIG memory word (also set FRAMES_PER_CELL to 4 instead of 3)
c) Add queue using ADDQ_FIFO
d) Set LOW_CDV
e) Set CMD_ATTN bit in An_CMD_REG (this will load LOW_CDV value) for that line
f) clear SUPPRESS_XMT bit (after 250 us)

Deactivate a LOW_CDV queue by doing the following:
a) Set SUPPRESS_XMT in TRANSMIT_CONFIG memory word
b) clear LOW_CDV
c) Set CMD_ATTN bit for that line

d) Clear TX_ACTIVE bit
e) Queue will be dequeued the next time a cell is processed (wait 16 ms to be safe)

Note when using this method, the first cell which the chip sends will not have SN=0.

An alternative method would be to do the same steps as above, but don't set the SUPPRESS_XMT bit when activating the queue. This will have the first cell have SN=0, but there will be a larger CDV value for the first cell until LOW_CDV is set. You may also get two cells sent close together when LOW_CDV takes effect.

2.5.3 Performance with workaround:

1. Scheduling is frame based not cell based.

2. Low CDV Mode operates normally.

2.5.4 Performance without workaround:

1. Data errors may result if adding and deleting queues when in Low CDV Mode.

2.6 RATM_CLK Must be Present even when Debugging Hardware

2.6.1 Description

In normal operation, a clock is present on RATM_CLK and this Errata 2.6 is not an issue.

When debugging and in those cases where the RATM_CLK is not present (i.e. when running the AAL1gator-32 in local loopback via the loopback_enable bit in the T_QUEUE_TBL), there is a problem. In this scenario, when the A1SPs are taken out of reset, the OAM queue and some of the receive data queues could detect cells even though nothing is connected to the UTOPIA interface. This will not happen if a clock signal is connected to the RATM_CLK pin.

2.6.2 Workarounds:

Ensure a clock exists on the RATM_CLK pin when chip is in reset.

2.6.3 Performance with workaround:

Operates normally.

2.6.4 Performance without workaround:

When the A1SPs are taken out of reset, the OAM queue and some of the receive data queues could detect cells even though nothing is connected to the UTOPIA interface.

2.7 SRTS Queue Underrun Impacts Other Lines in A1SP

2.7.1 Description

When using the Synchronous Residual Time Stamp (SRTS) scheme in Unstructured Data Format (UDF) mode, if the SRTS queue (buffer which contains received SRTS nibbles) underruns for a specific line, a signal is sent to the internal clock synthesizer that indicates that *all* lines are in SRTS underrun. This causes all lines within an A1SP block to revert to nominal clocking.

2.7.2 Workarounds:

1. Software workaround in Beta Release 1.0. This software workaround will be implemented in the AAL1gator-32 Beta Release 1.0 Software Driver which will make this deficiency virtually non-existent to the application. The workaround is described below to serve as a reference.

Beta Release 1.0 Software Workaround Description: One way to prevent this problem from occurring is to prevent the SRTS queue underrun event from occurring. The SRTS queue is only checked when EN_SRTS bit is set in the LIN_STR_MODE memory register. So the goal is to only have EN_SRTS set when the queue is already active and not in SRTS_UNDERRUN.

Startup:
1) When line is activated (set CMD_ATTN), make sure EN_SRTS is not set in LIN_STR_MODE. CLK_SOURCE_TX can stay at SRTS (will generate nominal or last clock with no SRTS data).
2) Initialize SRTS_CDVT to the normal value (ROUNDUP(R_CDVT/11.75)) plus 2. (this creates a gap between when the data buffer underruns and the SRTS queue underruns).
3) When line exits underrun (interrupt will occur), set SRTS_EN in LIN_STR_MODE for that line. Set CMD_ATTN in CMD_REG for it to take affect.

Now SRTS will work fine as long is there is not an SRTS underrun. A data buffer underrun is ok, as long as the SRTS queue does not underrun. To handle the underrun case, do the following steps when an underrun is detected (interrupt):

1) Clear SRTS_EN for that line, set CMD_ATTN.

2) Initialize SRTS read and write pointer to match SRTS_CDVT value.
3) When line exits underrun (interrupt will occur), set SRTS_EN in LIN_STR_MODE for that line. Set CMD_ATTN in CMD_REG for it to take affect.

Note that since the SRTS_CDVT value is set to 2 more than what would be normally set, this provides at least 3 ms to handle the interrupt. If more time is required, the initial SRTS_CDVT value should be set higher. Note the higher the SRTS_CDVT value is, the longer it will take to react to changes in clock frequency and it may take longer to lock.

2.7.3 Performance with workaround:

Operates normally. This software workaround will be implemented in the AAL1gator-32 Beta Release 1.0 Software Driver which will make this deficiency virtually non-existent to the application.

2.7.4 Performance without workaround:

This software workaround will be implemented in the AAL1gator-32 Beta Release 1.0 Software Driver which will make this deficiency virtually non-existent to the application and the device will operate normally.

2.8 When RDB/CSB is Asserted 15 ns Beyond ACKB Certain SBI Interrupt Register Read Cycles Result in Corrupt Data

2.8.1 Description

All RAM reads and all registers other than the ones listed below function normally.

For read cycles of certain SBI Insert/Extract Bus Interrupt registers, if the RDB and CSB signals are held active for more than 50 ns after the falling edge of ACKB the data read may be corrupt; however, the fact that an interrupt occurred is never missed. The corrupt data that is read results in a possibly incorrect association of the interrupt to the actual link that caused the interrupt.

The following registers are affected:

Extract FIFO Under Run Interrupt Status Register

Extract FIFO Over Run Interrupt Status Register

SBI Parity Error Interrupt Status Register

Extract Depth Check Reset Interrupt Status Register

Insert FIFO Under Run Interrupt Status Register

Insert FIFO Over Run Interrupt Status Register

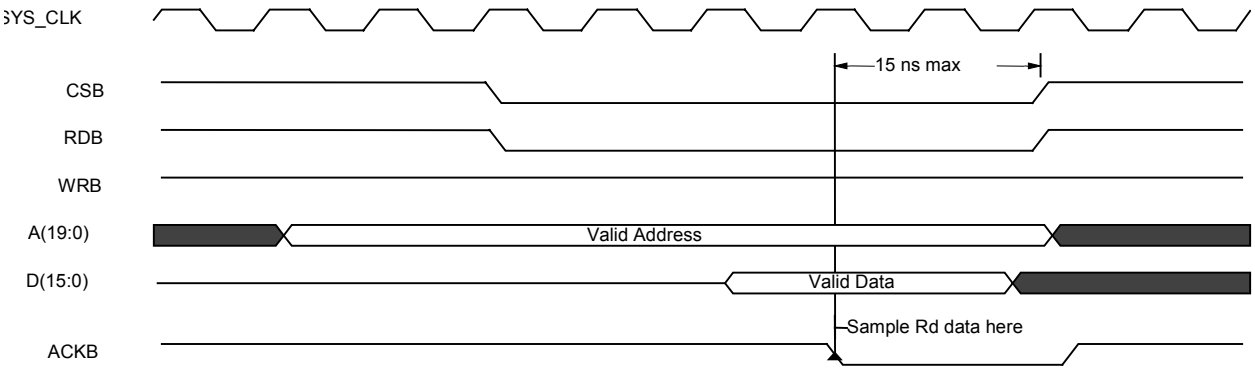
Insert Depth Check Reset Interrupt Status Register

2.8.2 Workarounds:

All RAM reads and all registers other than the SBI Insert/Extract Bus Interrupt registers listed above, function normally.

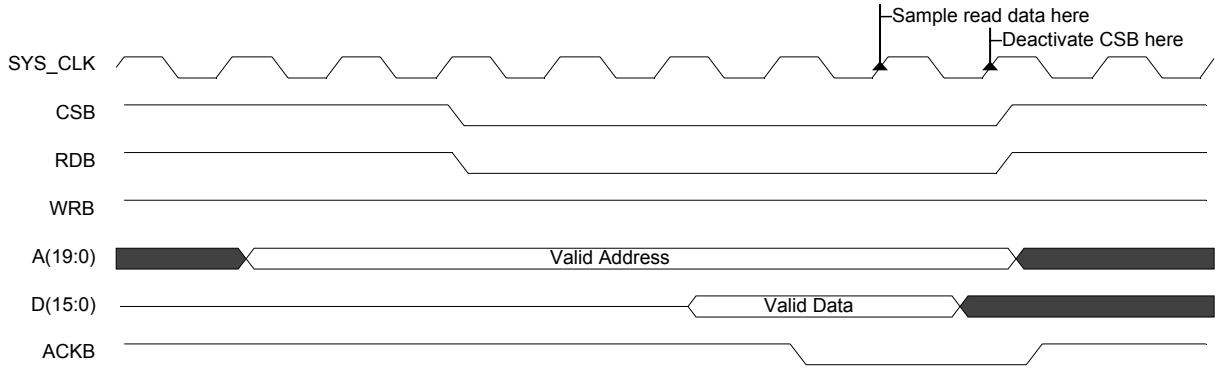
2.8.2.1 Asynchronous Solution

The AAL1gator-32 provides an ACKB signal to indicate when data is ready on chip reads. If the falling edge of ACKB is used to latch the data, and the CSB signal is deactivated within 15 ns of the falling edge of ACKB, reliable reads will occur.



2.8.2.2 Synchronous Solution

An alternative solution is to lock the SYS_CLK and SBI REF_CLK to a common reference. In this case, if SYS_CLK is used as the processor clock, data can be latched reliably using the first rising edge of SYS_CLK while ACKB active. CSB should then be deactivated with the following rising edge of SYS_CLK.



2.8.3 Performance with workaround:

Operates normally.

2.8.4 Performance without workaround:

Data read from the specific SBI Interrupt registers listed above is not reliable. The fact that an interrupt occurred is never missed however, the corrupt data that is read results in a possibly incorrect association of the interrupt to the actual link that caused the interrupt.

2.9 When a Significant Number of Queues are Configured in TDM-to-TDM Loopback Cells May be Dropped

2.9.1 Description

A loopback FIFO exists in the A1SP block that allows cells destined for the UTOPIA bus to instead be looped directly back to the receive ATM logic. (TDM-to-TDM loopback). This errata is not relevant (i.e. cells are not dropped) if only a few queues are configured for TDM-to-TDM loopback. Unless more than approximately six queues are configured for TDM-to-TDM loopback per A1SP, it is unlikely that this FIFO will overflow. If this FIFO fills and cells are sent to the FIFO, the cells will be dropped.

This deficiency will be fixed in Rev B such that all queues can be configured in TDM-to-TDM loopback without dropping any cells.

2.9.2 Workarounds:

This errata is not relevant (i.e. cells are not dropped) if only a few queues are configured for TDM-to-TDM loopback. Unless a significant amount of traffic for

an A1SP is configured for TDM-to-TDM loopback, it is unlikely that the FIFOs will overflow. If this FIFO fills then cells will be dropped. There are no workarounds for this problem.

2.9.3 Performance without workaround:

Looped back cells may be dropped. These cells will be replaced by dummy cells by the Receive ATM Processor (RALP).

2.10 MVIP-90 Mode is Not Functional

2.10.1 Description

The MVIP-90 option in Direct Low Speed Mode does not work correctly. *H-MVIP works correctly.*

2.10.2 Workarounds:

Use external glue logic to make an MVIP-90 signal appear to the AAL1gator-32 to be a typical direct low speed signal.

2.10.3 Performance with workaround:

With glue logic, the MVIP-90 signal appears to the AAL1gator-32 to be a typical direct low speed signal, and therefore functions normally.

2.10.4 Performance without workaround:

MVIP-90 is not functional; however H-MVIP works correctly. Data will not have correct frame alignment.

2.11 REF_VAL_ENABLE in E1 SDF-MF Mode is not Functional

2.11.1 Description

This errata only applies when using E1 SDF-MF mode; it does not apply to all other modes.

A new feature to minimize CDV for single-DS0 connections with signaling using full cells was introduced in the AAL1gator-32. As described in the “TxA1SP” and “Add Queue FIFO” sections of the datasheet for single DS0 queues with signaling enabled using full cells, cell clumping can occur in situations where

cells from different VCs are scheduled such that they are to be segmented at the same instance in time.

The CDV introduced in this case can be minimized by setting REF_VAL_ENABLE to 1. With REF_VAL_ENABLE set to 1, and using different offset values for each queue on a particular line, when adding an entry to the Add_Queue_FIFO, the scheduling of cell segmentation is distributed in such a manner as to minimize CDV. Note that the algorithm for distributing cell segmentation is based on the premise that all queues on a line are single DS0 full cell queues. See the datasheet for details.

This feature works for all modes except E1 SDF-MF mode.

2.11.2 Workaround:

Don't enable REF_VAL_ENABLE in E1 SDF-MF mode. All other modes support REF_VAL_ENABLE as documented in the datasheet.

With the REF_VAL_ENABLE bit cleared the CDV introduced by the AAL1gator-32 is the same as it is for the PM73121 AAL1gator-II.

2.11.3 Performance without workaround:

CDV introduced by the AAL1gator-32 is the same as it is for the PM73121 AAL1gator-II.

2.12 UTOPIA Registers - Read Timing Violation

2.12.1 Description

In the AAL1gator-32 Datasheet, the Microprocessor Interface Read Timing specifies that the AAL1gator-32 provides 5 ns of setup time from data valid to ACKB asserted low. For the UTOPIA registers (address 0x80120 -0x80125), the AAL1gator-32 Rev A actually provides negative 10 ns of setup time, i.e., AAL1gator-32 asserts ACKB low 10 ns *before* asserting data valid.

2.12.2 Workaround:

Read each UTOPIA register twice, discarding the read data from the first read.

2.12.3 Performance with workaround:

The data read from the UTOPIA registers will be correct.

2.12.4 Performance without workaround:

The data read from the UTOPIA registers may be invalid.

2.13 Setting HS_GEN_DS3_AIS Does Not Cause T_COND_CELL_CNT to Increment

2.13.1 Description

When the HS_GEN_DS3_AIS bit is set, the AAL1gator-32 generates cells with a framed DS3 AIS pattern, as a form of cell conditioning. The AAL1gator-32 should increment the T_COND_CELL_CNT instead of the T_CELL_CNT for each generated cell while HS_GEN_DS3_AIS is set. Instead the AAL1gator-32 erroneously continues to increment the T_CELL_CNT instead of the T_COND_CELL_CNT.

2.13.2 Workaround:

There is no workaround. See Section 2.13.3.

2.13.3 Performance without workaround:

T_COND_CELL_CNT does not indicate the number of conditioned cells generated. The number of conditioned cells generated can be approximated by multiplying the nominal cell rate by the amount of time that the HS_GEN_DS3_AIS bit was set.

2.14 Maintain Bit-Count-Integrity Through Underrun Feature is Not Functional

2.14.1 Description

For real-time applications such as voice, it may be desirable to have a shallow receive buffer to minimize delay - this is done by using a low R_CDVT value. With a low R_CDVT value, when as few as one cell is lost, the receive buffer can quickly underrun. For SDF-FR and SDF-MF queues, the Receive Adaptation Layer Processor (RALP) responds to this underrun by initiating a structure search which results in the RALP dropping all received cells until it finds the next structure pointer followed by dropping all cell bytes until if finds the start of the structure. The net result is a loss of bit-count-integrity on the CES connection. For UDF-ML queues, the RALP does not initiate a structure search, but does initiate the resume procedure in which RFTC plays out R_COND_DATA while RALP accumulates R_CDVT's worth of bits. This also results in a loss of bit-count-integrity on the CES connection.

With the Bit-Count-Integrity Through Underrun feature enabled by setting the BITI_UNDERRUN bit, the bit-count-integrity of the CES connection can be maintained. The RALP maintains bit-count-integrity because it does not initiate a structure search or a resume procedure when cells are lost. (see the section on " Sequence Number Processing" in the datasheet).

This feature is not functional in Rev A.

2.14.2 Workaround:

Use a larger value for R_CDVT when using sequence number processing so that underruns do not occur when cells are lost.

2.14.3 Performance without workaround:

R_CDVT must be set larger, when using sequence number processing. For small values of R_CDVT, the benefits of sequence number processing may not be realized.

2.15 Proper SBI Initialization Sequence is Required to Prevent CAS from Corruption

2.15.1 Description

This errata does not apply if the AAL1gator-32 is not configured in SBI mode. This errata is also not an issue if the correct SBI initialization sequence is followed. The recommended SBI initialization sequence is:

1. AAL1gator-32 INSBI
2. TEMUX INSBI (can switch steps 1 and 2)
3. AAL1gator-32 EXSBI
4. TEMUX EXSBI (can switch steps 3 and 4)

2.15.2 Workaround:

Follow the recommended SBI initialization sequence described above.

2.15.3 Performance with workaround:

AAL1gator-32 operates normally.

2.15.4 Performance without workaround:

There is a remote chance that AAL1gator-32 will corrupt CAS.

2.16 Reporting of Misaligned H-MVIP Sync Pulse Can Be Missed in a Certain Condition

2.16.1 Description

The AAL1gator-32 automatically resynchronizes when a misaligned sync pulse (F0B) is encountered on the H-MVIP interface. This functions normally. However if the F0B pulse advances by exactly one 4 MHz clock cycle (1 chance in 256) then the reporting of this misaligned sync pulse will not cause the R_LINE_RESYNC or T_LINE_RESYNC bit to be set in the A1SPn RSTAT_FIFO.

2.16.2 Workaround:

The F0B pulse is usually generated by external board logic. Any movement in this signal could be detected in the external frame generation logic.

2.16.3 Performance with workaround:

All movements of the F0B pulse will be reported by external logic.

2.16.4 Performance without workaround:

There is a 1 out of 256 chance that a misaligned F0B pulse will not be reported as such. In all cases, however, the AAL1gator-32 device will realign with the new F0B position.

2.17 Only After an Underrun Condition, the Value of the First Pointer Received is Not Verified for an Out of Range Condition or a Dummy Pointer Value

2.17.1 Description

Only after an underrun condition has occurred will the first pointer received after the underrun condition not be checked for an Out of Range Value or a Dummy Pointer Value.

2.17.2 Workaround:

There is no workaround. The implication is that only after an underrun condition, in the unlikely event that the first pointer received is invalid, a pointer reframe will occur.

2.17.3 Performance with workaround:

No workaround. See Section 2.17.2.

2.17.4 Performance without workaround:

No workaround. See Section 2.17.2.

2.18 Erroneous Depth Check Interrupts Occur on Floating (Asynchronous) SBI Tributaries when DC_EN=0

2.18.1 Description

The DC_EN bit in the INSBI and EXSBI registers enables the Depth Check Logic. When asserted high the Depth Check Logic will periodically monitor the Data/Framing FIFO Depth and compare it against the FIFO write and read pointers. In the unusual event of a discrepancy (i.e. a FIFO underrun or overrun) the tributary is synchronously reset by the Depth Check Logic.

Note that if there are any SBI synchronous tributaries (SYNCH_TRIB = 1) this Depth Check feature is not supported as described in Section 3.5 of this errata.

On SBI floating (asynchronous) tributaries when the depth check enable bit, DC_EN, of either the EXSBI or INSBI Control registers is cleared (i.e. disabled) and SYNC_INT_EN is set, erroneous depth check interrupts are reported. Note however that there is absolutely no effect on the data path.

With the DC_EN bit set and all tributaries configured with SYNCH_TRIB = 0, the Depth Check Logic functions as expected.

2.18.2 Workaround:

If all SBI tributaries are floating (asynchronous) tributaries, do not clear the depth check enable bits, DC_EN, of either the EXSBI or INSBI Control registers or make sure that SYNC_INT_EN is disabled. If there are any SBI synchronous tributaries the Depth Check feature is not supported as described in Section 3.5 of this errata.

2.18.3 Performance with workaround:

If all SBI tributaries are floating (asynchronous) tributaries and DC_EN is set, the depth check feature works properly.

2.18.4 Performance without workaround:

Erroneous depth check interrupts are reported.

2.19 C1FP_ADD Pin Not Available on AAL1gator-32 Revision A

2.19.1 Description

In SBI mode only, the B4 pin was unused in Revision A. For revisions above Revision A it can remain unconnected when not used. However an option which is enabled by setting the SBI_BUS_CFG_REG bit has been added to revisions above Revision A to enable this pin to be used as the Add Bus C1FP pulse. This would allow the C1FP pulses for the Add bus and Drop buses to be unique and offset from each other. See the C1FP_ADD Pin Description below.

C1FP_ADD	Input	B4	C1 Frame Pulse for Add bus. This pin can optionally be used as the C1FP pulse for the Add bus if the Add bus and Drop bus need to be offset from each other. To use this pin the TWO_C1FP_EN bit must be set in the SBI_BUS_CFG_REG.

2.19.2 Workaround:

Leave the B4 pin unused.

2.19.3 Performance with workaround:

Functions normally. The C1FP pulse for the Add bus and Drop bus are the same.

2.19.4 Performance without workaround:

The C1FP_Add pin is only available on revisions of devices above Revision A.

2.20 SHIFT_CAS Feature Not Available on AAL1gator-32 Revision A

2.20.1 Description

The AAL1gator-32 Revision A device reads the signaling nibble for each channel on the last nibble of each channel's data. A new feature, SHIFT_CAS, was added and is available on devices *after* Revision A. With the SHIFT_CAS bit set in the LIN_STR_MODE register the AAL1gator-32 reads the signaling nibble for each channel on the first nibble of each channel's data.

Note that:

1. SHIFT_CAS applies to both rl_sig and tl_sig signals
2. SHIFT_CAS applies to direct low speed and H-MVIP line modes only.

2.20.2 Performance with workaround:

SHIFT_CAS is not available on Revision A.

2.20.3 Performance without workaround:

SHIFT_CAS is not available on Revision A.

2.21 BUSMASTER Feature Not Available on AAL1gator-32 Revision A or B

2.21.1 Description

There are deficiencies in the PM8315 TEMUX SBI Add bus (EXSBI) and PM73122 AAL1gator-32 Drop bus (EXSBI) parity logic where parity is calculated across all tributaries, active or inactive, as well as across unused SBI overhead bytes. This results in erroneous SBI bus parity errors even when data is valid.

To compensate for this deficiency, a BUSMASTER bit has been added (bit 15 of the SBI_BUS_CFG_REG register) to the AAL1gator-32 Revision C – this feature is not available for either Revisions A or B. The BUSMASTER bit controls whether or not the AAL1gator-32 drives the SBI Add bus when no other device is driving the bus during SBI overhead bytes and inactive tributaries. If BUSMASTER is set and the DETECT signal is low (inactive), then it means no other device is driving the SBI Add bus and the AAL1gator-32 will drive the bus to a known state. This will prevent parity errors from otherwise being falsely detected by the PM8315 TEMUX.

Note that the TEMUX also provides a BUSMASTER bit for the same purpose on the SBI Drop bus (in the TEMUX to AAL1gator-32 direction). This bit must also be set to prevent parity errors from otherwise being falsely detected by the AAL1gator-32.

Note that if there are multiple devices on the SBI bus, to prevent contention, only one device on both the Add bus and Drop bus can have the BUSMASTER bit set.

2.21.2 Performance with workaround:

The BUSMASTER feature is available on AAL1gator-32 Revision C – this feature is not available for either Revisions A or B. Without the BUSMASTER feature, SBI parity errors will be erroneously detected by the PM8315 TEMUX. SBI parity interrupts on the PM8315 TEMUX should be disabled when using AAL1gator-32 Revision A.

2.21.3 Performance without workaround:

The BUSMASTER feature is available on AAL1gator-32 Revision C – this feature is not available for either Revisions A or B. Without the BUSMASTER feature, SBI parity errors will be erroneously detected by the PM8315 TEMUX. SBI parity interrupts on the PM8315 TEMUX should be disabled when using AAL1gator-32 Revision A.

3 DOCUMENTATION ERRORS OR CLARIFICATIONS

3.1 Register Values Incorrect for EXSBI, INSBI and DLL

Reset value for Reg EXSBI MIN_DEPTH FOR DS3 @ 0x80409 = 0x00FE, not 0x0004.

Reset value for Reg EXSBI DS3 THRESHOLD @ 0x8040C = 0x004C, not 0x002D.

Reset value for Reg INSBI MIN_DEPTH FOR DS3 @ 0x80508 = 0x00DC, not 0x000C.

Reset value for Reg INSBI INS_MSTR_INT @ 0x80512 = 0x40, not 0x00.

Reset value for Reg DLL Control & Status DLL_STAT_REG = 0b xxxx xxxx xxxx xx01, not 0b xxxx xxxx xxxx xx00.

3.2 Incorrect Sentence in SBI Programming Sequence Section

In the "Programming Sequence for SBI" section, under the heading, "INSBI/EXSBI Programming Steps", the following sentence is only valid for configuration of SBI tributary control RAM. Since the programming steps describe both mapping RAM and control RAM access, the statement is misleading.

Change original sentence:

"Whether tributary mapping is performed or using default 1:1 mapping, the above 4 steps must be done and must be repeated for every tributary access."

To the following:

“The mapping RAM only needs to be configured if tributary mapping is enabled (TS_EN=’1’). If tributary mapping is disabled, the default 1:1 mapping is automatically assumed and no mapping RAM configuration is necessary.

Whether tributary mapping is performed or using default 1:1 mapping, the control RAM needs to be configured for any active tributaries. All tributaries are initialized to being disabled.”

Note that this change also applies to document PMC-1991820, AAL1gator-32/8/4 Programmer’s Guide.” Issue 2 of this document contains this update.

3.3 Clarification of SBI Operation

1) CAS is only supported on tributaries, which have the INSBI configured in SYNC mode. CAS is not supported on ASYNC tributaries.

2) If any tributary is in SYNC mode, in INSBI, the DC_EN bit on all tributaries is ignored. The DC_EN bit is used to automatically reset the tributary if an underrun or overrun occurs.

3) If any INSBI or EXSBI tributary indicates an overrun or underrun, that tributary must be reset by writing the configuration register for that tributary. Simply writing the configuration register with the same data that is already in it will cause a reset. Note that the Overrun and Underrun Interrupt registers indicate the Link Number which had an error. This Link number needs to be mapped to an SBI tributary to determine which tributary to reset. Unless mapping is enabled, this will always be a 1:1 mapping.

If DC_EN is set then the tributary reset will happen automatically unless one of the INSBI tributaries is in SYNC mode and the error is detected by INSBI. Then the tributary needs to be reset by software. A reset routine has been incorporated into the driver to reset the INSBI tributary if this situation occurs.

Note that this reset routine is affected by errata described in section 2.8.

3.4 Clarification of Tributary Mapping Sequences in "Programming Sequence for SBI"

The last bullet item of "Programming Sequence for SBI" section is changed from:

" It is important to note that if tributary mapping needs to be done on any tributary, then all tributary mapping must be done to all tributaries in the SBI (i.e., 84 tributaries if all 3 SPEs are T1)"

to:

" It is important to note that if tributary mapping needs to be done on any tributary, then tributary mapping must be done to all tributaries in the SBI. For example, all 84 tributaries must be mapped if all 3 SPEs are T1 mode, or all 63 tributaries must be mapped if all 3 SPEs are E1 mode)"

3.5 Depth Check Not Supported in SBI Synchronous Mode

In the "Programming Sequence for SBI" section the following paragraph was added:

"In SBI Synchronous Mode the DC_EN bit is ignored and DC_INT_EN in the Extract/Insert Control register should be disabled to prevent spurious interrupts. This must be done as Depth Check logic does not support synchronous mode."

3.6 Exiting UDF_HS Loopback Mode Requires That High Speed Queue Be Reset

When exiting UDF_HS Loopback Mode the High Speed Queue must first be reset. The document PMC-1981419, PM73122 AAL1gator-32 Datasheet Issue 6, has been updated to describe this as follows:

In the T_QUEUE_TBL register description, the TRANSMIT_CONFIG Word Format (12_H) description for the LOOPBACK_ENABLE is modified to read:

LOOPBACK_ENABLE (14)	Set to 1 to loopback cell to receive side. Set VPI/VCI to correspoding receive queue number. Note to maximize throughput, this register is only read once in UDF-HS mode, when building the first cell. Therefore if loopback is desired for UDF-HS mode, this bit must be set first and cannot be changed after the queue is already running.

In the High Speed Mode Description within the Line Configuration Details Section of the Operations section, the following was added:

The An_SW_RESET bit in the An_CMD_REG memory register functions as a queue reset signal in high speed mode. If the state of LOOPBACK_ENABLE in TRANSMIT_CONFIG is desired to be changed, the high speed queue must be reset using the An_SW_RESET bit.

Also when re-activating a highspeed queue, if it is required that the first sequence number of the new connection has to be 0, then the queue must be reset using the An_SW_RESET bit.

Otherwise, clearing and setting the TX_ACTIVE bit in QUEUE_CONFIG can be used to deactivate and activate the queue.

3.7 SPE Activation Must Occur After Tributaries are Enabled

The description for SPEn_ENBL of Register 0x80300H: SBI Bus Configuration Register (SBI_BUS_CFG_REG) is modified in document PMC-1981419, PM73122 AAL1gator-32 Datasheet Issue 6, as follows:

SPEn_ENBL

The SPEn_ENBL field is used to enable or disable an entire SPE on the SBI. When high the SPE is enabled. All SPEs default to being disabled. Important Note: An SPE must not be enabled without any tributaries enabled on it. When initially activating an SPE, enable the tributaries first and then enable the SPE. When deactivating an SPE, disable the SPE first and then deactivate the tributaries.

3.8 INSBI and EXSBI RAM Register Description Correction

3.8.1 INSBI RAM Register Description Correction

The description for APAGE of Register 0x80500H: Insert Control Register (INS_CTL) is corrected in document PMC-1981419, PM73122 AAL1gator-32 Datasheet Issue 6, as follows:

APAGE

The tributary mapping ~~and control~~ configuration RAM~~s~~ active page select bit (APAGE) controls the selection of one of two pages in the tributary mapping RAM~~s~~ to be the active page. When APAGE is set high, the configuration in page 1 of the tributary mapping RAMs is used to associate incoming tributaries to AAL1gator links. When APAGE is set low, the configuration in page 0 of the tributary mapping RAMs is used to associate incoming tributaries to Aal1gator links. Changes of the active page as a result of write accesses to APAGE will be synchronized to SBI multi-frame boundaries at C1FP.

Note that only the Mapping RAM has ~~there are only~~ two pages ~~of the mapping RAM.~~ . ~~There is only one page of~~ The control ~~configuration~~ RAM has only one page."

3.8.2 EXSBI RAM Register Description Correction

The description for APAGE of Register 0x80400H: Extract Control Register (EXT_CTL) is corrected in document PMC-1981419, PM73122 AAL1gator-32 Datasheet Issue 6, as follows:

APAGE

The tributary mapping RAMs active page select bit (APAGE) controls the selection of one of two pages in the tributary RAMs to be the active page. When APAGE is set high, the configuration in page 1 of the tributary mapping RAMs is used to associate incoming tributaries to AAL1gator links. When APAGE is set

low, the configuration in page 0 of the tributary mapping RAMs is used to associate incoming tributaries to AAL1gator links. Changes of the active page as a result of write accesses to APAGE will be synchronized to SBI multi-frame boundaries at C1FP.

Note that only the Mapping RAM has ~~there are only~~ two pages ~~of the mapping RAM.~~ . ~~There is only one page of~~ The control ~~configuration~~ RAM has only one page."

3.9 INSBI/EXSBI Depth Check Interrupt Status Registers Provide SBI Trib Number, Not Link Number

Register 0x8040EH: Extract Depth Check Interrupt Status Register (EXT_DCR_INT) previously documented in the datasheet that the link number was reported upon a depth check error event on the INSBI/EXSBI links of the SBI bus. This is an error. The SBI tributary number is provided – not the link number. This is corrected in document PMC-1981419, PM73122 AAL1gator-32 Datasheet Issue 6, as follows:

Register 0x8040EH: Extract Depth Check Interrupt Status Register (EXT_DCR_INT)

Bit	Type	Function	Default
Bit 15	Rsvd	Unused	0
Bit 14	Rsvd	Unused	0
Bit 13	Rsvd	Unused	0
Bit 12	Rsvd	Unused	0
Bit 11	Rsvd	Unused	0
Bit 10	Rsvd	Unused	0
Bit 9	Rsvd	Unused	0
Bit 8	Rsvd	Unused	0
Bit 7	RO	SPE[1]	0
Bit 6	RO	SPE[0]	1
Bit 5	RO	SBI_TRIBUTARY[4]	0
Bit 4	RO	SBI_TRIBUTARY[3]	0
Bit 3	RO	SBI_TRIBUTARY[2]	0
Bit 2	RO	SBI_TRIBUTARY[1]	0
Bit 1	RO	SBI_TRIBUTARY[0]	0
Bit 0	R2C	DCR_INTI	0

- Back to back reads of this register must be at least 250 ns apart.

DCR_INTI

This bit is set when a Depth Check error is detected. This error is detected when the internal FIFO pointers do match the expected internal FIFO depth.

Values in these fields should only be looked at when DCR_INTI is a ‘1’.

SPE[1:0] and SBI_TRIBUTARY

The SPE and SBI_TRIBUTARY fields are used to specify which Tributary was associated with the Depth Check error. Note that if mapping is enabled the SBI

Tributary is different than the internal link. Also note that SPEs are numbered 1,2,3.

3.10 Clarification of R_SN_CONFIG Word Format – For Robust SNP The First Cell Received Will Always be Dropped

In the R_QUEUE_TBL section which describes the R_QUEUE_TBL Format, the definition of ROBUST_SN_EN and NODROP_IN_START in the R_SN_CONFIG Word Format ($0D_H$) has been modified as follows:

NODROP_IN_START (3)	In the "Fast SN Algorithm" for SN processing, the first cell received will always be dropped because a sequence has not been established yet. This bit disables the automatic dropping of cells while in the START state 0 When SN_STATE equals "000"$_b$ any received cell will be dropped. 1 When SN_STATE equals "000"$_b$ any received cell with valid SNP will be accepted. ***Note that in Robust SN processing or High Speed mode, this bit has no effect.***

3.11 Correction in "Out of Band Signaling Idle Detection" Description

There is a typo where the RX and TX CAS values are swapped in the "Out of Band Signaling Idle Detection" description in the Functional Description section. The second paragraph should read as below; a third paragraph was also added:

During the out of band signaling idle detection, a word is written to the Transmit Idle Interrupt FIFO every time the value of the CAS nibble changes and then remains stable for one additional multiframe. TIDLE_FIFO_EMPB is set as long as this FIFO contains any unread entries, which will result in a maskable interrupt. The structure of the word contained in the FIFO is shown in the Figure. The first eight bits indicate the channel, which encountered a change in the value of CAS. The next four bits indicate the RX CAS value and the final four bits indicate the TX CAS value.

TX refers to the CAS incoming on the TDM interface (SBI Drop bus, H-MVIP RL_SIG or direct low speed mode RL_SIG), and RX refers to CAS incoming in ATM cells at the UTOPIA Cell Sink interface.

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