Bookly Micro

32 Megabit (4M x 8/2M x 16) Flash Memory
AC29LV320B/T

3.0 Volt-Only Boot Sector Flash Memory

DEVICE FEATURES

- **Organized as 2M x 16 / 4M x 8**
- **Single Voltage Read and Write Operations**
  - 2.7~3.6V power supply
- **Sector Architecture**
  - Byte Mode (4M x 8): Eight 8 Kbyte and sixty-three 64 Kbyte sectors
  - Word Mode (2M x 16): Eight 4 Kword and sixty-three 32 Kword sectors
  - Page Mode: 2 Kword (or 4 Kbyte) per-page, total 1,024 pages
- **Top or Bottom Boot Block Configuration**
- **Read Access Time**
  - Access time: 90ns and 120ns
- **Power Consumption**
  - Automatic sleep mode current: 200 nA
  - Standby mode current: 200 nA
  - Active read current (at 1 MHz): 2 mA
  - Active read current (at 5 MHz): 10 mA
- **Erase Features**
  - Any combinations of sectors can be erased
- **Unlock Bypass Program Command**
  - Reduce overall programming time when issuing multiple program command sequences
- **End-of-Program or End-of-Erase Software Detection**
  - Data# Polling
  - Toggle Bit
- **End-of-Program or End-of-Erase Hardware Detection**
  - Ready/Busy# Pin (RY/BY#)
- **Hardware Reset (Reset#)**
  - Hardware method to reset the device to reading array data
- **WP#/ACC Input Pin**
  - Write protect (WP#) function allows protection of two outermost boot sectors, regardless of sector protect status
  - Acceleration (ACC) function accelerates program time
- **Sector Protection**
  - Using hardware method to lock a sector and prevent any program or erase operation within that sector. Sectors can be locked in system or via programming equipment.
  - Temporary Sector Unprotect feature allows code changes in previously locked sectors.
- **JEDEC Standard**
  - Pin-out and software compatible with single-power-supply flash memory
- **High reliability**
  - Endurance cycles: 100K (typical)
  - Data retention at 125°C: 10-year
- **Package Options**
  - 48-Pin TSOP
  - 48-Ball FBGA

PRODUCT DESCRIPTION

The AC29LV320 is a 32-Megabit, 3.0 volt-only flash memory, organized as 2,097,152 words of 16 bits each or 4,194,304 bytes of 8 bits each. The word mode data (x16) appears on DQ15-DQ0, and the byte mode data (x8) appears on DQ7-DQ0. The device can be programmed in-system using 3.0-volt single V_{CC} supply. No V_{PP} is required for write or erase operation. The device can also be programmed in standard EPROM programmers.

The device offers access times of 90 or 120 ns. The device has separate control signals, chip enable (CE#), write enable (WE#) and output enable (OE#), to eliminate bus contention. The device requires a 3.0-volt single power supply for both read and write operations. Both the program and erase operations are performed using the internally generated high voltages.

The device has command set that is compatible with the JEDEC single-power-supply Flash standard. The write cycles latch addresses and data needed for programming and erase operations. To read data from the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (Toggle Bits) status bits. After a program or erase cycle has been completed, the device is ready to read array data or to accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The page erase feature allows memory pages to be erased and reprogrammed without affecting the data contents of other pages. Hardware data protection feature includes a low V_{CC} detector that automatically inhibits write operation during power transition. The hardware sector protection feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved during in-system operation or via programming equipment.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The system can also place the device into the standby mode. Both modes reduce greatly the power consumption.

The device is offered in package types of 48-ball FBGA and 48-pin TSOP.

PRODUCT SELECTOR GUIDE

Part Number	AC29LV320	
Speed Option (Standard Voltage Range: V_{CC}=2.7~3.6V)	**90**	**120**
Max Access Time (ns)	90	120
CE# Access (ns)	90	120
OE# Access (ns)	40	50

ORDERING INFORMATION
Standard Products
The order number is defined by a combination of the following elements.

AC29LV320 T -- 90 E C _

Optional Processing
Blank= Standard Processing
B = Burn-in
N = 16-byte ESN devices

Temperature Range
C = Commercial (0°C to 70°C)
I = Industrial (-40°C to +85°C)
E = Extended (-55°C to +125°C)

Package Type
E = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS048)
WM = 48-Ball Fine Pitch Ball Grid Array (FBGA) 0.80 mm pitch, 6 x 12 mm package (FBD048)

Speed Option
See Product Selector Guide and Valid Combinations

Boot Code Sector Architecture
T = Top Sector
B = Bottom Sector

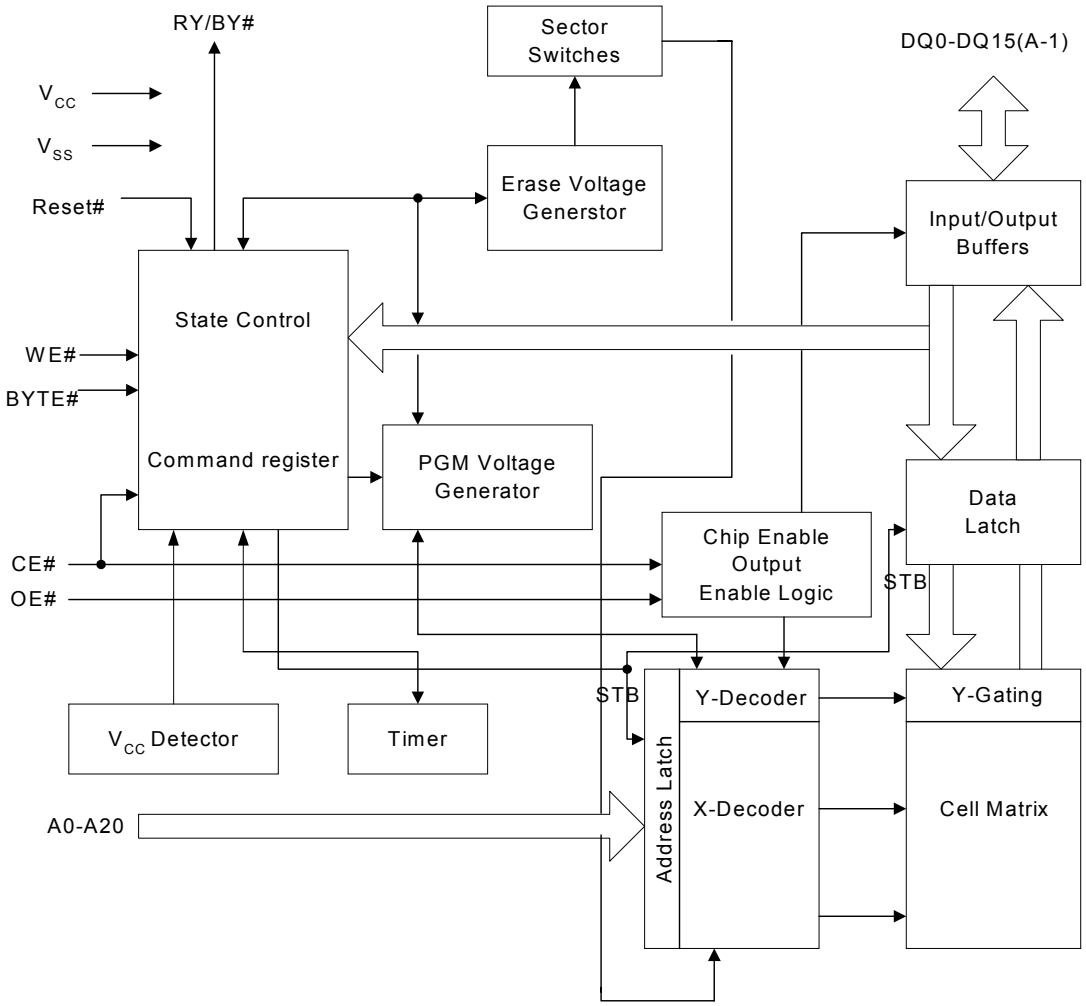
Device Number/Description
AC29LV320
32 Megabit (4M x 8/2M x 16) Flash Memory 3.0 Volt-only Read, Program and Erase

Valid Combinations for TSOP Packages	
AC29LV320T-90 AC29LV320B-90	EC, EI
AC29LV320T-120 AC29LV320B-120	EC, EI, EE

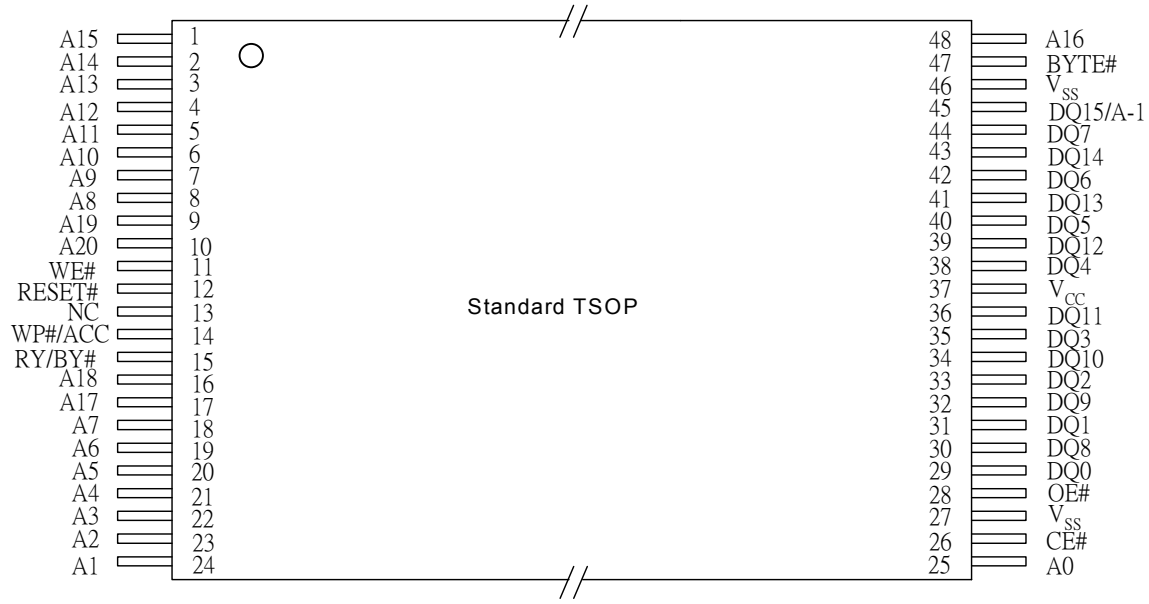
Valid Combinations for FBGA Packages			
Order Number		Package Marking	
AC29LV320T-90 AC29LV320B-90	WMC, WMI	CL320T-90 CL320B-90	C, I
AC29LV320T-120 AC29LV320B-120	WMC, WMI, WME	CL320T-12 CL320B-12	C, I, E

Valid Combinations: The Valid Combinations list the configurations to be supported in volume. Consult Actrans System Inc. sales office to confirm availability of any specific valid combination or to check newly released combination.

Functional Block Diagram

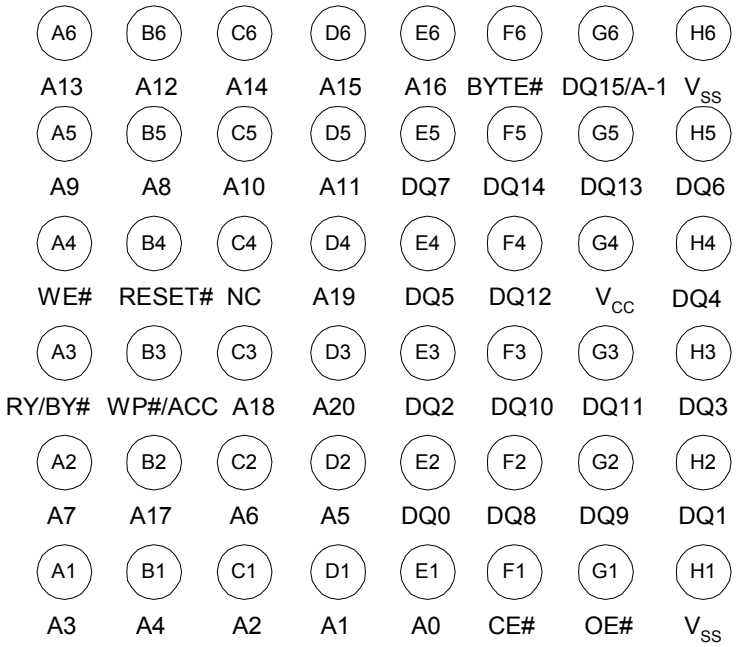


Connection Diagrams



Connection Diagrams

48-Ball FBGA
Top View, Balls Facing Down



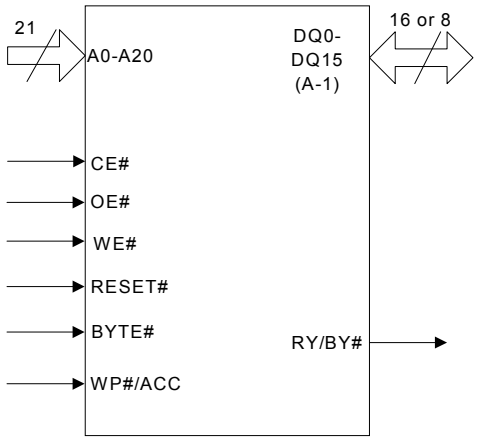
Special Handling Instructions for Fine Pitch Ball Grid Array (FBGA)

Special handling is required for Flash Memory products in FBGA packages. Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged period of time.

PIN DESCRIPTION

A0–A20	= 21 addresses
DQ0–DQ14	= 15 data inputs/outputs
DQ15/A-1	= DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	= Select 8-bit or 16-bit mode
CE#	= Chip enable
OE#	= Output enable
WE#	= Write enable
RESET#	= Hardware reset pin, active low
RY/BY#	= Ready/Busy# output
VCC	= 3.0-volt single power supply
VSS	= Device ground
NC	= Pin not connected internally
WP#/ACC	= Write protect/ Acceleration program

Logic Symbol



DEVICE OPERATION

The device operations are initiated through internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, and the address and data information that is needed to execute the command. The contents of the register serve as inputs to the internal state machine. The outputs of state machine dictate the function of the device. Table 1 lists the device operations, the inputs and control levels they require, and the resulting output.

Word/Byte Configuration

The BYTE# pin controls the device data I/O pins DQ15–DQ0 to operate either in byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, and DQ15– DQ0 are active and controlled by CE# and OE#. If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0– DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are in tri-state, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Read

To read array data from the outputs, the system must set the CE# and OE# pins to V_{IL}. CE# is the power control, which selects the device. OE# is the output control, which gates array data to the output pins. The WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set to read array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is required in this mode to obtain array data. The device remains enabled for read access until the command register contents are altered. The device is also ready to read array data after completing a Program or Erase operation.

The Read Operations table provides the read parameters, and Figure 11 shows the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Reset

Writing the reset command to the device resets the device to the read mode. The address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasing begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data.

Write Command/Command Sequence

Writing specific address and data commands or sequences into the command register initiates device operations. Table 11 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data.

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must set WE# and CE# to V_{IL}, and OE# to V_{IH}. All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in the "AC Characteristics" section.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for the write operations.

Word/Byte Program

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next. Table 11 shows the address and data requirements for the byte program command sequence. When the Program operation is complete,

the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6 or RY/BY#. See “Write Operation Status” for information on these status bits.

Note that a hardware reset immediately terminates the programming operation. In order to ensure data integrity, the Byte Program command sequence should be reinitiated once the device has reset to reading array data. Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a “0” back to a “1”. Attempting to do so may cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”.

Unlock Bypass

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles, followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 11 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the program address and the data 90h. The second cycle need only contain the data 00h. The device then returns to reading array data.

Figure 1 illustrates the algorithm for the program operation. See the Erase/Program Operations table in “AC Characteristics” for parameters, and to Figure 15 for timing diagrams.

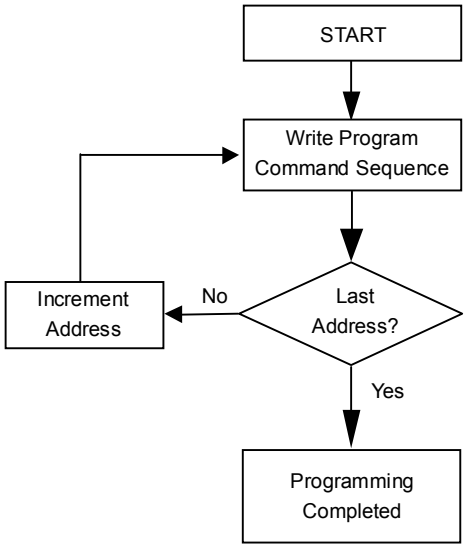


Figure 1. Program Operation

Note:
See Table 11 for program command sequence.

Accelerated Program Operation

The device offers accelerated program operation through the ACC function, which is one of the two functions provided by the WP#/ACC pin. This ACC function allows a faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, which temporarily unprotects any protected sectors and uses the high voltage V_{HH} on the pin to reduce the time required for program operation. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to the normal operation. Note that the WP#/ACC pin must not be set at V_{HH} for operations other than the accelerated program; otherwise the device may be damaged.

Table 1. AC29LV320 Device Operations

Operation	CE#	OE#	WE#	Reset#	WP#/ACC	Addresses (Note 2)	DQ0 ~ DQ7	DQ8-DQ15	
								Byte# $=V_{IH}$	Byte# $=V_{IL}$
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	D_{OUT}	DQ8-DQ14 =High-Z, DQ15=A-1
Write	L	H	L	H	(Note 3)	A_{IN}	(Note 4)	(Note 4)	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 4)	(Note 4)	
Standby	$V_{CC}\pm$ 0.3V	X	X	$V_{CC}\pm$ 0.3V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	L/H	SA, A6=L, A1=H, A0=L	(Note 4)	X	X
Sector Unprotect (Note 2)	L	H	L	V_{ID}	(Note 3)	SA, A6=H, A1=H, A0=L	(Note 4)	X	X
Temporary Sector Unprotect	X	X	X	V_{ID}	(Note 3)	A_{IN}	(Note 4)	(Note 4)	High-Z

Legend: L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5~12.5 V, V_{HH} = 11.5~12.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes:

1. Addresses are A20:A0 in word mode (BYTE# = V_{IH}), A20:A-1 in byte mode (BYTE# = V_{IL}).
2. The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.
3. If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP#/ACC = V_{HH}, all sectors will be unprotected.
4. D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm.

Besides, the WP#/ACC pin must not be left floating or unconnected; otherwise the device may be in inconsistent behavior.

Chip Erase

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Then, two additional unlock write cycles are issued, followed by the chip erase command. The system is not required to provide any controls or timings during these operations. Table 11 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Chip Erase operation are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. In order to ensure data integrity, the Chip Erase command sequence should be reinitiated once the device has returned to reading array data.

The system can determine the status of the erase operation by using DQ7, DQ6, or RY/BY#. See "Write Operation Status" for information about these status bits. When the Erase operation is complete, the device returns to reading array data and addresses are no longer latched.

Figure 2 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters.

Sector Erase

Sector erase is a six-bus-cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Then, two additional unlock write cycles

are issued, followed by the address of the sector to be erased, and the sector erase command. Table 11 shows the address and data requirements for the sector erase command sequence.

The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. Any command other than Sector Erase during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

A hardware reset during the sector erase operation immediately terminates the operation. In order to ensure data integrity, the Sector Erase command sequence should be reinitiated once the device has returned to reading array data.

Figure 2 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the “AC Characteristics” section for parameters, and the Figure 16 for timing diagrams.

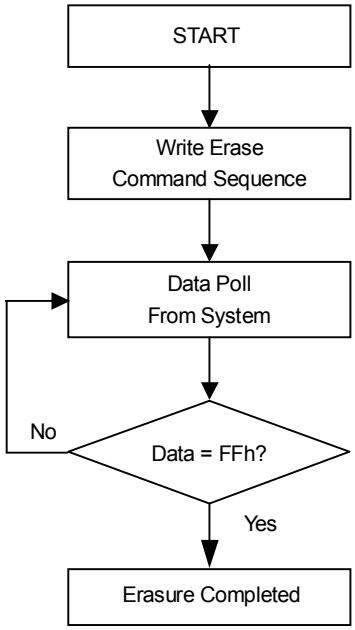


Figure 2. Erase Operation

Note:

See Table 11 for erase command sequence.

Page Erase

Page erase is a six-bus-cycle operation. The page erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Then, two additional unlock write cycles are issued, followed by the address of the page to be erased, and the page erase command. Table 11 shows the address and data requirements for the page erase command sequence.

The system is not required to provide any controls or timings during these operations.

Autoselect Mode

When the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7~DQ0. The standard read cycle timings are applied in this mode.

The autoselect mode provides manufacturer and device identification, and sector protection verification through identifier codes appearing on outputs DQ7–DQ0. This mode is primarily used for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. Besides, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins A6, A1, and A0 must be set as shown in Table 4**.** In addition, when verifying sector protection, the sector address must appear properly on the highest order address bits (see Tables 2 and 3). Table 4 shows the remaining address bits that are don’t care. After setting all

necessary bits as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can also issue the autoselect command via the command register, as shown in Table 11. This method does not require V_{ID}.

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 11 shows the address and data requirements. This method is an alternative to that shown in Table 4, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address within a sector that is in the read mode.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times without initiating another command sequence. When device is in word-wide configuration, the read cycles at addresses XX00h, XX03h and XX40h retrieve the manufacturer code, and the read cycle at address XX01h returns the device identification code. When device is in byte-wide configuration, the read cycles at addresses XX00h, XX06h and XX80h retrieve the manufacturer code, and the read cycle at address XX02h returns the device identification code. A read cycle containing a sector address (SA) and the address XX02h in word mode (or XX04h in byte mode) returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Tables 2 and 3 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Standby Mode

When the system is not reading from or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state and are independent of the OE# input. The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3V. Note that this is a more restricted voltage range than V_{IH}. If CE# and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3V, the device will be in the standby mode, but the standby current will be greater. When in either of these standby modes, the device requires standard access time (t_{CE}) for read access before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes device power consumption. The device enables automatically this mode when addresses are remain stable for t_{ACC} + 30ns. The automatic sleep mode is independent of the CE#, WE# and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC5} in the DC Characteristics table represents the automatic sleep mode current specification.

Hardware Reset Pin (RESET#)

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, sets all output pins in tri-state, and ignores all read/write commands during the period of RESET# pulse.

The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated after the device is ready to accept another command sequence. This function is to ensure the data integrity.

Current is reduced during the period of RESET# pulse. When RESET# is held at V_{SS} ± 0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS} ± 0.3 V, the standby current will be larger.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus reset the device also, enabling the system to read the boot-up firmware from the device.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains at “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY}. The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (i.e., the RY/BY# pin remains at “1”), the reset operation

is completed within a time of t_{READY}. The system can read data t_{RH} after the RESET# pin returns to V_{IH}. Refer to the AC Characteristics tables for RESET# parameters and to Figure 12 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Sector/Sector Block Protection and Unprotection

Note that the term "sector" applies to both sectors and sector blocks in the following discussion. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Tables 5 and 6).

The hardware sector protection can disable both program and erase operations in any sector. The hardware sector unprotection can re-enable both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods. The primary method requires V_{ID} on the RESET# pin, which can be implemented either in-system or via programming equipment. Figure 4 shows the algorithms and Figure 20 shows the timing diagram.

The alternate method mainly for programming equipment requires V_{ID} on address pin A9 and OE#. This method is compatible with programmer routines written for earlier 3.0 volt-only Actrans flash devices. The device is shipped with all sectors unprotected. Actrans System Inc. offers the option of programming and protecting sectors at its factory prior to shipping the device. Please contact an Actrans System Inc.'s representative for details.

It is possible to determine whether a sector is protected or unprotected. See the Autoselect Mode section for details.

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the WP#/ACC pin.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two "outermost" 8 Kbyte boot sectors regardless of whether those sectors were protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". The two outermost 8 Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts V_{IH} on the WP#/ACC pin, the two outermost 8 Kbyte boot sectors of the device reverts to protected or unprotected state that was set previously. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection".

Note that the WP#/ACC pin must not be left floating or unconnected to prevent the inconsistent behavior of the device.

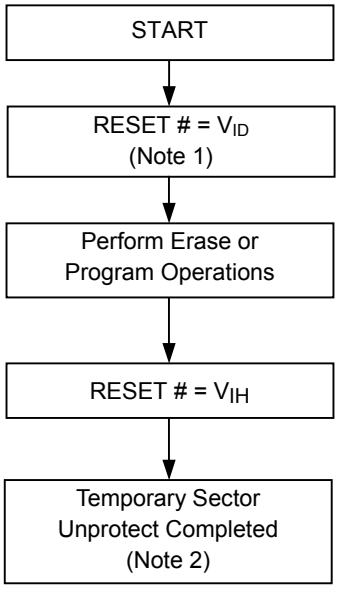


Figure 3. Temporary Sector Unprotect Operation

Notes:
1. All protected sectors are unprotected. (If WP#/ACC = V_{IL}, outermost boot sectors will remain protected).
2. All previously protected sectors are protected once again.

Table 2. AC29LV320T Top Boot Block Sector Address Table

Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA0	000000xxx	64/32	000000h-00FFFFh	000000h-007FFFh
SA1	000001xxx	64/32	010000h-01FFFFh	008000h-00FFFFh
SA2	000010xxx	64/32	020000h-02FFFFh	010000h-017FFFh
SA3	000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
SA4	000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
SA5	000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
SA6	000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
SA7	000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
SA8	001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
SA9	001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
SA10	001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
SA11	001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
SA12	001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
SA13	001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
SA14	001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
SA15	001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
SA16	010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
SA17	010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
SA18	010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
SA19	010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
SA20	010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
SA21	010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
SA22	010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
SA23	010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
SA24	011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
SA25	011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
SA26	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
SA27	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
SA28	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
SA29	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
SA30	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
SA31	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh
SA32	100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
SA33	100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
SA34	100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
SA35	100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
SA36	100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
SA37	100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
SA38	100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
SA39	100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh
SA40	101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
SA41	101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
SA42	101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
SA43	101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
SA44	101100xxx	64/32	2C0000h-2CFFFFh	160000h-167FFFh
SA45	101101xxx	64/32	2D0000h-2DFFFFh	168000h-16FFFFh

Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA46	101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
SA47	101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
SA48	110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
SA49	110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
SA50	110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
SA51	110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
SA52	110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
SA53	110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
SA54	110110xxx	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
SA55	110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
SA56	111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
SA57	111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
SA58	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
SA59	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
SA60	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
SA61	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
SA62	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
SA63	111111000	8/4	3F0000h-3F1FFFh	1F8000h-1F8FFFh
SA64	111111001	8/4	3F2000h-3F3FFFh	1F9000h-1F9FFFh
SA65	111111010	8/4	3F4000h-3F5FFFh	1FA000h-1FAFFFh
SA66	111111011	8/4	3F6000h-3F7FFFh	1FB000h-1FBFFFh
SA67	111111100	8/4	3F8000h-3F9FFFh	1FC000h-1FCFFFh
SA68	111111101	8/4	3FA0000h-3FBFFFh	1FD000h-1FDFFFh
SA69	111111110	8/4	3FC000h-3FDFFFh	1FE000h-1FEFFFh
SA70	111111111	8/4	3FE000h-3FFFFFh	1FF000h-1FFFFFh

Note: The address range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).

Table 3. AC29LV320B Bottom Boot Block Sector Addresses Table

Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA0	000000000	8/4	000000h-001FFFh	000000h-000FFFh
SA1	000000001	8/4	002000h-003FFFh	001000h-001FFFh
SA2	000000010	8/4	004000h-005FFFh	002000h-002FFFh
SA3	000000011	8/4	006000h-007FFFh	003000h-003FFFh
SA4	000000100	8/4	008000h-009FFFh	004000h-004FFFh
SA5	000000101	8/4	00A000h-00BFFFh	005000h-005FFFh
SA6	000000110	8/4	00C000h-00DFFFh	006000h-006FFFh
SA7	000000111	8/4	00E000h-00FFFFh	007000h-007FFFh
SA8	000001xxx	64/32	010000h-01FFFFh	008000h-00FFFFh
SA9	000010xxx	64/32	020000h-02FFFFh	010000h-017FFFh
SA10	000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
SA11	000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
SA12	000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
SA13	000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
SA14	000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
SA15	001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
SA16	001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
SA17	001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
SA18	001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
SA19	001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
SA20	001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
SA21	001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
SA22	001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
SA23	010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
SA24	010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
SA25	010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
SA26	010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
SA27	010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
SA28	010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
SA29	010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
SA30	010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
SA31	011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
SA32	011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
SA33	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
SA34	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
SA35	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
SA36	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
SA37	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
SA38	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh
SA39	100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
SA40	100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
SA41	100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
SA42	100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
SA43	100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
SA44	100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
SA45	100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh

Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA46	100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh
SA47	101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
SA48	101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
SA49	101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
SA50	101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
SA51	101100xxx	64/32	2C0000h-2CFFFFh	160000h-167FFFh
SA52	101101xxx	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
SA53	101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
SA54	101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
SA55	110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
SA56	110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
SA57	110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
SA58	110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
SA59	110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
SA60	110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
SA61	110110xxx	64/32	360000h-36FFFFh	1B8000h-1B7FFFh
SA62	110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
SA63	111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
SA64	111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
SA65	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
SA66	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
SA67	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
SA68	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
SA69	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
SA70	111111xxx	64/32	3F0000h-3FFFFFh	1F8000h-1FFFFFFh

Note: The address range is A20:A-1 in byte mode (BYTE#=V_{IL}) or A20:A0 in word mode (BYTE#=V_{IH}).

Table 4. AC29LV320 Autoseclet Codes (High Voltage Method)

Description	CE#	OE#	WE#	A20 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A2	A1	A0	DQ8 to DQ15		DQ7 to DQ0
												BYTE# = V_{IH}	BYTE# = V_{IL}	
Manufacturer ID: ACTRANS	L	L	H	X	X	V_{ID}	X	L	X	L	L	X	X	7Fh
								L		H	H			7Fh
								H		L	L			1Fh
Device ID: AC29LV320	L	L	H	X	X	V_{ID}	X	L	X	L	H	22h	X	18h (T), 19h (B)
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	H	L	X	X	01h (protected) 00h (unprotected)

Legend: T = Top Boot Block, B = Bottom Boot Block, L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Table 5. Top Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector	A20-A12	Sector/Sector Block Size
SA0-SA3	000000XXX 000001XXX 000010XXX 000011XXX	256 (4 x 64) Kbytes
SA4-SA7	0001XXXXX	256 (4 x 64) Kbytes
SA8-SA11	0010XXXXX	256 (4 x 64) Kbytes
SA12-SA15	0011XXXXX	256 (4 x 64) Kbytes
SA16-SA19	0100XXXXX	256 (4 x 64) Kbytes
SA20-SA23	0101XXXXX	256 (4 x 64) Kbytes
SA24-SA27	0110XXXXX	256 (4 x 64) Kbytes
SA28-SA31	0111XXXXX	256 (4 x 64) Kbytes
SA32-SA35	1000XXXXX	256 (4 x 64) Kbytes
SA36-SA39	1001XXXXX	256 (4 x 64) Kbytes
SA40-SA43	1010XXXXX	256 (4 x 64) Kbytes
SA44-SA47	1011XXXXX	256 (4 x 64) Kbytes
SA48-SA51	1100XXXXX	256 (4 x 64) Kbytes
SA52-SA55	1101XXXXX	256 (4 x 64) Kbytes
SA56-SA59	1110XXXXX	256 (4 x 64) Kbytes
SA60-SA62	111100XXX 111101XXX 111110XXX	192 (3 x 64) Kbytes
SA63	111111000	8 Kbytes
SA64	111111001	8 Kbytes
SA65	111111010	8 Kbytes
SA66	111111011	8 Kbytes
SA67	111111100	8 Kbytes
SA68	111111101	8 Kbytes
SA69	111111110	8 Kbytes
SA70	111111111	8 Kbytes

Table 6 Bottom Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector	A20-A12	Sector/Sector Block Size
SA70-SA67	111111XXX 111110XXX 111101XXX 111100XXX	256 (4 x 64) Kbytes
SA66-SA63	1110XXXXX	256 (4 x 64) Kbytes
SA62-SA59	1101XXXXX	256 (4 x 64) Kbytes
SA58-SA55	1100XXXXX	256 (4 x 64) Kbytes
SA54-SA51	1011XXXXX	256 (4 x 64) Kbytes
SA50-SA47	1010XXXXX	256 (4 x 64) Kbytes
SA46-SA43	1001XXXXX	256 (4 x 64) Kbytes
SA42-SA39	1000XXXXX	256 (4 x 64) Kbytes
SA38-SA35	0111XXXXX	256 (4 x 64) Kbytes
SA34-SA31	0110XXXXX	256 (4 x 64) Kbytes
SA30-SA27	0101XXXXX	256 (4 x 64) Kbytes
SA26-SA23	0100XXXXX	256 (4 x 64) Kbytes
SA22-SA19	0011XXXXX	256 (4 x 64) Kbytes
SA18-SA15	0010XXXXX	256 (4 x 64) Kbytes
SA14-SA11	0001XXXXX	256 (4 x 64) Kbytes
SA10-SA8	000011XXX 000010XXX 000001XXX	192 (3 x 64) Kbytes
SA7	000000111	8 Kbytes
SA6	000000110	8 Kbytes
SA5	000000101	8 Kbytes
SA4	000000100	8 Kbytes
SA3	000000011	8 Kbytes
SA2	000000010	8 Kbytes
SA1	000000001	8 Kbytes
SA0	000000000	8 Kbytes

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID} (11.5V~12.5V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 3 shows the algorithm, and Figure 19 shows the timing diagrams of this feature.

Hardware Data Protection

The command sequence with the requirement of unlock cycles for programming or erasure provides data protection against inadvertent writes (refer to Table 11 for command definitions).

In addition, the following hardware data protection features can prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. This feature protects data during V_{CC} power-up and power-down. When V_{CC} becomes greater than V_{LKO}, the system must provide the proper signals to the control pins to prevent unintentional writes.

Noise/Glitch Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

Write Inhibit Mode

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = $V_{IH,}$ or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE#=CE#=V_{IL} and OE#=V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ6, DQ7, and RY/BY#. Table 12 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether a Program or Erase operation is in progress or has been completed.

Data# Polling (DQ7)

The Data# Polling bit, DQ7, indicates whether a Program or Erase operation is in progress or completed. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Program operation, the device output on DQ7 is complement to the datum programmed to DQ7. When the Program operation is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1μs, then the device returns to reading array data.

During the Erase operation, Data# Polling produces a “0” on DQ7. When the Erase operation is complete, Data# Polling produces a “1” on DQ7. This is analogous to the complement/true datum output described for the Program operation: the erase function changes all the bits in a sector to “1”; prior to this, the device outputs the “complement”, or “0”. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 μs, then the device returns to reading array data. If not all selected sectors are protected, the Erase operation erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

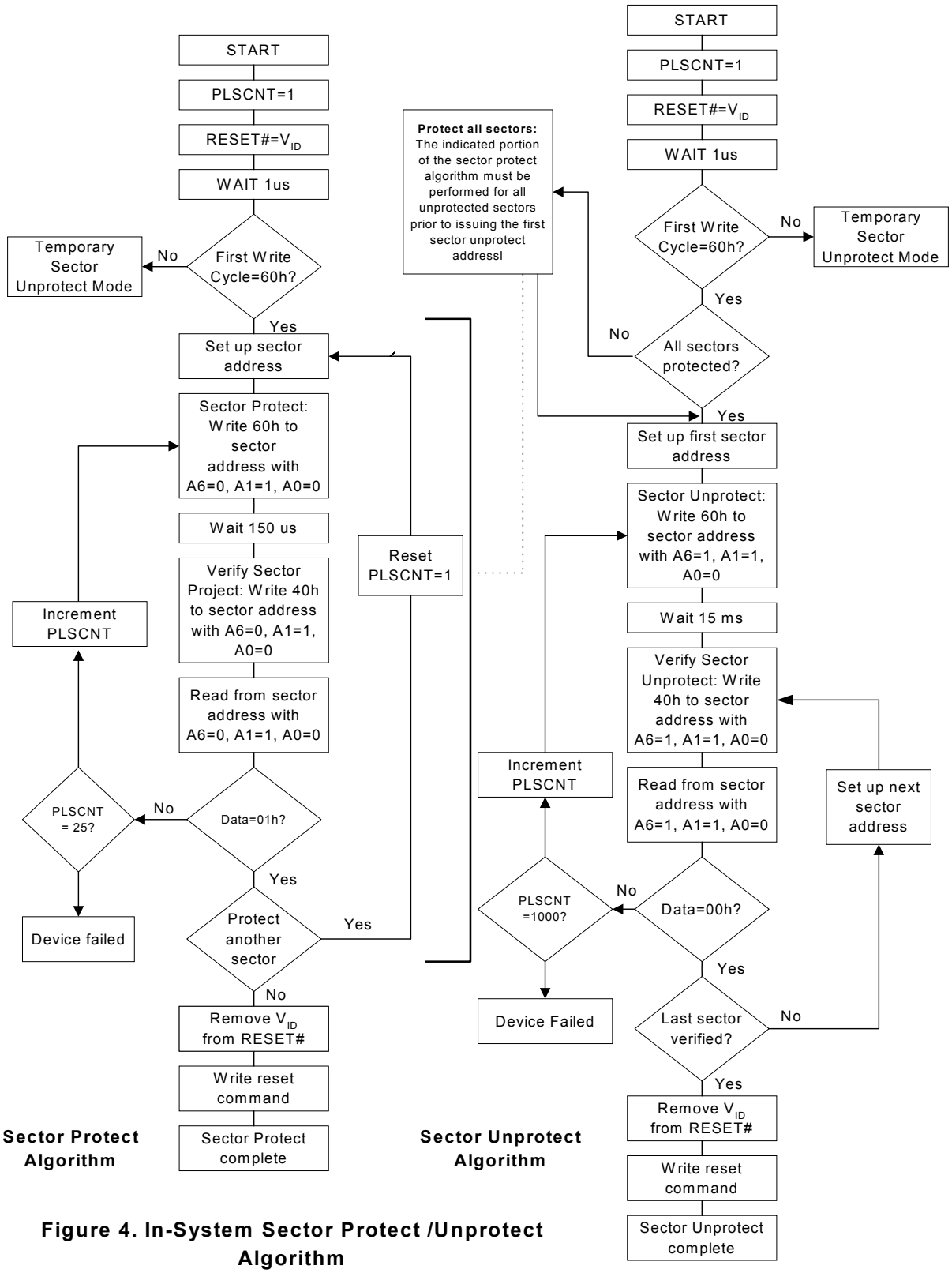


Figure 4. In-System Sector Protect /Unprotect Algorithm

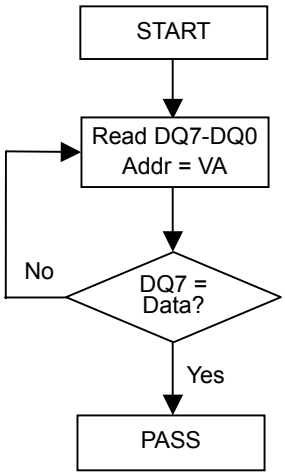


Figure 5. Data# Polling Algorithm

Notes:
VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.

Just prior to the completion of a Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Thus, depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0–DQ7 will appear on successive read cycles.

Table 12 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 17 in the AC Characteristics section shows the Data# Polling timing diagram.

Ready/Busy# (RY/BY#)

The RY/BY# is a dedicated, open-drain output pin that indicates whether a Program or Erase operation is complete or in progress. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel and connect to V_{CC} with a pull-up resistor.

If the output is low (Busy), the device is actively erasing or programming. If the output is high (Ready), the device is ready to read array data, or is in the standby mode.

Toggle Bit (DQ6)

The “Toggle Bit” on DQ6 indicates whether a Program or Erase operation is complete or in progress. Toggle Bit may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During a Program or Erase operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Erase operation erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 to determine whether a sector is actively erasing. When the device is actively erasing (i.e., the Erase operation is in progress), DQ6 toggles. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

Table 12 shows the outputs for Toggle Bit on DQ6. Figure 6 shows the toggle bit algorithm. Figure 18 in the “AC Characteristics” section shows the toggle bit timing diagrams.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines the device and the host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for the entire families of the devices. Software support can then be device-independent,

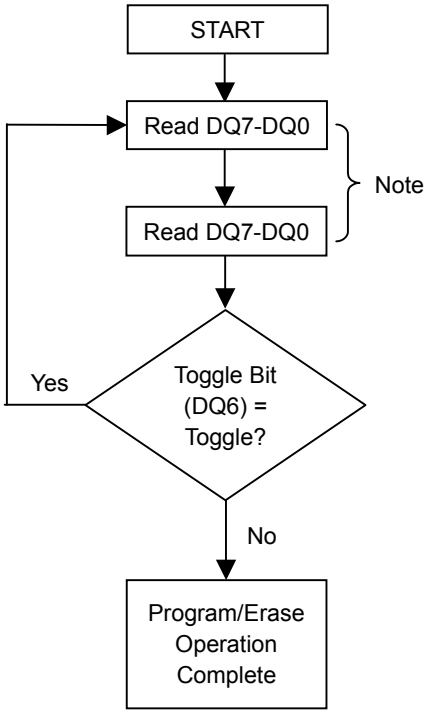


Figure 6. Toggle Bit Algorithm

Notes:
Read toggle bit twice to determine whether or not it is toggling (see text).

JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 7–10. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 7–9. The system must write the reset command to return the device to the autoselect mode.

Table 7 CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 8. System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. Voltage (00h=no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. Voltage (00h=no V_{PP} pin present)
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout for Min size buffer write 2^N µs (00h = not supported)
21h	42h	0004h	Typical timeout per individual block erase 2^N ms
22h	44h	0008h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0001h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0002h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0002h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 9 Device Geometry Definitions

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0016h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information
31h 32h 33h 34h	62h 64h 66h 68h	003Eh 0000h 0000h 0001h	Erase Block Region 2 Information
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 10. Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0031h	Minor version number, ASCII
45h	8Ah	0000h	Address Sensitive Unlock (Bits 1-0) 0=Required, 1 = Not required Silicon Revision Number (Bits 7-2)
46h	8Ch	0000h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write)
47h	8Eh	0004h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004	Sector Protect/Unprotect scheme 04 = 29LV800 mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported,
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page 02 = 8 Word Page
4Dh	9Ah	0000h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	0000h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	000Xh	Top/Bottom Boot Sector Flag 02h= Bottom Boot Device, 03h= Top Boot Device

Table 11. AC29LV320 Command Definitions

Command Sequence (Note 1)			Cycle	Bus Cycles (Notes 2-5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 6)			1	RA	RD										
Reset (Note 7)			1	XXX	F0										
Autoselect (Note 8)	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	7F				
		Byte		AAA		555		AAA		X00					
		Word	4	555	AA	2AA	55	555	90	X03	7F				
		Byte		AAA		555		AAA		X06					
		Word	4	555	AA	2AA	55	555	90	X40	1F				
		Byte		AAA		555		AAA		X80					
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	90	X01	2218				
		Byte		AAA		555		AAA		X02	18				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	555	90	X01	2219				
		Byte		AAA		555		AAA		X02	19				
	Sector/Sector Block Protect Verify (Note 9)	Word	4	555	AA	2AA	55	555	90	(SA) X02	00/ 01				
		Byte		AAA		555		AAA		(SA) X04					
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program (Note 10)			2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 11)			2	PA	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Page Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	PEA	20
		Byte		AAA		555		AAA		AAA		555			
CFI Query (Note 12)		Word	1	55	98										
		Byte		AA											

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A20–A12 uniquely select any sector.

PEA = Address of the page to be erased. Address bits A20–A8 uniquely select any page.

Notes:

1. See Table 1 for description of bus operations.
2. All values are in hexadecimal.

3. Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.
4. Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.
5. Unless otherwise noted, address bits A20–A11 are don't cares.
6. No unlock or command cycles required when device is reading array data.
7. The Reset command is required to return to the read mode when a device is in the autoselect mode.
8. The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See the Autoselect Command Sequence section for more information.
9. The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.
10. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
11. The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.
12. Command is valid when device is ready to read array data or when device is in autoselect mode.

Table 12. Write Operation Status

Status	DQ7 (Note)	DQ6	RY/BY#
Program	DQ7#	Toggle	0
Erase	0	Toggle	0

Note: DQ7 requires a valid address when reading status information. Refer to the appropriate subsection for further details.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Plastic Packages …… –65°C to 150°C
Ambient Temperature with Power Applied. ……..…..…….. –65°C to 125°C
Voltage with Respect to Ground V_{CC} (Note 1)…… –0.5 V to +4.0 V
A9, OE#, and RESET# (Note 2)…….…… –0.5 V to +12.5 V
All Other Pins (Note 1)……..……..….. –0.5 V to V_{CC} +0.5 V
Output Short Circuit Current (Note 3)……... 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 8.
2. Minimum DC input voltage on pins A9, OE#, WP#/ACC and RESET# is –0.5 V. During voltage transitions, A9, OE#, WP#/ACC and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 7. Maximum DC input voltage on pin A9 is +12.5 V, which may overshoot to 14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is 9.5V which may overshoot to +12.0V for periods up to 20ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

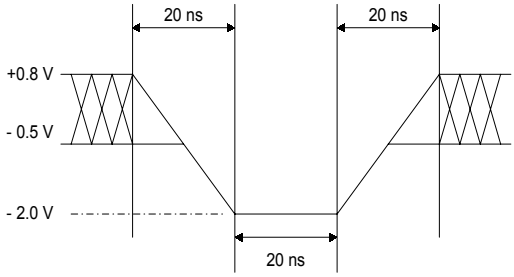


Figure 7. Maximum Negative Overshoot Waveform

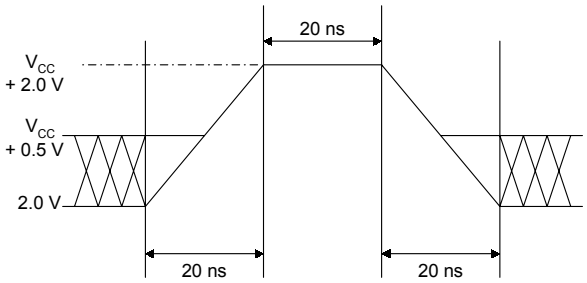


Figure 8. Maximum Positive Overshoot Waveform

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A)…..……0°C to 70°C
Industrial (I) Devices
Ambient Temperature (T_A)……..…–40°C to 85°C
Extended (E) Devices
Ambient Temperature (T_A)……–55°C to 125°C

V_{CC} Supply Voltages
V_{CC} for full voltage range…….. 2.7 V to 3.6 V

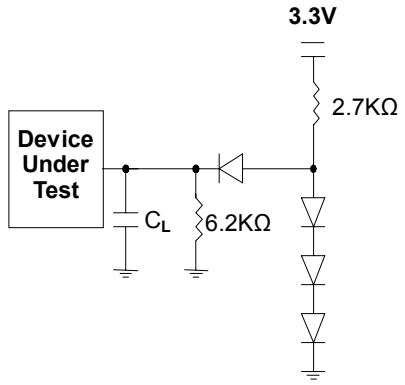
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS
CMOS Compatible

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN}=V_{SS}$ to V_{CC}, $V_{CC}=V_{CC\ max}$				±3.0	μA
I_{LIT}	A9 Input Load Current	$V_{CC}=V_{CC\ max}$; A9=12.5V				35	μA
I_{LO}	Output Leakage Current	$V_{OUT}=V_{SS}$ to V_{CC}, $V_{CC}=V_{CC\ max}$				±1.0	μA
I_{CC1}	V_{CC} Active Read Current (Note 1,2)	CE#=V_{IL}, OE#=V_{IH}, Byte Mode	5 MHz		10	16	mA
			1 MHz		2	4	
		CE# =V_{IL}, OE# =V_{IH}, Word Mode	5 MHz		10	16	
			1 MHz		2	4	
I_{CC2}	V_{CC} Active Write Current (Note 2, 3)	CE#=V_{IL}, OE#=V_{IH} WE#=V_{IL}			15	30	mA
I_{CC3}	V_{CC} Standby Current (Note 2)	CE#, Reset#=V_{CC}±0.3V			0.2	5	μA
I_{CC4}	V_{CC} Reset Current (Note 2)	Reset#=V_{SS}±0.3V			0.2	5	μA
I_{CC5}	Automatic Sleep Mode (Notes 2, 4)	$V_{IH}=V_{CC}$±0.3V; $V_{IL}=V_{SS}$±0.3V			0.2	5	μA
I_{ACC}	ACC Accelerated Program Current, Word or Byte	CE#=V_{IL}, OE#=V_{IH}	ACC pin		5	10	mA
			V_{CC} pin		15	30	mA
V_{IL}	Input Low Voltage			-0.5		0.8	V
V_{IH}	Input High Voltage			0.7 x V_{CC}		V_{CC} +0.3	V
V_{HH}	Voltage for WP#/ACC Sector Protect /Unprotect and Program Acceleration	V_{CC}=3.0 V ± 10%		9		12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC}=3.0 V ± 10%		9		12.5	V
V_{OL}	Output Low Voltage	I_{OL}=4.0mA, $V_{CC}=V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH}=-2.0mA, $V_{CC}=V_{CC\ min}$		0.85 V_{CC}			V
V_{OH2}		I_{OH}=-100μA, $V_{CC}=V_{CC\ min}$		V_{CC}-0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 5)			2.3		2.5	V

Notes:
1. The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.
2. Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC\ max}$.
3. I_{CC} active while Erase or Program is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.
5. Not 100% tested.

TEST CONDITIONS



Note: Diodes are IN3064 or equivalent

Figure 9. Test Setup

Table 13. Test Specifications

Test Conditions	90	120	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0-3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

KEY TO SWITCHING WAVEFORMS

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is high Impedance State (High Z)

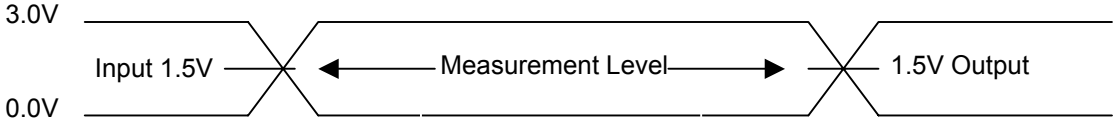


Figure 10. Input Waveforms and Measurement Levels

AC CHARACTERISTICS
Read Operations

Parameter		Description		Test Setup		Speed Options		Unit
JEDEC	Std					90	120	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	90	120	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#=V_{IL}, OE#=V_{IL}	Max	90	120	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay			Max	90	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		OE#=V_{IL}	Max	40	50	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	30	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	30	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	0		ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns

Notes:
1. Not 100% tested.
2. See Figure 9 and Table 13 for test specifications.

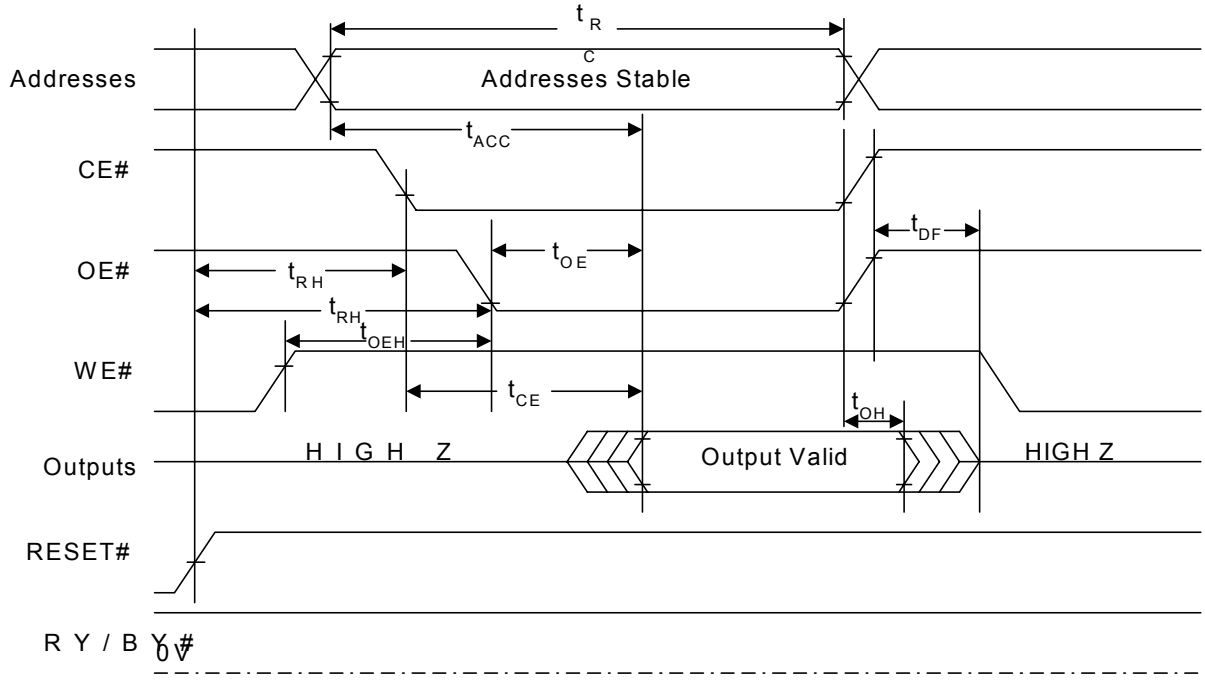
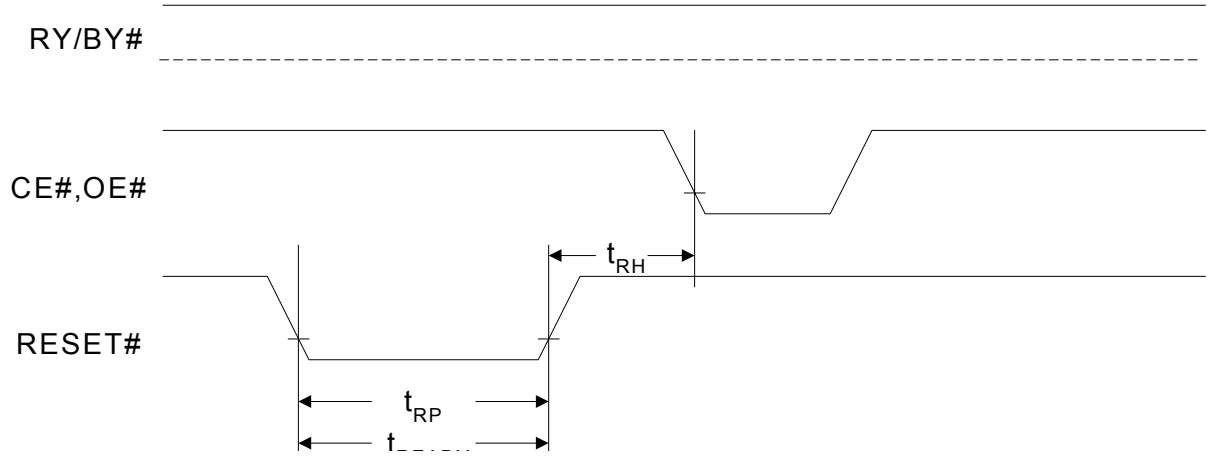


Figure 11. Read Operation Timings

AC CHARACTERISTICS
Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	μs
	t_{READY}	RESET# Pin Low (Not During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	μs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: Not 100% tested.



Reset Timings NOT during Program or Erase operations

Reset Timings during Program or Erase

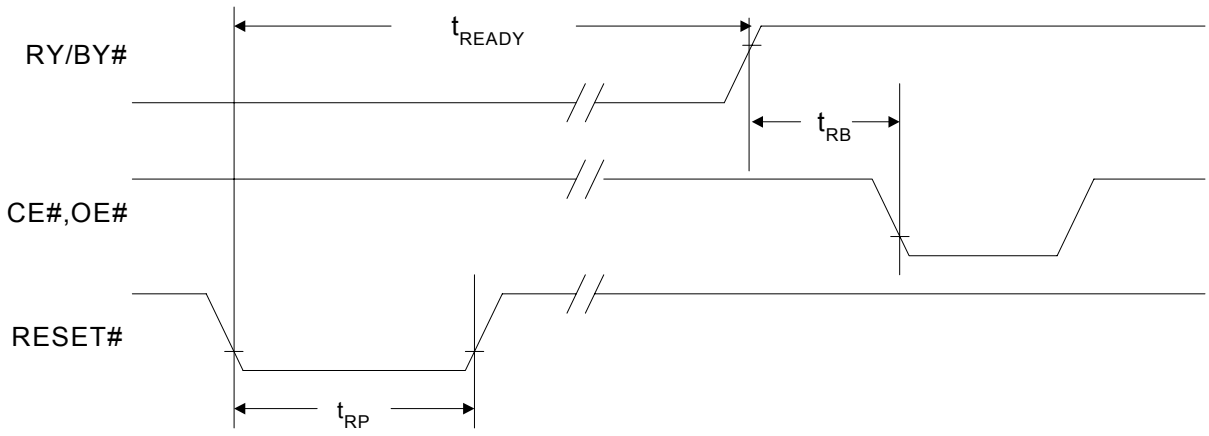


Figure 12. Reset# Timings

AC CHARACTERISTICS
Word/Byte Configurations (Byte#)

Parameter		Description		Speed Options		Unit
JEDEC	Std			90	120	
	t_{ELFL}/t_{ELFH}	CE# to Byte# Switching Low or High	Max	5		ns
	t_{FLQZ}	BYTE# Switching Low to Output HIGH Z	Max	30	30	ns
	t_{FHQV}	BYTE# Switching High to Output Active	Min	90	120	ns

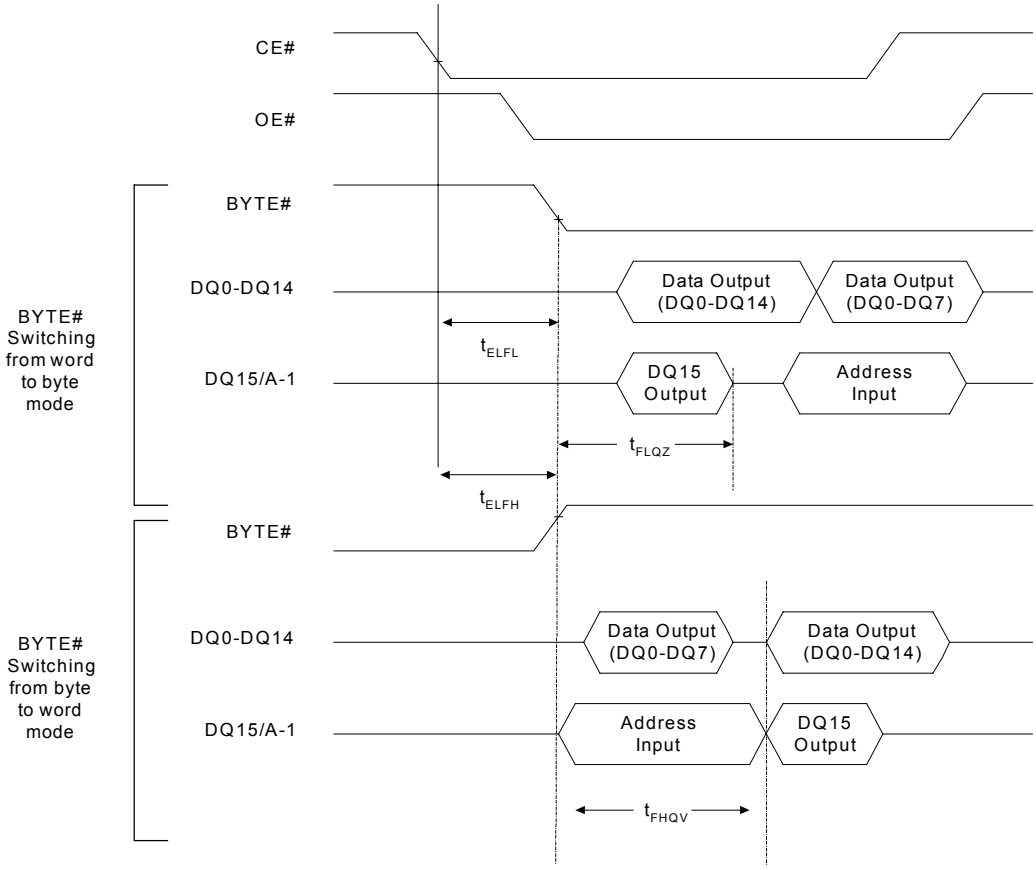
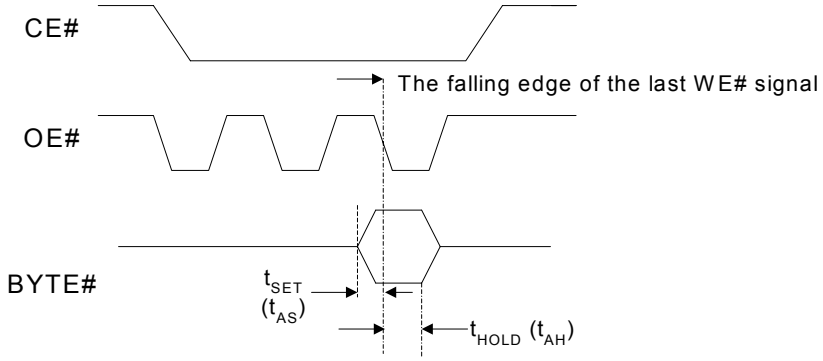


Figure 13. BYTE# Timings for Read Operations



Note: Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications

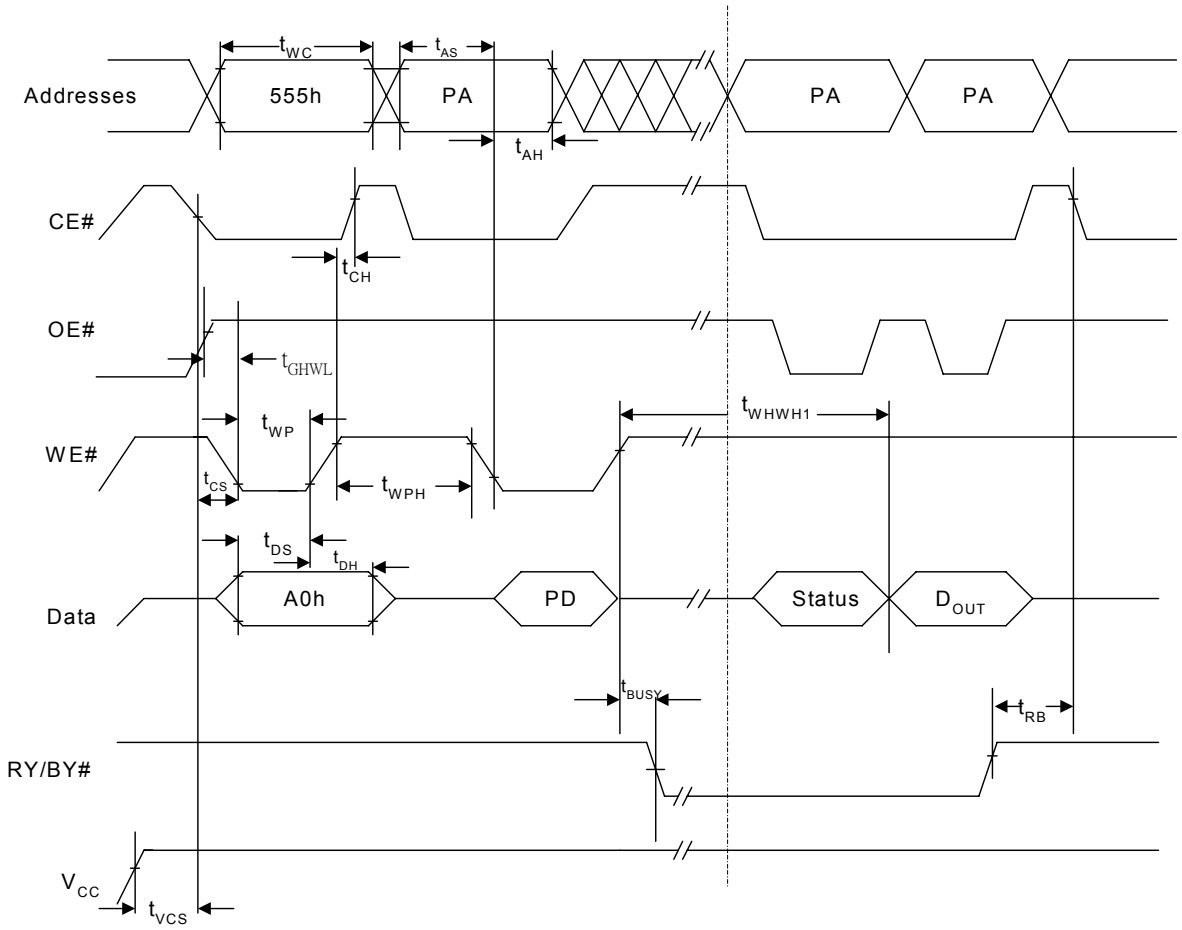
Figure 14. BYTE# Timings for Write Operations

AC CHARACTERISTICS
Erase/Program Operations

Parameter		Description			Speed Options		Unit
JEDEC	Std				90	120	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0		ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	50	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9		µs
			Word	Typ	11		
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	20		ms
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50		µs
	t_{RB}	Write Recovery Time from RY/BY#		Min	0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Min	90		ns

Notes:
1. Not 100% tested.
2. See the “Erase and Programming Performance“ section for more information.

AC CHARACTERISTICS

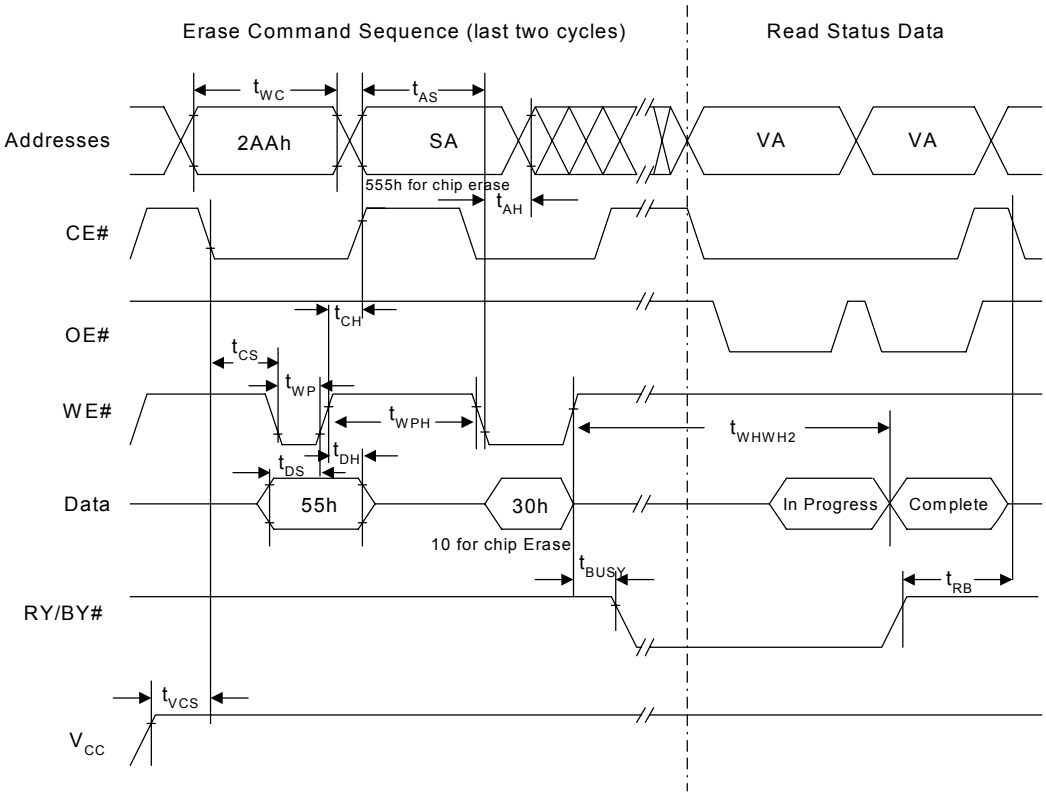


Notes:

1. PA= program address, PD=program data, D_{OUT} is the true data at the program address.
2. Illustration shows device in word mode.

Figure 15. Program Operation Timings

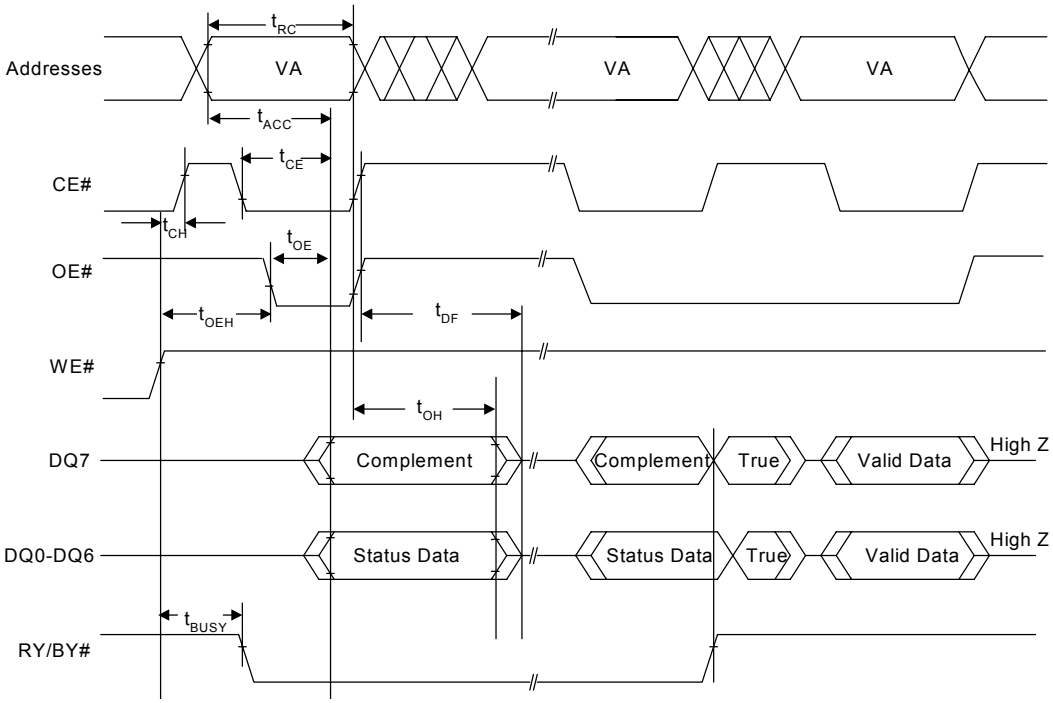
AC CHARACTERISTICS



Notes:
1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see “Write Operation Status”)
2. Illustration shows device in word mode.

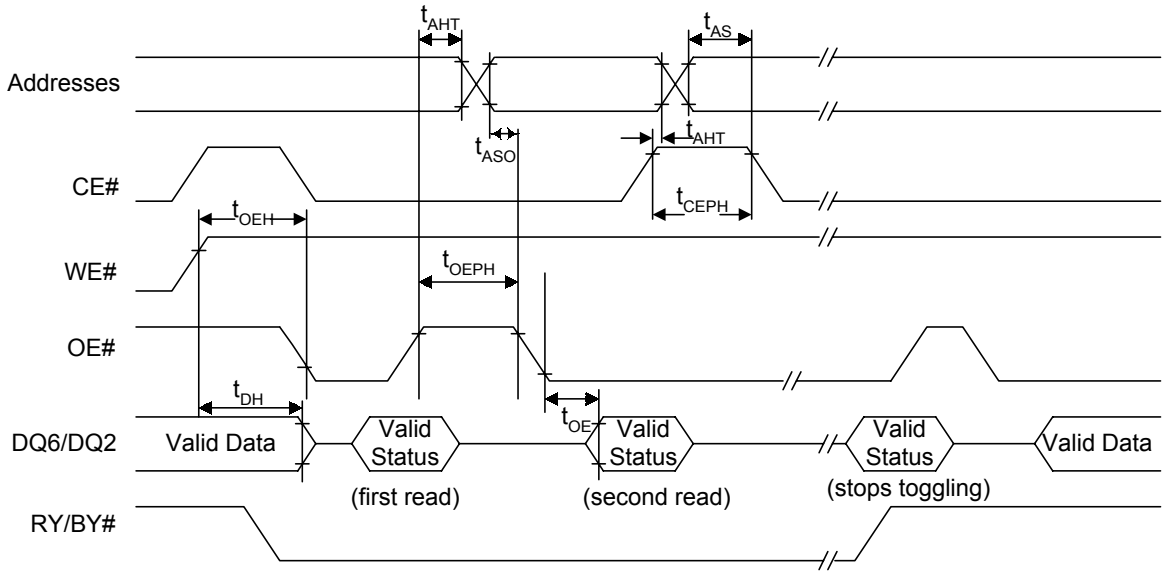
Figure 16. Chip/Sector Erase Timings

AC CHARACTERISTICS



Note: VA=Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 17. Data# Polling Timings



Note: VA=Valid address; not required for DQ6. Illustration shows first two status cycles after command sequences, last status read cycle, and array data read cycle.

Figure 18. Toggle Bit Timings

AC CHARACTERISTICS
Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	µs

Note: Not 100% tested.

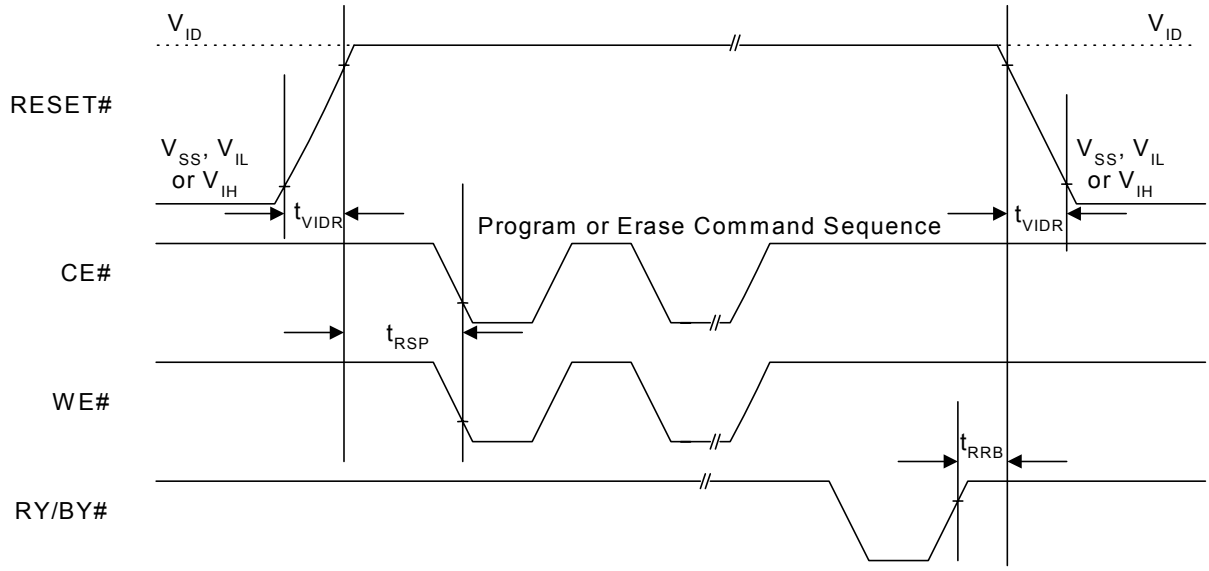
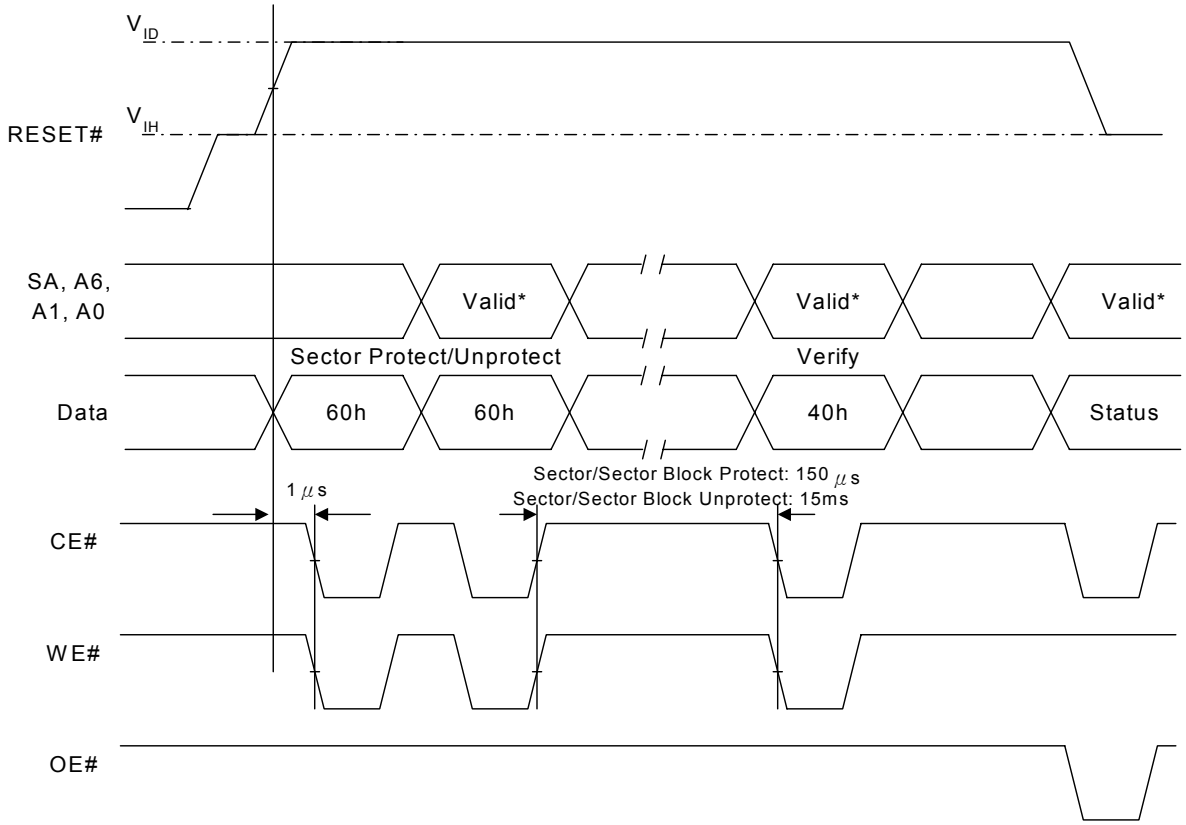


Figure 19. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS



*For sector protect, A6=0, A1=1, A0=0. For sector unprotect, A6=1, A1=1, A0=0

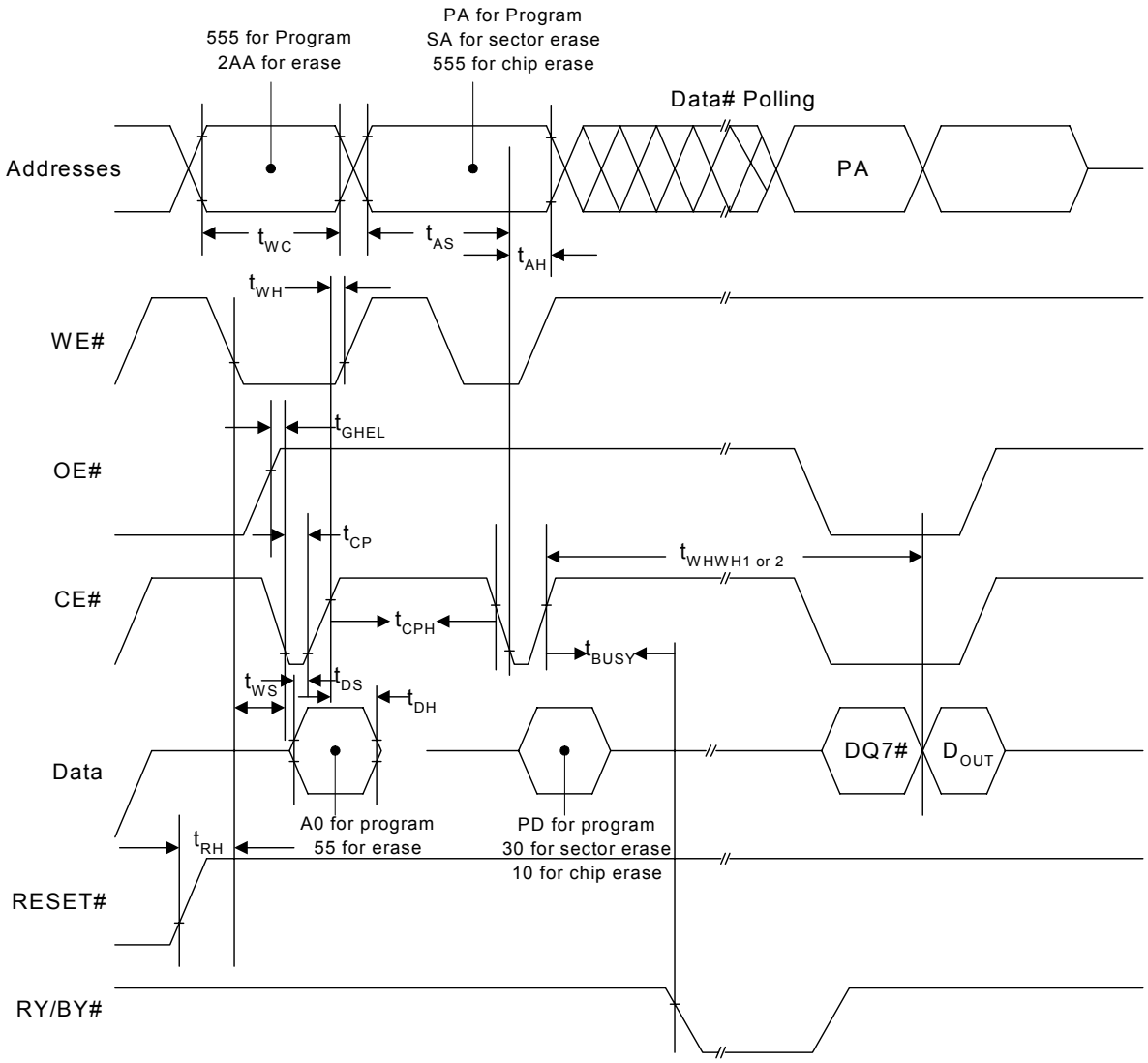
Figure 20. Sector/Sector Block Protect and Unprotect Timing Diagram

AC CHARACTERISTICS
Alternate CE# Controlled Erase/Program Operations

Parameter		Description			Speed Options		Unit
JEDEC	Std				90	120	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OES}	Output Enable Setup Time		Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0		ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	45	50	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Byte	Typ	9		µs
			Word	Typ	11		
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	20		ms

Notes:
1. Not 100% tested.
2. See the “Erase and Programming Performance“ section for more information.

AC CHARACTERISTICS



Notes:

1. Figure indicates last two bus cycles of a program or erase operation.
2. PA=program address, SA=sector address, PD=program data.
3. DQ7# is the complement of the data written to the device. DOUT is the data written to the device.
4. Waveforms are for the word mode.

Figure 21. Alternate CE# Controlled Write (Erase/Program)

Erase and Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		20		ms	
Chip Erase Time		500		ms	
Byte Program Time		9	20	μs	Excludes system level overhead (Note 3)
Accelerated Byte/Word Program Time		7	18	μs	
Word Program Time		11	22	μs	
Chip Program Time	Byte Mode	30		sec	
	Word Mode	24			

Notes:
1. Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 100,000 cycles. Additionally, programming typical assume checkerboard pattern.
2. Under worst-case conditions of 90°C, V_{CC} = 2.7 V, 100,000 cycles.
3. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 11 for further information on command definitions.
4. The device has a typical erase and program cycle endurance of 100,000 cycles.

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins expect I/O pins (including A9, OE#, and RESET#)	-1.0V	12.5V
Input voltage with respect to V_{SS} on all I/O pins	-1.0V	V_{CC} + 1.0V
V_{CC} Current	-100mA	+100mA

Notes: Includes all pins except V_{CC}. Test conditions: V_{CC} =3.0V, one pin at a time.

TSOP AND SO PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN}=0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN}=0	7.5	9	pF

Notes:
1. Samples, not 100% tested.
2. Test conditions T_A=25°C, f=1.0MHz.

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years