

# MC14541B

## Programmable Timer

The MC14541B programmable timer consists of a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, an automatic power-on reset circuit, and output control logic.

Timing is initialized by turning on power, whereupon the power-on reset is enabled and initializes the counter, within the specified  $V_{DD}$  range. With the power already on, an external reset pulse can be applied. Upon release of the initial reset command, the oscillator will oscillate with a frequency determined by the external RC network. The 16-stage counter divides the oscillator frequency ( $f_{OSC}$ ) with the  $n^{th}$  stage frequency being  $f_{OSC}/2^n$ .

- Available Outputs  $2^8$ ,  $2^{10}$ ,  $2^{13}$  or  $2^{16}$
- Increments on Positive Edge Clock Transitions
- Built-in Low Power RC Oscillator ( $\pm 2\%$  accuracy over temperature range and  $\pm 20\%$  supply and  $\pm 3\%$  over processing at  $< 10$  kHz)
- Oscillator May Be Bypassed if External Clock Is Available (Apply external clock to Pin 3)
- External Master Reset Totally Independent of Automatic Reset Operation
- Operates as  $2^n$  Frequency Divider or Single Transition Timer
- $Q/\bar{Q}$  Select Provides Output Logic Level Flexibility
- Reset (auto or master) Disables Oscillator During Resetting to Provide No Active Power Dissipation
- Clock Conditioning Circuit Permits Operation with Very Slow Clock Rise and Fall Times
- Automatic Reset Initializes All Counters On Power Up
- Supply Voltage Range = 3.0 Vdc to 18 Vdc with Auto Reset Disabled (Pin 5 =  $V_{DD}$ )  
= 8.5 Vdc to 18 Vdc with Auto Reset Enabled (Pin 5 =  $V_{SS}$ )

### MAXIMUM RATINGS\* (Voltages Referenced to $V_{SS}$ )

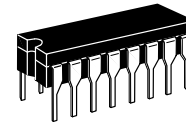
Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage	- 0.5 to + 18.0	V
$V_{in}, V_{out}$	Input or Output Voltage (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}$	Input Current (DC or Transient), per Pin	$\pm 10$	mA
$I_{out}$	Output Current (DC or Transient), per Pin	$\pm 45$	mA
$P_D$	Power Dissipation, per Package†	500	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

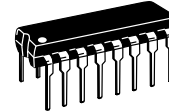
† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



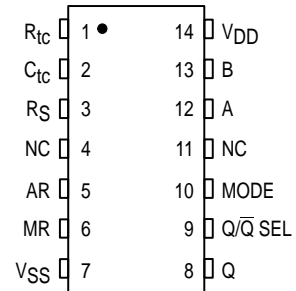
**D SUFFIX**  
SOIC  
CASE 751A

### ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

$T_A = -55^\circ$  to  $125^\circ\text{C}$  for all packages.

### PIN ASSIGNMENT



NC = NO CONNECTION

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95		—
			10	9.95	—	9.95	10	—	9.95		—
			15	14.95	—	14.95	15	—	14.95		—
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5		—
			10	7.0	—	7.0	5.50	—	7.0		—
			15	11	—	11	8.25	—	11		—
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-7.96	—	-6.42	-12.83	—	-4.49	—	mAdc	
		10	-4.19	—	-3.38	-6.75	—	-2.37	—		
		15	-16.3	—	-13.2	-26.33	—	-9.24	—		
	Sink I <sub>OL</sub>	5.0	1.93	—	1.56	3.12	—	1.09	—		
		10	4.96	—	4.0	8.0	—	2.8	—		
		15	19.3	—	15.6	31.2	—	10.9	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Pin 5 is High) Auto Reset Disabled	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Auto Reset Quiescent Current (Pin 5 is low)	I <sub>DDR</sub>	10	—	250	—	30	250	—	1500	μAdc	
		15	—	500	—	82	500	—	2000		
Supply Current**† (Dynamic plus Quiescent)	I <sub>D</sub>	5.0	I <sub>D</sub> = (0.4 μA/kHz) f + I <sub>DD</sub>							μAdc	
10	I <sub>D</sub> = (0.8 μA/kHz) f + I <sub>DD</sub>										
15	I <sub>D</sub> = (1.2 μA/kHz) f + I <sub>DD</sub>										

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†When using the on chip oscillator the total supply current (in μAdc) becomes: I<sub>T</sub> = I<sub>D</sub> + 2 C<sub>tc</sub> V<sub>DD</sub> f x 10<sup>-3</sup> where I<sub>D</sub> is in μA, C<sub>tc</sub> is in pF, V<sub>DD</sub> in Volts DC, and f in kHz. (see Fig. 3) Dissipation during power-on with automatic reset enabled is typically 50 μA @ V<sub>DD</sub> = 10 Vdc.

**This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.**

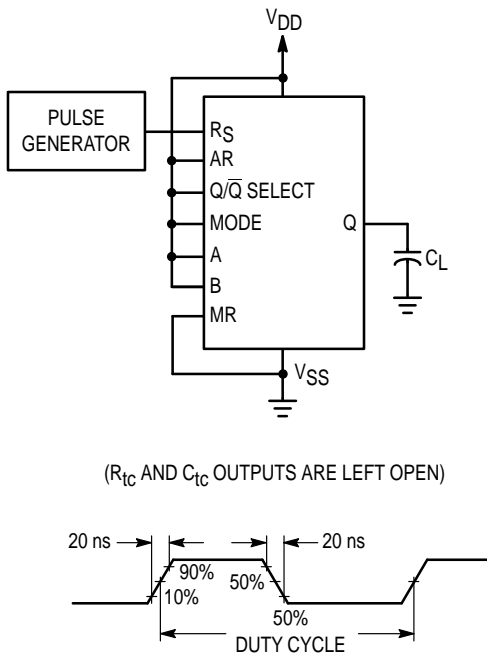
**Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.**

**SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

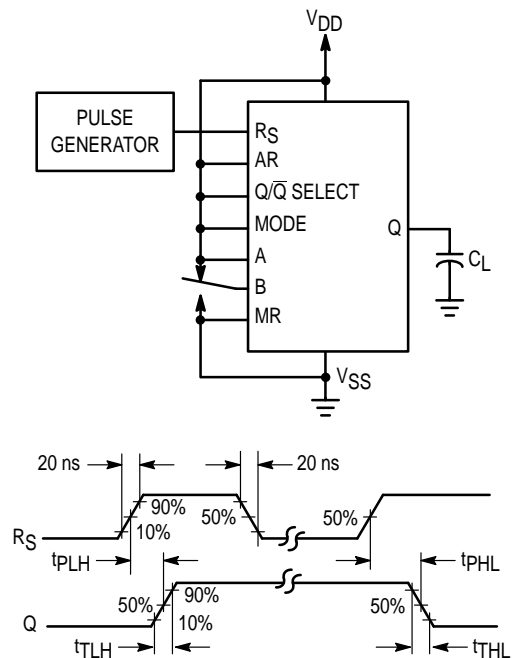
Characteristic	Symbol	V <sub>DD</sub>	Min	Typ #	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH}, t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay, Clock to Q (2 <sup>8</sup> Output) $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 3415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 1217 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 875 \text{ ns}$	$t_{PLH}, t_{PHL}$	5.0 10 15	— — —	3.5 1.25 0.9	10.5 3.8 2.9	μs
Propagation Delay, Clock to Q (2 <sup>16</sup> Output) $t_{PHL}, t_{PLH} = (1.7 \text{ ns/pF}) C_L + 5915 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.66 \text{ ns/pF}) C_L + 3467 \text{ ns}$ $t_{PHL}, t_{PLH} = (0.5 \text{ ns/pF}) C_L + 2475 \text{ ns}$	$t_{PHL}, t_{PLH}$	5.0 10 15	— — —	6.0 3.5 2.5	18 10 7.5	μs
Clock Pulse Width	$t_{WH}(cl)$	5.0 10 15	900 300 225	300 100 85	— — —	ns
Clock Pulse Frequency (50% Duty Cycle)	$f_{cl}$	5.0 10 15	— — —	1.5 4.0 6.0	0.75 2.0 3.0	MHz
MR Pulse Width	$t_{WH}(R)$	5.0 10 15	900 300 225	300 100 85	— — —	ns
Master Reset Removal Time	$t_{rem}$	5.0 10 15	420 200 200	210 100 100	— — —	ns

\* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

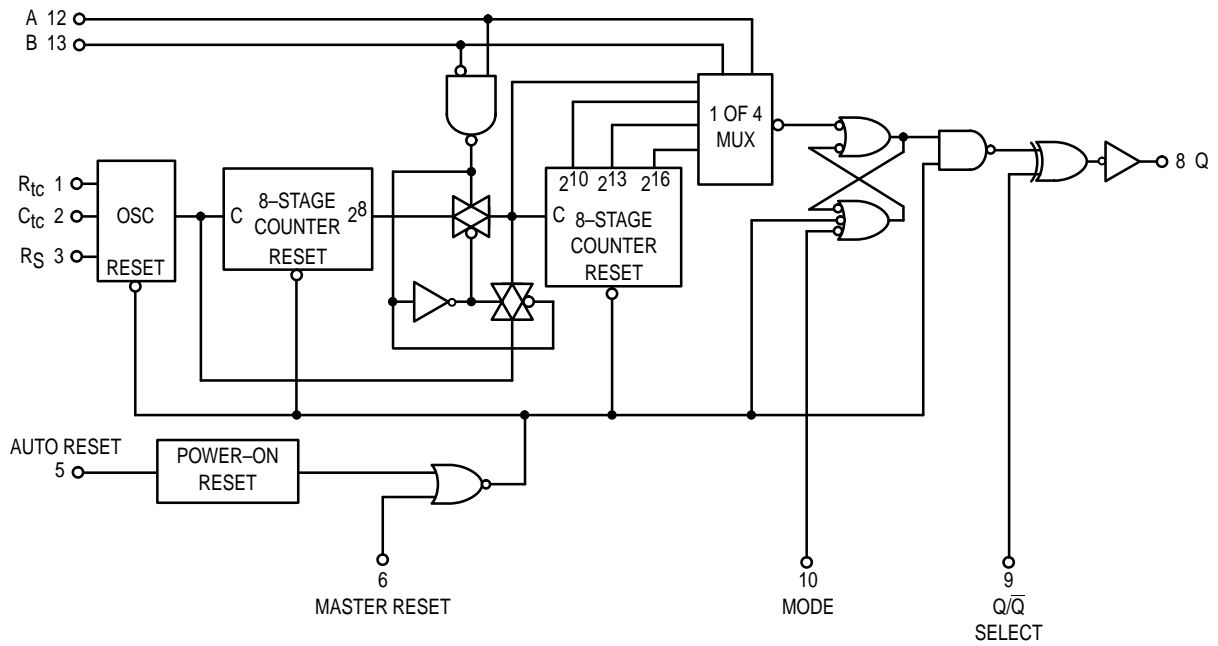


**Figure 1. Power Dissipation Test Circuit and Waveform**



**Figure 2. Switching Time Test Circuit and Waveforms**

### EXPANDED BLOCK DIAGRAM



V<sub>DD</sub> = PIN 14  
V<sub>SS</sub> = PIN 7

### FREQUENCY SELECTION TABLE

A	B	Number of Counter Stages n	Count 2 <sup>n</sup>
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

### TRUTH TABLE

Pin	State	
	0	1
Auto Reset, 5	Auto Reset Operating	Auto Reset Disabled
Master Reset, 6	Timer Operational	Master Reset On
Q/ $\bar{Q}$ , 9	Output Initially Low After Reset	Output Initially High After Reset
Mode, 10	Single Cycle Mode	Recycle Mode

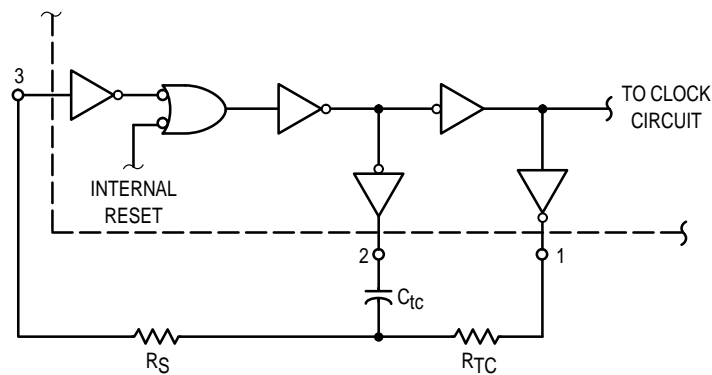


Figure 3. Oscillator Circuit Using RC Configuration

## TYPICAL RC OSCILLATOR CHARACTERISTICS

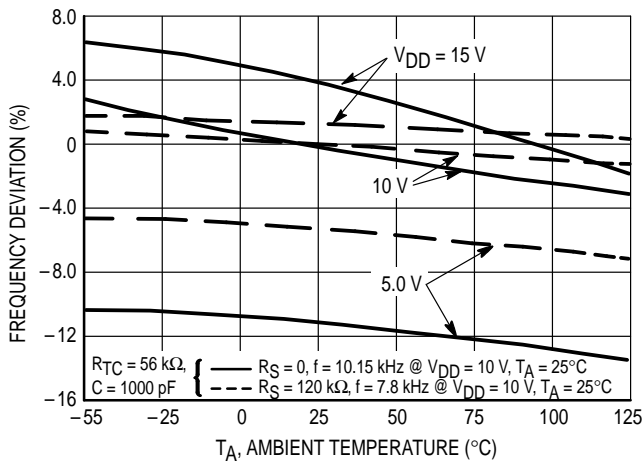


Figure 4. RC Oscillator Stability

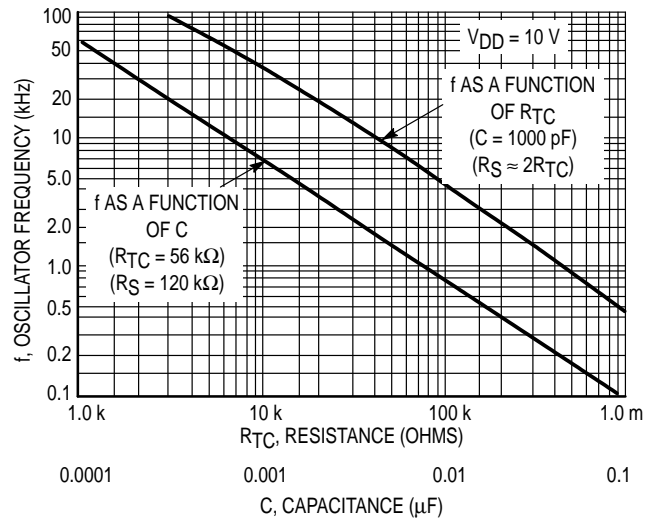


Figure 5. RC Oscillator Frequency as a Function of  $R_{tc}$  and  $C_{tc}$

## OPERATING CHARACTERISTICS

With Auto Reset pin set to a “0” the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a “1”. Both types of reset will result in synchronously resetting all counter stages independent of counter state. Auto Reset pin when set to a “1” provides a low power operation.

The RC oscillator as shown in Figure 3 will oscillate with a frequency determined by the external RC network i.e.,

$$f = \frac{1}{2.3 R_{tc} C_{tc}} \quad \text{if } (1 \text{ kHz} \leq f \leq 100 \text{ kHz})$$

and  $R_S \approx 2 R_{tc}$  where  $R_S \geq 10 \text{ k}\Omega$

A value of  $R_S$  required to sustain oscillation over a wide range of operating temperatures may need to be determined empirically. This may be done by finding a minimum to maximum resistor value range for oscillation at the two operating temperature extremes. Then, select a value well centered in the overlapping span of the combined ranges.

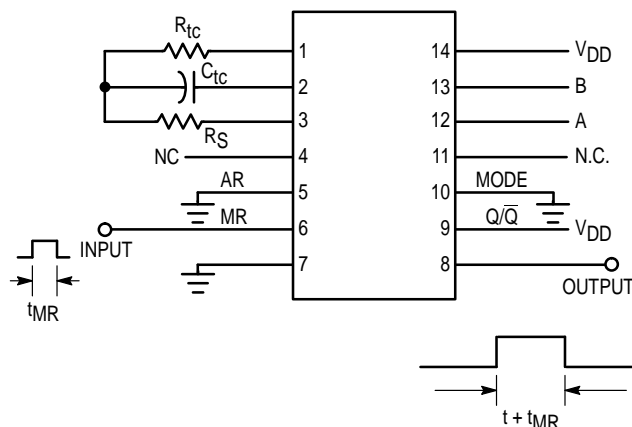
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages ( $2^8$ ,  $2^{10}$ ,  $2^{13}$  and

$2^{16}$ ). The  $2^n$  counts as shown in the Frequency Selection Table represents the Q output of the  $N^{\text{th}}$  stage of the counter. When A is “1”,  $2^{16}$  is selected for both states of B. However, when B is “0”, normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting  $2^8$ ).

The  $Q/\bar{Q}$  select output control pin provides for a choice of output level. When the counter is in a reset condition and  $Q/\bar{Q}$  select pin is set to a “0” the Q output is a “0”, correspondingly when  $Q/\bar{Q}$  select pin is set to a “1” the Q output is a “1”.

When the mode control pin is set to a “1”, the selected count is continually transmitted to the output. But, with mode pin “0” and after a reset condition the  $R_S$  flip-flop (see Expanded Block Diagram) resets, counting commences, and after  $2^n - 1$  counts the  $R_S$  flip-flop sets which causes the output to change state. Hence, after another  $2^n - 1$  counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

## DIGITAL TIMER APPLICATION



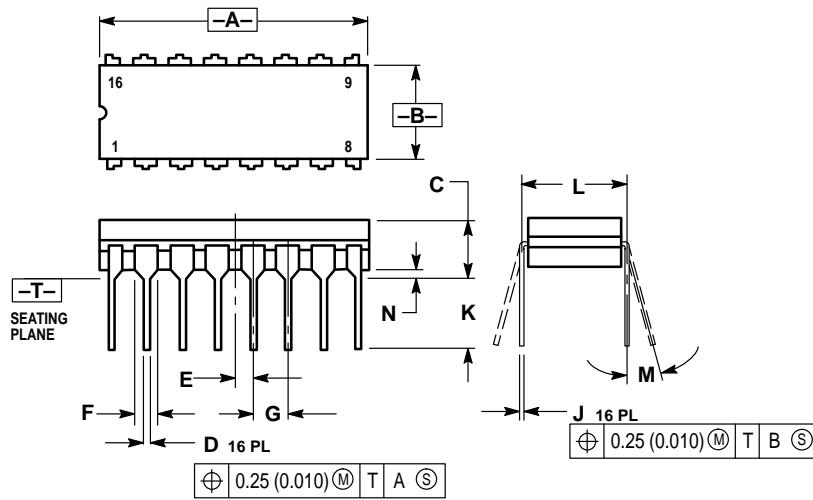
When Master Reset (MR) receives a positive pulse, the internal counters and latch are reset. The Q output goes high and remains high for one half the number ( $2^n - 1$ ) of clock pulses selected (via A and B), the Q output then goes low and remains low for the remaining half clock pulses or until another input pulse is received.

This “one shot” is fully retriggerable and as accurate as the input frequency. An external clock can be used (pin 3 is the clock input, pins 1 and 2 are outputs) if additional accuracy is needed.

Notice that a setup time equal to the desired pulse width output is required immediately following initial power up, during which time Q output will be high.

## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

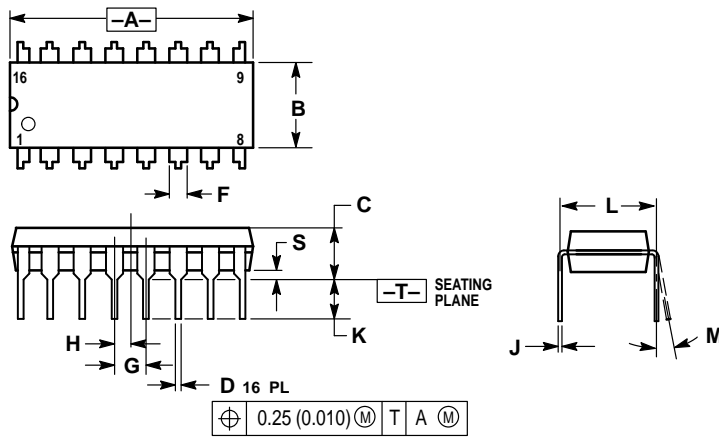


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



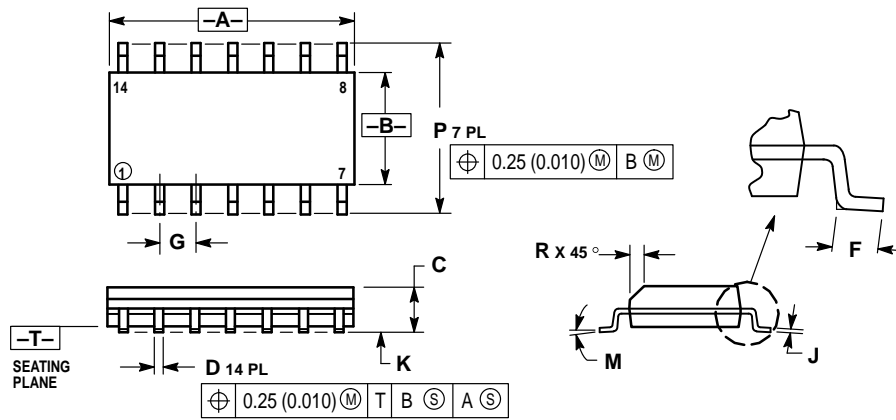
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

## OUTLINE DIMENSIONS


### D SUFFIX PLASTIC SOIC PACKAGE CASE 751A-03 ISSUE F



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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**MC14541B/D**