Integrated Circuit Systems, Inc.

ICS9250-37

Preliminary Product Preview

Frequency Generator for P4™

Recommended Application:
Intel Tehema Chipset

Output Features:

- 4 Differential CPU Clock Pairs @ 3.3V
- 2 - 3V MREF clocks for memory reference seeds, (separate single ended but 180 degrees out of phase)
- 4 - 66MHz reference output
- 10 - 3V 33MHz PCI clocks
- 2 - 48MHz clocks
- 2 - 14.318 reference output

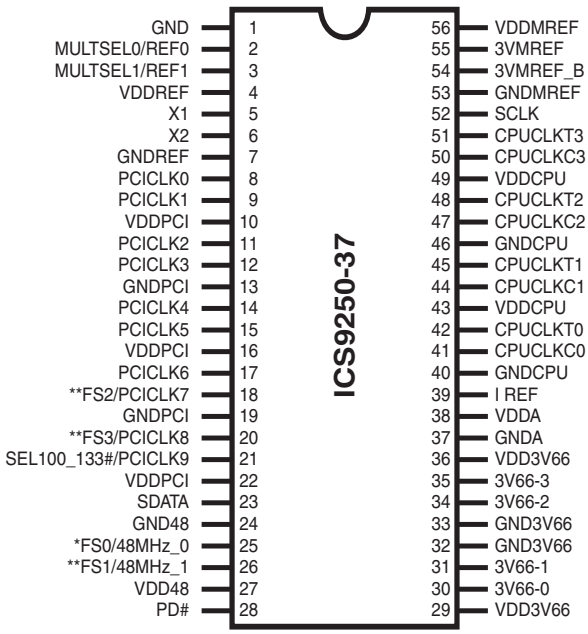
Features:

- Up to 156MHz frequency support
- Support power management: Power Down Mode
- Supports Spread Spectrum modulation: 0 to -0.5% down spread and ±0.25 center spread.
- Uses external 14.318MHz crystal
- Select logic for Differential Swing Control, Test mode, Tristate, Power down, Spread Spectrum, limited frequency select, selective clock enable.
- External resistor for current reference

Key Specifications:

- 3V66 Output jitter <300ps
- CPU Output Jitter <200ps
- MREF Output jitter <250ps

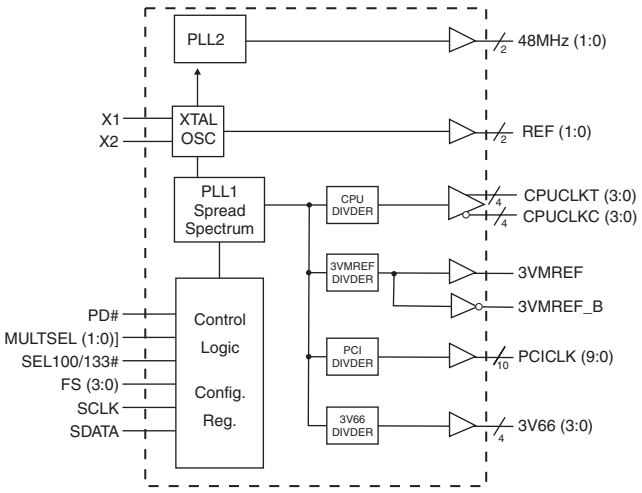
Pin Configuration



56-Pin 300mil SSOP

* This input has a 120K internal pull up to VDD.
** This input has a 120K internal pull down to GND.

Block Diagram



Frequency Table

SEL 133/100#	FS3	FS2	FS1	FS0	CPU	MRef	PCI	3V66
0	0	0	0	0	90.00	45.00	30.00	60.00
0	0	0	0	1	100.00	50.00	33.33	66.67
0	0	0	1	0	100.40	50.20	33.47	66.93
0	0	0	1	1	103.00	51.50	34.33	68.67
0	0	1	0	0	105.00	52.50	35.00	70.00
0	0	1	0	1	108.00	54.00	36.00	72.00
0	0	1	1	0	110.00	55.00	36.67	73.33
0	0	1	1	1	112.00	56.00	37.33	74.67
0	1	0	0	0	115.00	57.50	38.33	76.67
1	0	0	0	1	133.33	66.67	33.33	66.67
1	0	0	1	0	133.60	66.80	33.40	66.80
1	0	0	1	1	136.00	68.00	34.00	68.00
1	0	1	0	0	138.00	69.00	34.50	69.00
1	0	1	0	1	140.00	70.00	35.00	70.00
1	0	1	1	0	142.00	71.00	35.50	71.00
1	0	1	1	1	144.00	72.00	36.00	72.00

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General Description

The **ICS9250-37** is a single chip clock solution, for multi processor server or high-end desktop applications.

Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-37 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Power Groups

VDDREF, GNDREF= REF, X1, X2
VDDPCI, GNDPCI = PCICLK
VDD48, GND48 = 48MHz, Fixed PLL2
VDD3V66, GND3V66=3V66
VDDCPU, GNDCPU = CPUCLK
VDDMREF, GNDMREF=3VMREF, 3VMREF_B
VDDA=VDD (core supply voltage 3.3V)

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 7, 13, 19, 24, 32, 33, 37, 40, 46, 53	GND	PWR	Ground pins for 3.3V supply
3, 2	REF/MULTSEL (1:0)	IN	MULTSEL0 and MULTSEL1 inputs are sensed on power-up and then internally latched prior to the pin being used for output on 3V 14.318MHz clocks.
4, 10, 16, 22, 27, 29, 36, 38, 43, 49, 56	VDD	PWR	3.3V power supply
5	X1	X2 Crystal Input	14.318MHz Crystal input
6	X2	X1 Crystal Output	14.318MHz Crystal output
17, 15, 14, 12, 11, 9, 8	PCICLK (6:0)	OUT	PCI clock outputs
18	FS2[1,3]	IN	Margin testing frequency select pin
	PCICLK7	OUT	PCI clock output
20	FS3[1]	IN	Margin testing frequency select pin
	PCICLK8	OUT	PCI clock output
21	SEL100/133	IN	CPU Frequency Select. Low=100MHz, High=133MHz
	PCICLK9	OUT	PCI clock output
23	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
26, 25	FS1[1,3], FS0[1,2]	IN	Frequency select pins
	48MHz	OUT	48MHz clock output
28	PD#	IN	Invokes power-down mode. Active Low.
35, 24, 31, 30	3V66 (3:0)	OUT	66MHz reference clocks
39	I REF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin takes a fixed precision resistor tied to ground in order to establish the required current.
51, 48, 45, 42	CPUCLKT (3:0)	OUT	"True" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
50, 47, 44, 41	CPUCLKC (3:0)	OUT	"Complementory" clocks of differential pair CPU outputs. These are current outputs and external resistors are required for voltage bias.
52	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
54	3VMREF_B	OUT	3V reference to memory clock driver (out of phase with 3Vmref)
55	3VMREF	OUT	3V reference to memory clock driver

Notes:
1. To ensure proper Intel defined frequency is used, an external 10K ohm pull down resistor is recommended.
2. This input has 120K pull up.
3. This input has 120K pull down.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Byte 7	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 7***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
	Byte 7
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description										PWD
Bit 2, Bit 7:4	Bit2 SEL_133/100#	Bit7 FS3	Bit6 FS3	Bit5 FS1	Bit4 FS0	CPU	Mref	PCI	3V66	Spread Precentage	Note1 00000
	0	0	0	0	0	90.00	45.00	30.00	60.00	0 to 0.5% down spread	
	0	0	0	0	1	100.00	50.00	33.33	66.67	0 to 0.5% down spread	
	0	0	0	1	0	100.40	50.20	33.47	66.93	± 0.25% center spread	
	0	0	0	1	1	103.00	51.50	34.33	68.67	± 0.25% center spread	
	0	0	1	0	0	105.00	52.50	35.00	70.00	± 0.25% center spread	
	0	0	1	0	1	108.00	54.00	36.00	72.00	± 0.25% center spread	
	0	0	1	1	0	110.00	55.00	36.67	73.33	± 0.25% center spread	
	0	0	1	1	1	112.00	56.00	37.33	74.67	± 0.25% center spread	
	0	1	0	0	0	115.00	57.50	38.33	76.67	± 0.25% center spread	
	0	1	0	0	1	118.00	59.00	39.33	78.67	± 0.25% center spread	
	0	1	0	1	0	120.00	60.00	40.00	80.00	± 0.25% center spread	
	0	1	0	1	1	122.00	61.00	40.67	81.33	± 0.25% center spread	
	0	1	1	0	0	125.00	62.50	41.67	83.33	± 0.25% center spread	
	0	1	1	0	1	125.00	62.50	41.67	83.33	± 0.25% center spread	
	0	1	1	1	0	130.00	65.00	43.33	86.67	± 0.25% center spread	
	0	1	1	1	1	133.60	66.80	44.53	89.07	± 0.25% center spread	
	1	0	0	0	0	120.00	60.00	30.00	60.00	± 0.25% center spread	
	1	0	0	0	1	133.33	66.67	33.33	66.67	0 to 0.5% down spread	
	1	0	0	1	0	133.60	66.80	33.40	66.80	± 0.25% center spread	
	1	0	0	1	1	136.00	68.00	34.00	68.00	± 0.25% center spread	
	1	0	1	0	0	138.00	69.00	34.50	69.00	± 0.25% center spread	
	1	0	1	0	1	140.00	70.00	35.00	70.00	± 0.25% center spread	
	1	0	1	1	0	142.00	71.00	35.50	71.00	± 0.25% center spread	
	1	0	1	1	1	144.00	72.00	36.00	72.00	± 0.25% center spread	
	1	1	0	0	0	145.00	72.50	36.25	72.50	± 0.25% center spread	
	1	1	0	0	1	148.00	74.00	37.00	74.00	± 0.25% center spread	
	1	1	0	1	0	150.00	75.00	37.50	75.00	± 0.25% center spread	
	1	1	0	1	1	152.00	76.00	38.00	76.00	± 0.25% center spread	
	1	1	1	0	0	154.00	77.00	38.50	77.00	± 0.25% center spread	
	1	1	1	0	1	156.00	78.00	39.00	78.00	± 0.25% center spread	
	1	1	1	1	0	133.00	66.50	26.60	53.20	± 0.25% center spread	
	1	1	1	1	1	150.00	75.00	30.00	60.00	± 0.25% center spread	
Bit 3	0 - Frequency is selected by hardware select, Latched Input 1 - I^2C select										0
Bit 1	0 - Spread Spectrum Disable 1 - Spread Spectrum Enabled										0
Bit 0	0 - Running 1- Tristate all outputs										0

Note: PWD = Power-Up Default

Byte 1: CPU, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Readback FS0#
Bit 6	-	1	Readback FS1#
Bit 5	-	1	Readback FS2#
Bit 4	-	1	Readback (SEL133/100#)#
Bit 3	50,51	1	CPUC3/T3
Bit 2	47,48	1	CPUC2/T2
Bit 1	44/41	1	CPUC1/T1
Bit 0	41/42	1	CPUC0/T0

Byte 2: PCI, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	18	1	PCICLK7
Bit 6	17	1	PCICLK6
Bit 5	15	1	PCICLK5
Bit 4	14	1	PCICLK4
Bit 3	12	1	PCICLK3
Bit 2	11	1	PCICLK2
Bit 1	9	1	PCICLK1
Bit 0	8	1	PCICLK0

Byte 3: REF, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	21	1	PCICLK9
Bit 6	20	1	PCICLK8
Bit 5	54	1	3VMREF_B
Bit 4	55	1	3VMREF
Bit 3	3	1	REF1
Bit 2	2	1	REF0
Bit 1	26	1	48MHz_1
Bit 0	25	1	48MHz_0

Byte 4: 3V66, Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Readback FS3#
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	35	1	3V66_3
Bit 2	34	1	3V66_2
Bit 1	31	1	3V66_1
Bit 0	30	1	3V66_0

Byte 5: Reserved , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	1	Reserved

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 6: Peripheral , Active/Inactive Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: Don't write into this register, writing into this register can cause malfunction

CPUCLK Buffer Configuration

	Conditions	Configuration	Load	Min	Max
Iout	Vdd = nominal (3.30V)	All combinations of M0, M1 and Rr shown in table below	Nominal test load for given configuration	-7% I nominal	+7% I nominal
Iout	Vdd = 3.30 ± 5%	All combinations of M0, M1 and Rr shown in table below	Nominal test load for given configuration	-12% I nominal	+12% I nominal

CPUCLK Swing Select Functions

MULTSEL0	MULTSEL1	Board Target Trace/Term Z	Reference R, Iref= Vdd/(3*Rr)	Output Current	Voh @ Z, Iref=2.32mA
0	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.71V @ 60
0	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.59V @ 50
0	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.85V /2 60
0	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.71V @ 50
1	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.56V @ 60
1	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.47V @ 50
1	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.99V @ 60
1	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.82V @ 50
0	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.75V @ 30
0	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.62V @ 20
0	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.90V @ 30
0	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.75V @ 20
1	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.60 @ 20
1	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.5V @ 20
1	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	1.05V @ 30
1	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	0.84V @ 20

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V ±5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP}$	C_L = 0 pF; Select @ 66M			100	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND			600	µA
Input frequency	F_i	V_{DD} = 3.3 V;				MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{out}	Out put pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	mS
Settling Time[1]	T_s	From 1st crossing to 1% target Freq.			3	mS
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	mS
Delay	t_{PZH},t_{PZH}	output enable delay (all outputs)	1		10	nS
	t_{PLZ},t_{PZH}	output disable delay (all outputs)	1		10	nS

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C, V_{DD} = 3.3V R_S=33Ω, R_P (pulldown)=50Ω (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5		45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}[2]	$V_{OH@MIN}$= 1.0V , $V_{OH@MAX}$= 2.375V	-27		-27	mA
Output Low Current	I_{OL2B}[2]	$V_{OL@MIN}$= 1.2V , $V_{OL@MAX}$= 0.3V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 20% to 80%	175		700	ps
Fall Time	t_{f2B}[1]	V_{OH} = 80% to 20%	175		700	ps
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V Crossing Point	45		55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V Crossing Point			150	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V Crossing Point			200	ps

[1]Guarenteed by design, not 100% tested in production.

[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - REF, 48MHz

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-29		-23	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1		4	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1		4	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			N/A	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			1000	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - MREF/MREF_B

T_A = 0 - 70C; V_{DD} = 3.3 V ± 5%; C_L =10-30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			N/A	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			250	ps

[1]Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; V_{DD} = 3.3 V +/-5%; C_L =10-30 pF (unless otherwise stated)

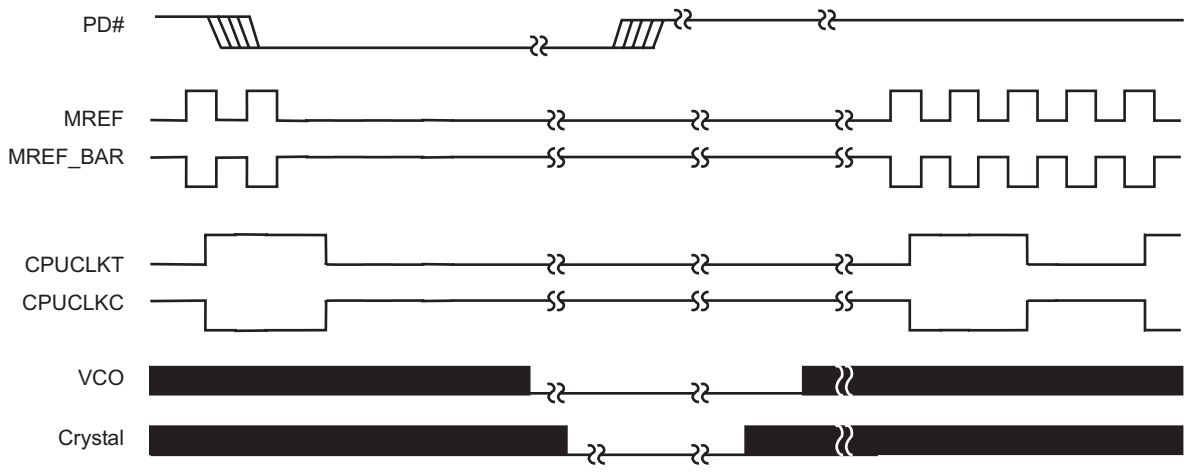
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH1}	VOH@ MIN = 1.0 V, VOH@ MAX = 3.135 V	-33		-33	mA
Output Low Current	I_{OL1}	VOL@ MIN = 1.95 V, VOL@ MAX= 0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			250	ps
Jitter	$t_{jcyc-cyc}$	V_T = 1.5 V			300	ps

[1]Guarenteed by design, not 100% tested in production.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below.



Notes:
1. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9250-37 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

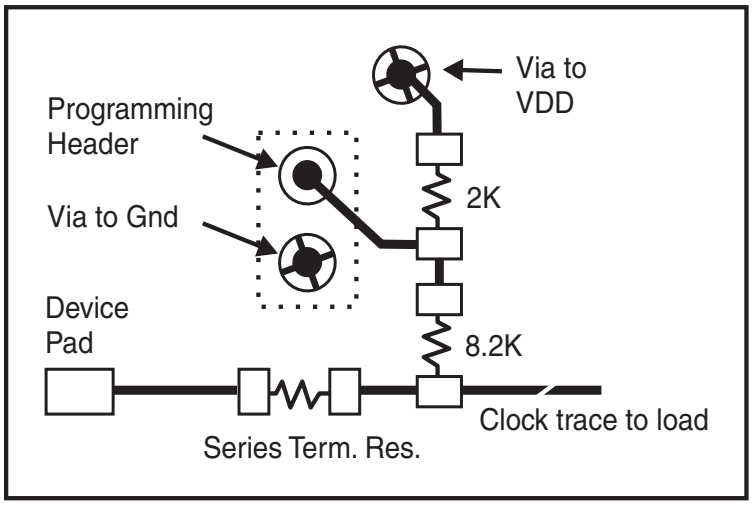
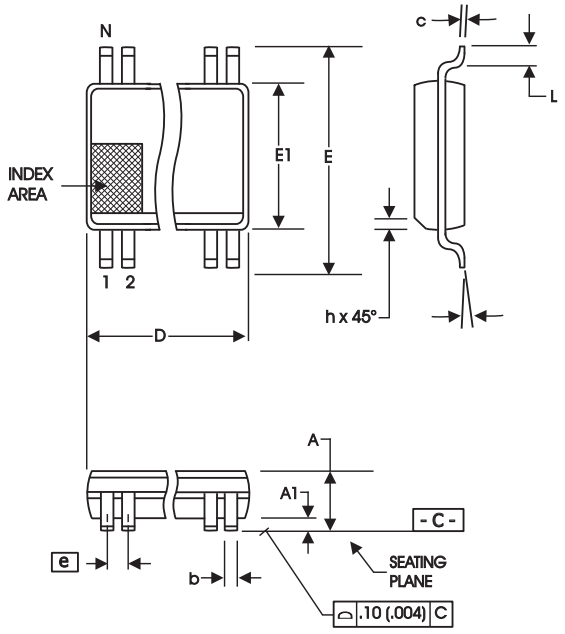


Fig. 1



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS9250yF-37-T

Example:

ICS XXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device