

# SIEMENS

## 4M × 72-Bit EDO-DRAM Module (ECC - Module)

**HYM 72V4005GS-50/-60**  
**HYM 72V4015GS-50/-60**

### 168 pin buffered DIMM Module

- 168 Pin JEDEC Standard, Buffered 8 Byte Dual In-Line Memory Module for PC main memory applications
- 1 bank 4M x 72 organisation
- Optimized for ECC applications
- Extended Data Out (EDO)
- Performance:

		-50	-60
tRAC	RAS Access Time	50 ns	60 ns
tCAC	CAS Access Time	18 ns	20 ns
tAA	Access Time from Address	30 ns	35 ns
tRC	Cycle Time	84 ns	104 ns
tHPC	EDO Mode Cycle Time	20 ns	25 ns

- Single + 3.3V (± 0.3V) supply
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh,  $\overline{\text{RAS}}$ -only-refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clock fully LVTTTL & LVCMOS compatible
- 4 Byte interleave enabled, Dual Address inputs (A0/B0)
- Buffered inputs excepts  $\overline{\text{RAS}}$  and DQ
- Parallel Presence detects
- Utilizes eighteen 4M × 4 -DRAMs and four BiCMOS buffers/line drivers
- Two versions : HYM 72V4005GS with TSOPII-components (4 mm thickness)  
HYM 72V4015GS with SOJ-components (9 mm thickness)
- 4096 refresh cycles / 64 ms with 12 / 10 addressing
- Gold contact pad
- Double sided module with 25.35 mm (1000 mil) height

The HYM 72V4005/15GS-50/-60 is a 32 MByte DRAM module organized as 4 194 430 words by 72-bit in a 168-pin, dual read-out, single-in-line package comprising eighteen HYB 3116405BT/BJ 4M × 4 DRAMs in 300 mil wide TSOPII or SOJ- packages mounted together with ceramic decoupling capacitors on a PC board. All inputs except  $\overline{\text{RAS}}$  and DQ are buffered by using four BiCMOS buffers/line drivers.

Each HYB 3116405BT/BJ is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

The density and speed of the module can be detected by the use of presence detect pins.

### Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 72V4005GS-50		L-DIM-168-5	3.3V 50ns EDO-DRAM module
HYM 72V4005GS-60		L-DIM-168-5	3.3V 60ns EDO-DRAM module
HYM 72V4015GS-50		L-DIM-168-5	3.3V 50ns EDO-DRAM module
HYM 72V4015GS-60		L-DIM-168-5	3.3V 60ns EDO-DRAM module

### Pin Names

A0-A11,B0	Address Input
DQ0 - DQ71	Data Input/Output
$\overline{\text{RAS}}_0$ , $\overline{\text{RAS}}_2$	Row Address Strobe
$\overline{\text{CAS}}_0$ , $\overline{\text{CAS}}_4$	Column Address Strobe
$\overline{\text{WE}}_0$ , $\overline{\text{WE}}_2$	Read / Write Input
$\overline{\text{OE}}_0$ , $\overline{\text{OE}}_2$	Output Enable
Vcc	Power (+3.3 Volt)
Vss	Ground
PD1 - PD8	Presence Detect Pins
$\overline{\text{PDE}}$	Presence Detect Enable
ID0 , ID1	ID identification bit
N.C.	No Connection

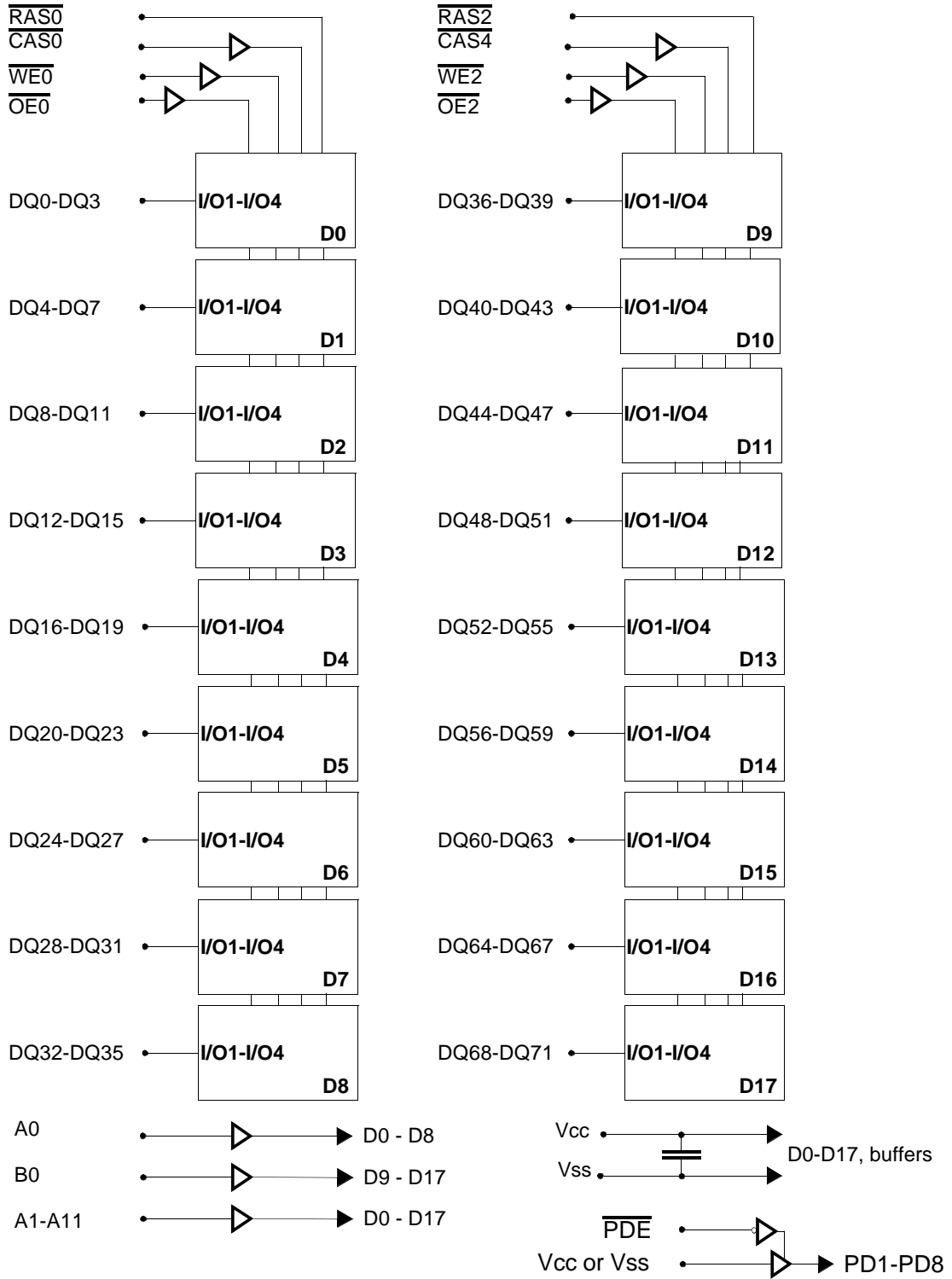
### Presence-Detect and ID-pin Truth Table:

Module	ID0	ID1	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8
HYM 72V4005/15GS-50	Vss	Vss	1	1	0	1	1	0	0	0
HYM 72V4005/15GS-60	Vss	Vss	1	1	0	1	1	1	1	0

**Note:** 1 = High Level ( Driver Output) , 0 = Low Level (Driver Output) for  $\overline{\text{PDE}}$  active ( ground) . For  $\overline{\text{PDE}}$  at a high level all PD terminal are in tri-state.

### Pin Configuration

PIN #	Symbol	PIN #	Symbol	PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	OE2	86	DQ36	128	NC
3	DQ1	45	RAS2	87	DQ37	129	NC
4	DQ2	46	CAS4	88	DQ38	130	NC
5	DQ3	47	NC	89	DQ39	131	NC
6	VCC	48	WE2	90	VCC	132	PDE
7	DQ4	49	VCC	91	DQ40	133	VCC
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	VCC	101	DQ49	143	VCC
18	VCC	60	DQ24	102	VCC	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	VSS	65	DQ25	107	VSS	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	VCC	68	VSS	110	VCC	152	VSS
27	WE0	69	DQ28	111	NC	153	DQ64
28	CAS0	70	DQ29	112	NC	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	RAS0	72	DQ31	114	NC	156	DQ67
31	OE0	73	VCC	115	NC	157	VCC
32	VSS	74	DQ32	116	VSS	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	VCC	82	PD7	124	VCC	166	PD8
41	NC	83	ID0 (VSS)	125	NC	167	ID1 (VSS)
42	NC	84	VCC	126	B0	168	VCC



### Block Diagram

### Absolute Maximum Ratings

Operating temperature range .....	0 to + 70 °C
Storage temperature range.....	- 55 to + 125 °C
Input/output voltage .....	-0.5 to min (V <sub>CC</sub> +0.5, 4.6) V
Power supply voltage.....	- 1 to + 4.6 V
Power dissipation.....	8.3 W
Data out current (short circuit) .....	50 mA

**Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics

$T_A = 0$  to  $70$  °C;  $V_{CC} = 3.3$  V  $\pm$  0.3V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	$V_{IH}$	2.0	$V_{CC}+0.5$	V	1)
Input low voltage	$V_{IL}$	- 1.0	0.8	V	1)
Output high voltage (LVTTTL) Output „H“ voltage level ( $I_{OUT} = - 2$ mA)	$V_{OH}$	2.4	-	V	1)
Output low voltage (LVTTTL) Output „L“ voltage level ( $I_{OUT} = 2$ mA)	$V_{OL}$	-	0.4	V	1)
Output high voltage (LVCMOS) Output „H“ voltage level ( $I_{OUT} = - 100$ $\mu$ A)	$V_{OH}$	$V_{CC}-0.2$	-	V	1)
Output low voltage (LVCMOS) Output „L“ voltage level ( $I_{OUT} = 100$ $\mu$ A)	$V_{OL}$	-	0.2	V	1)
Input leakage current ( $0$ V < $V_{IN} < V_{CC}$ , all other pins = $0$ V)	$I_{I(L)}$	- 20	20	$\mu$ A	1)
Output leakage current (DO is disabled, $0$ V < $V_{OUT} < V_{CC}$ )	$I_{O(L)}$	- 20	20	$\mu$ A	1)
Average $V_{CC}$ supply current:  -50 version -60 version	$I_{CC1}$	-	1800 1620	mA mA	2)3)4)
( $\overline{RAS}$ , $\overline{CAS}$ , address cycling, $t_{RC} = t_{RC}$ min.)					
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = 2.4$ V, one address change within 15,6 $\mu$ s trc).	$I_{CC2}$	-	50	mA	-

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average $V_{CC}$ supply current during $\overline{RAS}$ only refresh cycles: -50 version -60 version ( $\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ , $t_{RC} = t_{RC \text{ min.}}$ )	$I_{CC3}$	–	1800 1620	mA mA	2)4)
Average $V_{CC}$ supply current during hyper page mode (EDO): -50 version -60 version ( $\overline{RAS} = V_{IL}$ , $\overline{CAS}$ , address cycling $t_{PC} = t_{PC \text{ min.}}$ )	$I_{CC4}$	– – –	1260 990	mA mA	2)3)4)
Standby $V_{CC}$ supply current ( $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2 \text{ V}$ , one address change within 15,6 $\mu\text{s}$ trc)	$I_{CC5}$	–	30	mA	–
Average $V_{CC}$ supply current during $\overline{CAS}$ -before- $\overline{RAS}$ refresh mode: -50 version -60 version ( $\overline{RAS}$ , $\overline{CAS}$ cycling, $t_{RC} = t_{RC \text{ min.}}$ )	$I_{CC6}$	–	1800 1620	mA mA	2)4)

### Capacitance

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ;  $V_{CC} = 3.3 \text{ V} \pm 0.3\text{V}$ ;  $f = 1 \text{ MHz}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11, B0)	$C_{11}$	–	10	pF
Input capacitance ( $\overline{RAS0}$ , $\overline{RAS2}$ )	$C_{12}$	–	50	pF
Input capacitance ( $\overline{CAS0}$ , $\overline{CAS4}$ )	$C_{13}$	–	15	pF
Input capacitance ( $\overline{WE0}$ , $\overline{WE2}$ , $\overline{OE0}$ , $\overline{OE2}$ )	$C_{14}$	–	15	pF
I/O capacitance (DQ0-DQ71)	$C_{IO1}$	–	15	pF

### AC Characteristics (note: 5,6,7,8)

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ,  $V_{CC} = 3.3 \pm 0.3 \text{ V}$

Parameter	Symbol	-50		-60		Unit	Note
		min.	max.	min.	max.		

#### *common parameters*

Random read or write cycle time	$t_{RC}$	84	–	104	–	ns	
RAS precharge time	$t_{RP}$	30	–	40	–	ns	
RAS pulse width	$t_{RAS}$	50	100k	60	100k	ns	
$\overline{\text{CAS}}$ pulse width	$t_{CAS}$	8	10k	10	10k	ns	
Row address setup time	$t_{ASR}$	5	–	5	–	ns	9
Row address hold time	$t_{RAH}$	6	–	8	–	ns	10
Column address setup time	$t_{ASC}$	2	–	2	–	ns	11
Column address hold time	$t_{CAH}$	13	–	15	–	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	$t_{RCD}$	10	32	12	40		12
$\overline{\text{RAS}}$ to column address delay time	$t_{RAD}$	8	20	10	25	ns	12
$\overline{\text{RAS}}$ hold time	$t_{RSH}$	18	–	20	–	ns	9
$\overline{\text{CAS}}$ hold time	$t_{CSH}$	38	–	48	–	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	$t_{CRP}$	10	–	10	–	ns	9
Transition time (rise and fall)	$t_T$	1	30	1	30	ns	7
Refresh period	$t_{REF}$	–	64	–	64	ms	

#### *Read Cycle*

Access time from $\overline{\text{RAS}}$	$t_{RAC}$	–	50	–	60	ns	13,14
Access time from $\overline{\text{CAS}}$	$t_{CAC}$	–	18	–	20	ns	9,13,14
Access time from column address	$t_{AA}$	–	30	–	35	ns	9,13, 15
$\overline{\text{OE}}$ access time	$t_{OEA}$	–	18	–	20	ns	9,13
Column address to $\overline{\text{RAS}}$ lead time	$t_{RAL}$	30	–	35	–	ns	9
Read command setup time	$t_{RCS}$	2	–	2	–	ns	11
Read command hold time	$t_{RCH}$	2	–	2	–	ns	11,16
Read command hold time referenced to $\overline{\text{RAS}}$	$t_{RRH}$	0	–	0	–	ns	16
$\overline{\text{CAS}}$ to output in low-Z	$t_{CLZ}$	2	–	2	–	ns	11,13
Output buffer turn-off delay	$t_{OFF}$	–	18	–	20	ns	9,17

### AC Characteristics (cont'd) (note: 5,6,7,8)

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ,  $V_{CC} = 3.3 \pm 0.3 \text{ V}$

Parameter	Symbol	-50		-60		Unit	Note
		min.	max.	min.	max.		
Output buffer turn-off delay from $\overline{\text{OE}}$	$t_{\text{OEZ}}$	–	18	–	20	ns	9,17
$\overline{\text{CAS}}$ delay time from Din	$t_{\text{DZC}}$	0	–	0	–	ns	18
Data to $\overline{\text{OE}}$ low delay	$t_{\text{DZO}}$	0	–	0	–	ns	18
$\overline{\text{CAS}}$ high to data delay	$t_{\text{CDD}}$	15	–	18	–	ns	9,19
$\overline{\text{OE}}$ high to data delay	$t_{\text{ODD}}$	15	–	18	–	ns	9,19

### Write Cycle

Write command hold time	$t_{\text{WCH}}$	13	–	15	–	ns	9
Write command pulse width	$t_{\text{WP}}$	8	–	10	–	ns	
Write command setup time	$t_{\text{WCS}}$	2	–	2	–	ns	11,20
Write command to $\overline{\text{RAS}}$ lead time	$t_{\text{RWL}}$	18	–	20	–	ns	9
Write command to $\overline{\text{CAS}}$ lead time	$t_{\text{CWL}}$	13	–	15	–	ns	
Data setup time	$t_{\text{DS}}$	-2	–	-2	–	ns	10,21
Data hold time	$t_{\text{DH}}$	13	–	15	–	ns	9,21

### Read-Modify-Write Cycle

Read-write cycle time	$t_{\text{RWC}}$	118	–	143	–	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	$t_{\text{RWD}}$	66	–	77	–	ns	11,21
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	$t_{\text{CWD}}$	29	–	34	–	ns	11,21
Column address to $\overline{\text{WE}}$ delay time	$t_{\text{AWD}}$	41	–	49	–	ns	11,21
$\overline{\text{OE}}$ command hold time	$t_{\text{OEH}}$	8	–	11	–	ns	10

### Hyper Page Mode (EDO) Cycle

Hyper page mode cycle time	$t_{\text{PC}}$	20	–	25	–	ns	
$\overline{\text{CAS}}$ precharge time	$t_{\text{CP}}$	8	–	10	–	ns	
Access time from $\overline{\text{CAS}}$ precharge	$t_{\text{CPA}}$	–	32	–	37	ns	9,13
Output data hold time	$t_{\text{COH}}$	3	–	3	–	ns	10
$\overline{\text{RAS}}$ pulse width	$t_{\text{RAS}}$	50	200k	60	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay	$t_{\text{RHCP}}$	32	–	37	–	ns	9
$\overline{\text{OE}}$ setup time prior to $\overline{\text{CAS}}$	$t_{\text{OES}}$	5	–	5	–	ns	



### AC Characteristics (cont'd) (note: 5,6,7,8)

$T_A = 0$  to  $70$  °C,  $V_{CC} = 3.3 \pm 0.3$  V

Parameter	Symbol	-50		-60		Unit	Note
		min.	max.	min.	max.		

#### **Hyper Page Mode Read-Modify-Write Cycle**

Hyper page mode read-write cycle time	$t_{PRWC}$	60	–	70	–	ns	11
$\overline{CAS}$ precharge to $\overline{WE}$	$t_{CPWD}$	43	–	51	–	ns	11,21

#### **$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Cycle**

$\overline{CAS}$ setup time	$t_{CSR}$	12	–	12	–	ns	11
$\overline{CAS}$ hold time	$t_{CHR}$	8	–	8	–	ns	10
$\overline{RAS}$ to $\overline{CAS}$ precharge time	$t_{RPC}$	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	$t_{WRP}$	12	–	12	–	ns	11
Write hold time referenced to $\overline{RAS}$	$t_{WRH}$	8	–	8	–	ns	10

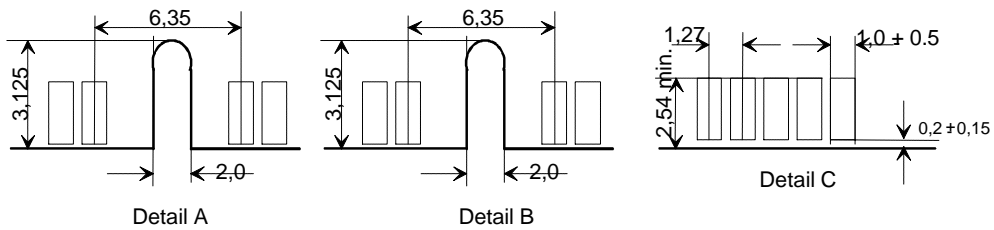
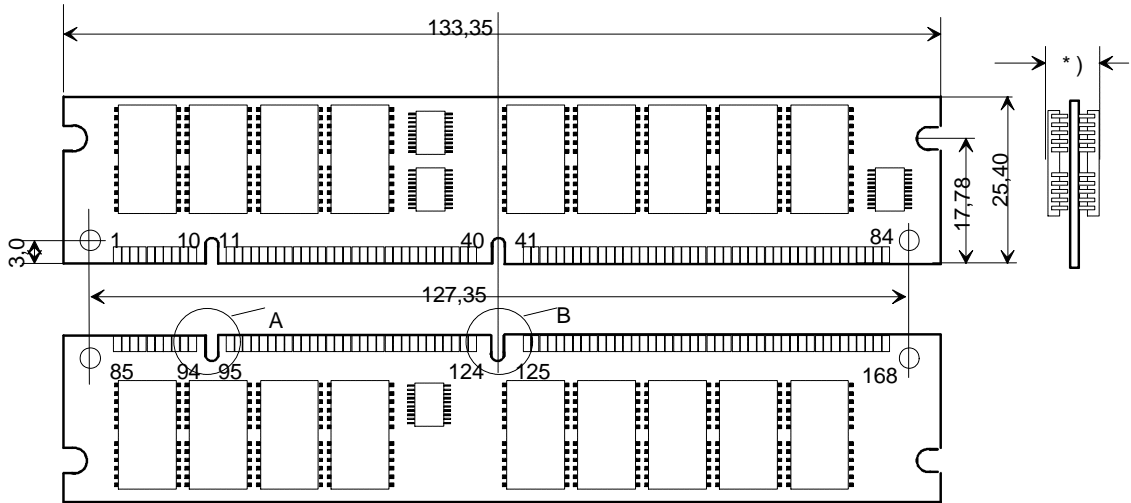
#### **Presence Detect Read Cycle**

$\overline{PDE}$ to valid presence detect data	$t_{PD}$	–	10	–	10	ns	
$\overline{PDE}$ inactive to presence detects inactive	$t_{PDOFF}$	0	10	0	10	ns	

**Notes:**

- 1) All voltages are referenced to VSS.
- 2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
- 3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.
- 4) Address can be changed once or less while  $\overline{RAS} = \text{Vil}$ . In the case of ICC4 it can be changed once or less during a hyper page mode (EDO) cycle ( thpc).
- 5) An initial pause of 100  $\mu\text{s}$  is required after power-up followed by 8 RAS-only-refresh cycles, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
- 6) AC measurements assume  $t_T = 2 \text{ ns}$ .
- 7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.
- 8) The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns ( $\overline{CAS}$ ,  $\overline{WE}$ ,  $\overline{OE}$ , addresses) maximum delay, no pulse shrinkage to the DRAM device timings. The data and RAS signals are not buffered, which preserves the DRAMs access specification of 50ns and 60ns.
- 9) A +5ns timing skew from the DRAM to the module resulted from the addition of line drivers.
- 10) A -2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
- 11) A +2ns timing skew from the DRAM to the module resulted from the addition of line drivers.
- 12) A -2ns (min.) and a -5ns (max.) timing skew from the DRAM to the module resulted from the addition of line drivers.
- 13) Measured with the specified current load and 100 pF at  $V_{oh} = 2.0 \text{ V}$  and  $V_{ol} = 0.8 \text{ V}$ . Access time is determined by the latter of tRAC, tCAC, tAA, tCPA, tOEA. tCAC is measured from tristate.
- 14) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.
- 15) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.
- 16) Either tRCH or tRRH must be satisfied for a read cycle.
- 17) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels. tOFF is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.
- 18) Either tDZC or tDZO must be satisfied.
- 19) Either tCDD or tODD must be satisfied.
- 20) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $tWCS > tWCS(\text{min.})$ , the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if  $tRWD > tRWD(\text{min.})$ ,  $tCWD > tCWD(\text{min.})$ ,  $tAWD > tAWD(\text{min.})$  and  $tCPWD > tCPWD(\text{min.})$ , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.
- 21) These parameters are referenced to  $\overline{CAS}$  leading edge in early write cycles and to  $\overline{WE}$  leading edge in Read-Modify-Write cycles.

**L-DIM-168-5  
Module package  
(dual read-out, single in-line memory module)**



4Mx72 3.3V  
DM168-5.WMF

preliminary drawing

\*) 9 mm thickness for modules assembled with SOJ-devices  
4mm thickness for modules assembled with TSOPII-devices