

# MACH445-12/15/20

Lattice Semiconductor

## High-Density EE CMOS Programmable Logic

### DISTINCTIVE CHARACTERISTICS

- 100-pin version of the MACH435 in PQFP
- 5 V, in-circuit programmable
- JTAG, IEEE 1149.1 JTAG testing capability
- 128 macrocells
- 12 ns  $t_{PD}$
- 83 MHz  $f_{CNT}$
- 70 inputs with pull-up resistors
- 64 outputs
- 192 flip-flops
  - 128 macrocell flip-flops
  - 64 input flip-flops
- Up to 20 product terms per function, with XOR
- Flexible clocking
  - Four global clock pins with selectable edges
  - Asynchronous mode available for each macrocell
- 8 "PAL33V16" blocks
- Input and output switch matrices for high routability
- Fixed, predictable, deterministic delays
- JEDEC-file compatible with MACH435
- Zero-hold-time input register option

### GENERAL DESCRIPTION

The MACH445 is a member of the high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide. It is architecturally identical to the MACH435, with the addition of JTAG and 5-V programming features.

The MACH445 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH445 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and

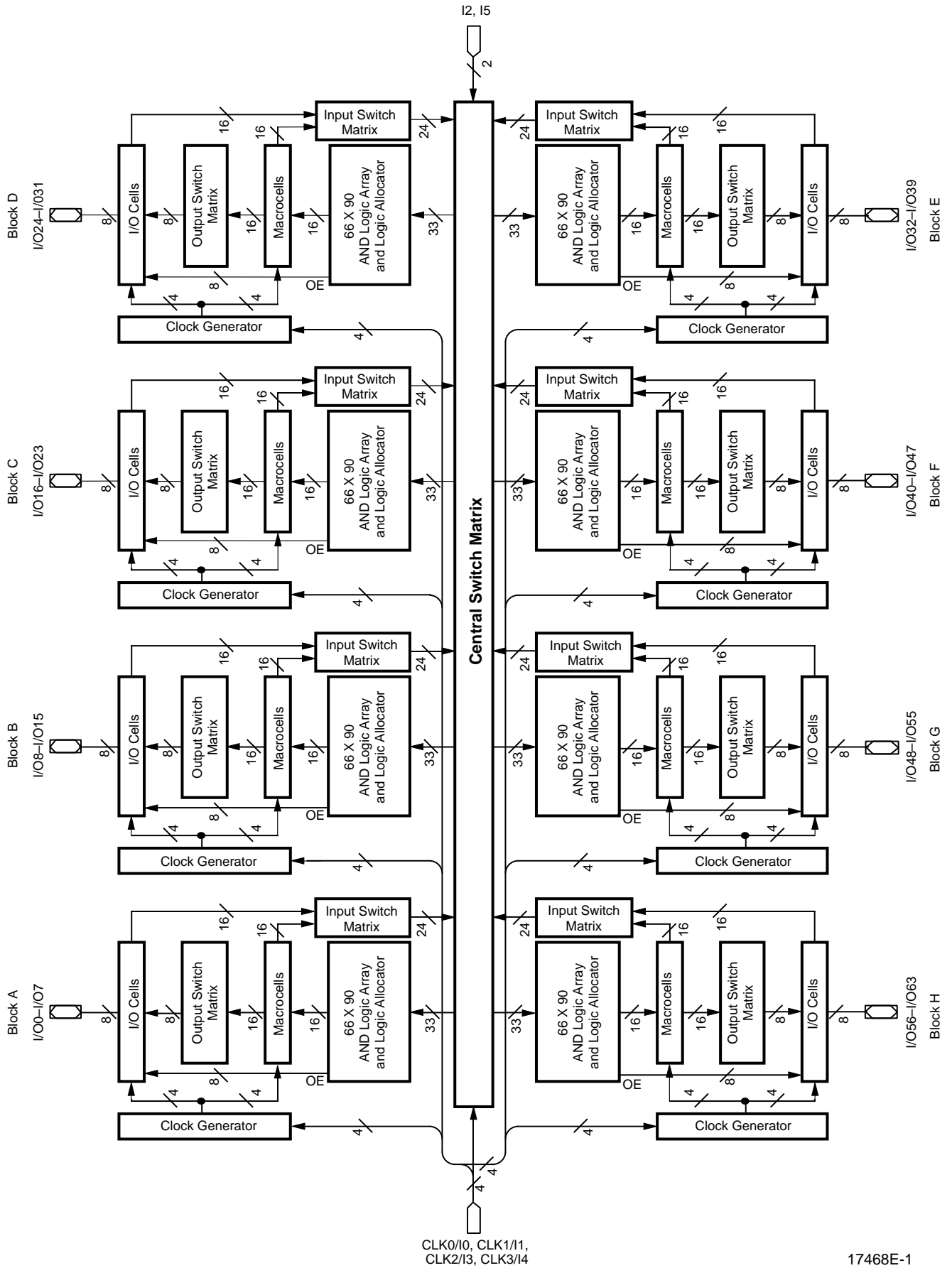
asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH445 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

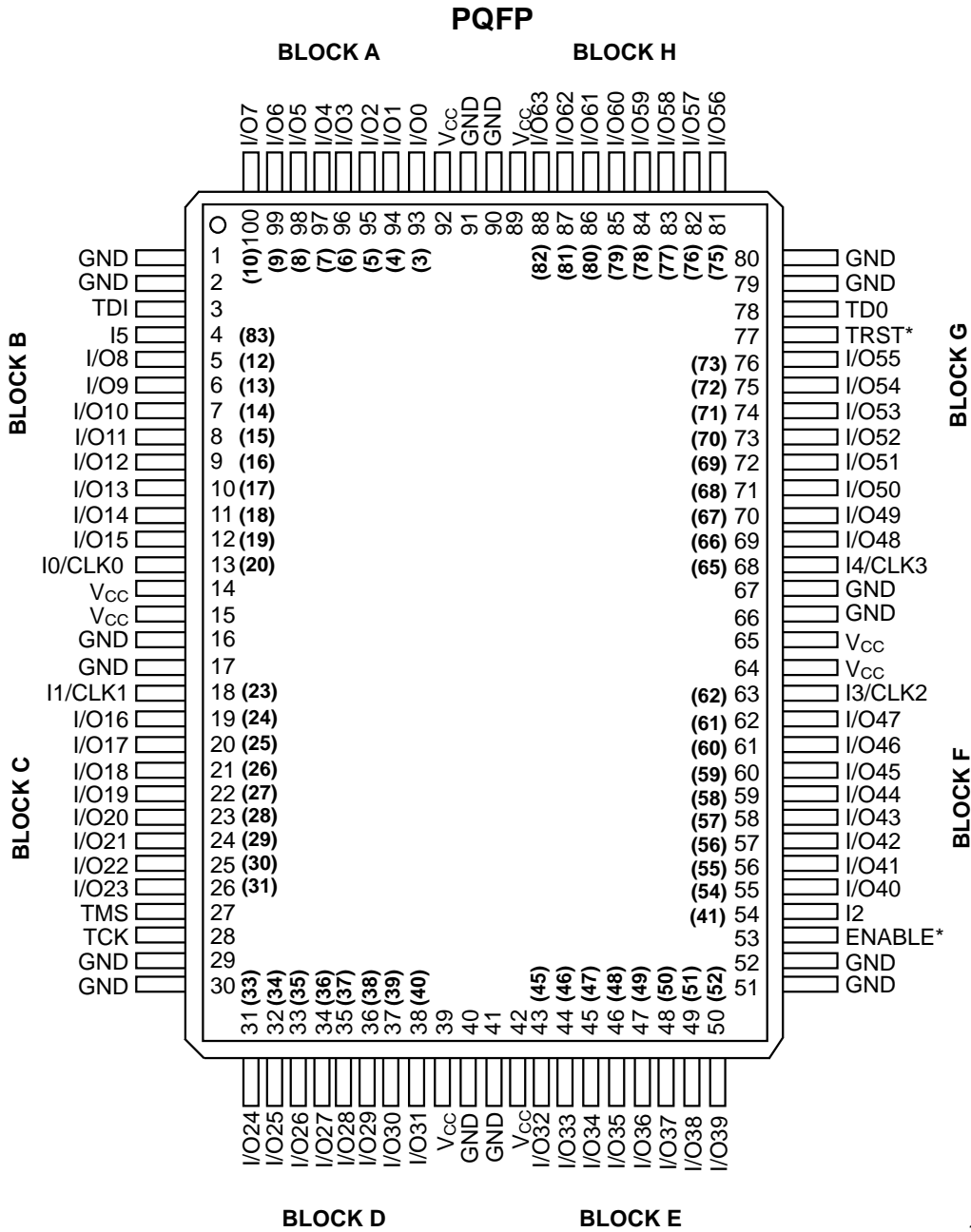
# BLOCK DIAGRAM



17468E-1

# CONNECTION DIAGRAM MACH445 (MACH435)

## Top View



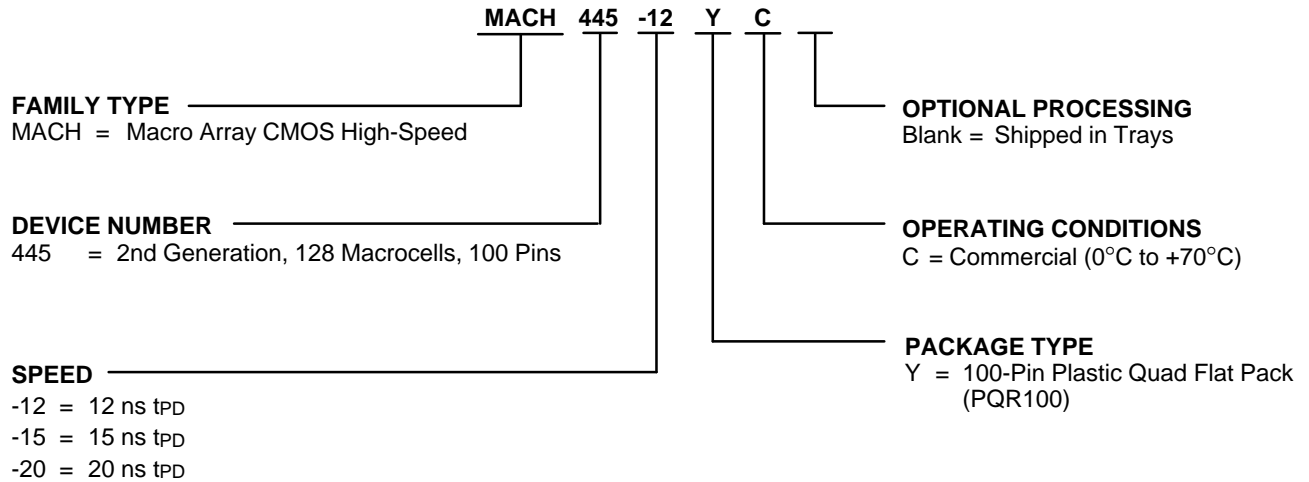
### PIN DESIGNATIONS

- CLK/I = Clock or Input
- GND = Ground
- I = Input
- I/O = Input/Output
- V<sub>cc</sub> = Supply Voltage

# ORDERING INFORMATION

## Commercial Products

Programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH445-12	YC
MACH445-15	
MACH445-20	

### Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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## FUNCTIONAL DESCRIPTION

The MACH445 consists of eight PAL blocks connected by a central switch matrix. There are 64 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

### The PAL Blocks

Each PAL block in the MACH445 (Figure 1) contains a clock generator, a 90-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 8 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent "PAL33V16" with 8 to 16 buried macrocells.

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product terms are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

### The Central Switch Matrix and Input Switch Matrix

The MACH445 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals, 8 registered input signals, and 8 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

### The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

### The Product-Term Array

The MACH445 product-term array consists of 80 product terms for logic use, eight product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

### The Logic Allocator

The logic allocator in the MACH445 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms in synchronous mode, or 18 product terms in asynchronous mode. When product terms are routed away from a macrocell, all 5 product terms may be redirected, which precludes the use of the macrocell for logic generation. It is possible to redirect only 4 product terms, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. Emulating all flip-flop types with a D-type flip-flop is also made possible. Register type emulation is automatically handled by the design software.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

**Table 9. Logic Allocation**

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

### The Macrocell and Output Switch Matrix

The MACH445 has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 2. Please refer to Figure 1 for macrocell and I/O pin numbers.

**Table 2. Output Switch Matrix Combinations**

Macrocell	Routeable to I/O Pins
M0, M1	I/O5, I/O6, I/O7, I/O0
M2, M3	I/O6, I/O7, I/O0, I/O1
M4, M5	I/O7, I/O0, I/O1, I/O2
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7
I/O Pin	Available Macrocells
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M10, M11, M12, M13, M14, M15, M0, M1
I/O6	M12, M13, M14, M15, M0, M1, M2, M3
I/O7	M14, M15, M0, M1, M2, M3, M4, M5

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

### The I/O Cell

The I/O cell in the MACH445 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The input flip-flop can be configured as a register or latch. Both the direct I/O signal and the registered/latched signal are available to the input switch matrix, and can be used simultaneously if desired.

### JTAG Testing

JTAG is the commonly used acronym for the IEEE Standard 1149.1–1990. The JTAG standard defines input and output pins, logic control functions, and instructions. Lattice/Vantis has incorporated this standard into the MACH445 device.

The JTAG standard was developed as a means of providing both board-level and device-level testing.

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## Five-Volt Programming

Another benefit from the JTAG circuitry that we have derived is the ability to use the JTAG port for five-volt programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate Plastic Quad Flat Pack, or PQFP, leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially which is ideal for on-board programming since it only requires the use of the Test Access Port. Use of the programming Enable Pin (ENABLE\*) is optional.

## Zero-Hold-Time Input Register

The MACH445 device has a zero-hold time (ZHT) fuse. This fuse controls the time delay associated with loading data into all I/O cell registers and latches in the MACH445 device.

When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized and the device timing is compatible with the MACH435 device.

This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

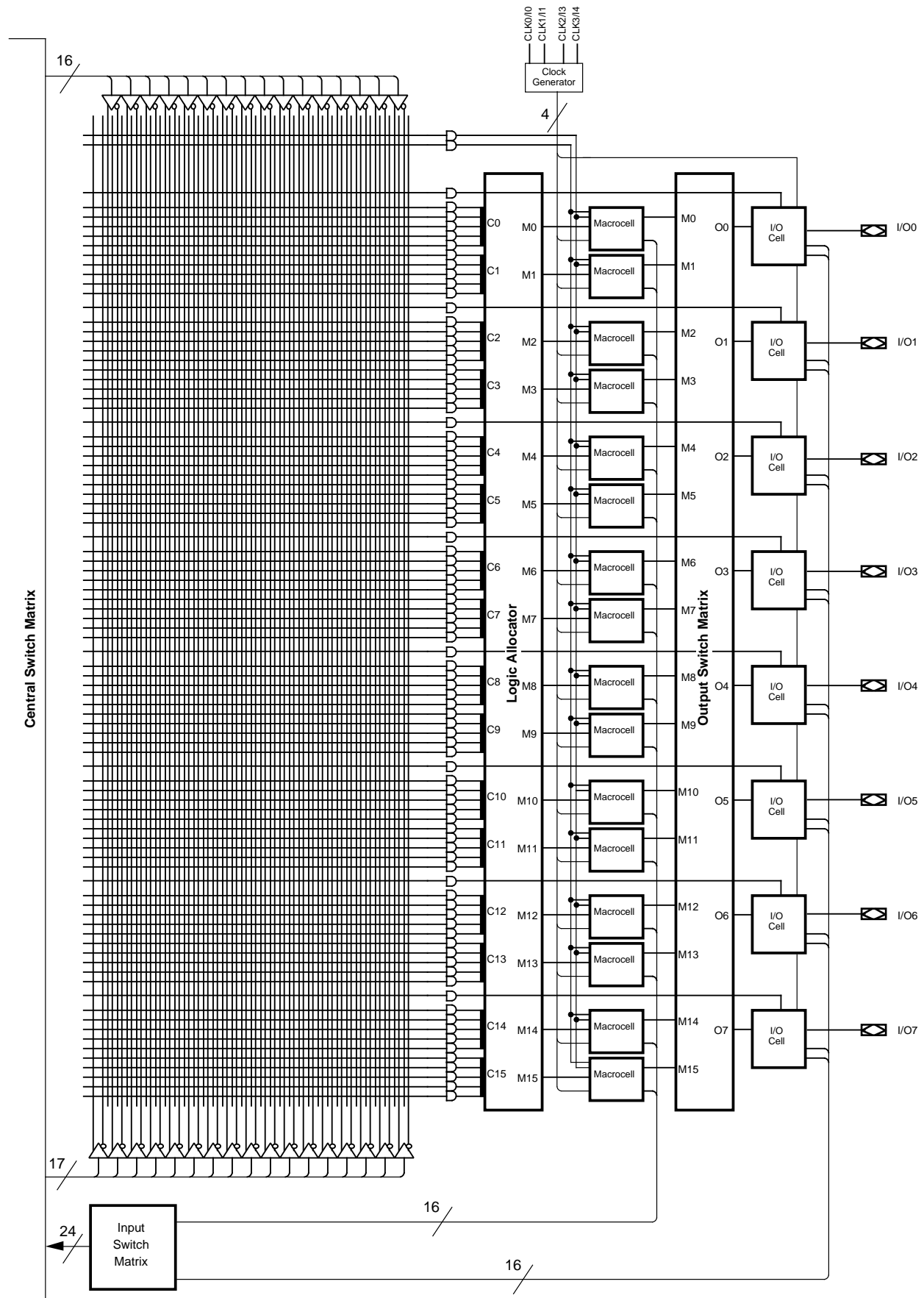


Figure 1. MACH445 PAL Block

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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	−0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ )	200 mA

## OPERATING RANGES

### Commercial (C) Devices

Temperature ( $T_A$ ) Operating in Free Air	0°C to +70°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 1)			0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)			10	$\mu\text{A}$
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)			−100	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)			10	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)			−100	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)	−30		−160	mA
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA) $V_{CC} = 5.0$ V, $f = 25$ MHz, $T_A = 25^\circ\text{C}$ (Note 5)		255		mA

## CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions	Typ	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 2.0$ V	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 2.0$ V		
		$V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$ , $f = 1$ MHz	8	pF

### Notes:

1. Total  $I_{OL}$  for one PAL block should not exceed 128 mA.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.
5. Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description		-12		Unit
			Min	Max	
t <sub>PD</sub>	Input, I/O, or Feedback to Combinatorial Output		3	12	ns
t <sub>SA</sub>	Setup Time from Input, I/O, or Feedback to Product Term Clock	D-type	5		ns
		T-type	6		ns
t <sub>HA</sub>	Register Data Hold Time Using Product Term Clock		5		ns
t <sub>COA</sub>	Product Term Clock to Output		4	14	ns
t <sub>WLA</sub>	Product Term, Clock Width	LOW	8		ns
t <sub>WHA</sub>		HIGH	8		ns
f <sub>MAXA</sub>	Maximum Frequency Using Product Term Clock (Note 2)	External Feedback	D-type	52.6	MHz
			T-type	50.0	MHz
		Internal Feedback (f <sub>CNTA</sub> )	D-type	58.8	MHz
			T-type	55.6	MHz
No Feedback (Note 3)			62.5	MHz	
t <sub>SS</sub>	Setup Time from Input, I/O, or Feedback to Global Clock	D-type	7		ns
		T-type	8		ns
t <sub>HS</sub>	Register Data Hold Time Using Global Clock		0		ns
t <sub>COS</sub>	Global Clock to Output		2	8	ns
t <sub>WLS</sub>	Global Clock Width	LOW	6		ns
t <sub>WHS</sub>		HIGH	6		ns
f <sub>MAXS</sub>	Maximum Frequency Using Global Clock (Note 2)	External Feedback	D-type	66.7	MHz
			T-type	62.5	MHz
		Internal Feedback (f <sub>CNTS</sub> )	D-type	83.3	MHz
			T-type	76.9	MHz
No Feedback (Note 3)			83.3	MHz	
t <sub>SLA</sub>	Setup Time from Input, I/O, or Feedback to Product Term Clock		5		ns
t <sub>HLA</sub>	Latch Data Hold Time Using Product Term Clock		5		ns
t <sub>GOA</sub>	Product Term Gate to Output			16	ns
t <sub>GWA</sub>	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		6		ns
t <sub>SLS</sub>	Setup Time from Input, I/O, or Feedback to Global Gate		8		ns
t <sub>HLS</sub>	Latch Data Hold Time Using Global Gate		0		ns
t <sub>GOS</sub>	Gate to Output			10	ns
t <sub>GWS</sub>	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		6		ns
t <sub>ICO</sub>	Input Register Clock to Combinatorial Output			18	ns

**SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)  
(continued)**

Parameter Symbol	Parameter Description	-12		Unit	
		Min	Max		
t <sub>ICS</sub>	Input Register Clock to Output Register Setup	D-type	9	ns	
		T-type	10	ns	
t <sub>WICL</sub>	Input Register Clock Width	LOW	6	ns	
t <sub>WICH</sub>		HIGH	6	ns	
f <sub>MAXIR</sub>	Maximum Input Register Frequency	1/(t <sub>WICL</sub> + t <sub>WICH</sub> )		83.3	MHz
t <sub>IGO</sub>	Input Latch Gate to Combinatorial Output		16	ns	
t <sub>IGOL</sub>	Input Latch Gate to Output Through Transparent Output Latch		18	ns	
t <sub>IGSA</sub>	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate	4		ns	
t <sub>IGSS</sub>	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate	9		ns	
t <sub>WIGL</sub>	Input Latch Gate Width LOW	6		ns	
t <sub>AR</sub>	Asynchronous Reset to Registered or Latched Output		16	ns	
t <sub>ARW</sub>	Asynchronous Reset Width (Note 2)	12		ns	
t <sub>ARR</sub>	Asynchronous Reset Recovery Time (Note 2)	10		ns	
t <sub>AP</sub>	Asynchronous Preset to Registered or Latched Output		16	ns	
t <sub>APW</sub>	Asynchronous Preset Width (Note 2)	12		ns	
t <sub>APR</sub>	Asynchronous Preset Recovery Time (Note 2)	8		ns	
t <sub>EA</sub>	Input, I/O, or Feedback to Output Enable	2	12	ns	
t <sub>ER</sub>	Input, I/O, or Feedback to Output Disable	2	12	ns	
<b>Input Register with Standard-Hold-Time Option</b>					
t <sub>PDL</sub>	Input, I/O, or Feedback to Output Through Transparent Input Latch		14	ns	
t <sub>SIR</sub>	Input Register Setup Time	2		ns	
t <sub>HIR</sub>	Input Register Hold Time	3		ns	
t <sub>SIL</sub>	Input Latch Setup Time	2		ns	
t <sub>HIL</sub>	Input Latch Hold Time	3		ns	
t <sub>SLLA</sub>	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	4		ns	
t <sub>SLLS</sub>	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	9		ns	
t <sub>PDLL</sub>	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		16	ns	

**SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)  
(continued)**

Parameter Symbol	Parameter Description	-12		Unit
		Min	Max	
<b>Input Register with Zero-Hold-Time Option</b>				
$t_{PDL}^1$	Input, I/O, or Feedback to Output Through Transparent Input Latch		20	ns
$t_{SIR}^1$	Input Register Setup Time	6		ns
$t_{HIR}^1$	Input Register Hold Time	0		ns
$t_{SIL}^1$	Input Latch Setup Time	6		ns
$t_{HIL}^1$	Input Latch Hold Time	0		ns
$t_{SLLA}^1$	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	16		ns
$t_{SLLS}^1$	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	18		ns
$t_{PDLL}^1$	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		22	ns

**Notes:**

1. See Switching Test Circuit at the end of this Data Book for test conditions.
2. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
3. This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	−0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	−0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ )	200 mA

## OPERATING RANGES

### Commercial (C) Devices

Temperature ( $T_A$ ) Operating in Free Air	0°C to +70°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 1)			0.5	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)			10	$\mu\text{A}$
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)			−100	$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)			10	$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 3)			−100	$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)		−30	−160	mA
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA), $V_{CC} = 5.0$ V, $f = 25$ MHz $T_A = 25^\circ\text{C}$ (Note 5)		255		mA

## CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions	Typ	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 2.0$ V	6	$\mu\text{F}$
$C_{OUT}$	Output Capacitance	$V_{OUT} = 2.0$ V		
		$V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$ , $f = 1$ MHz	8	$\mu\text{F}$

### Notes:

1. Total  $I_{OL}$  for one PAL block should not exceed 128 mA.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.
5. Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset. An actual  $I_{CC}$  value can be calculated by using the "Typical Dynamic  $I_{CC}$  Characteristics" Chart towards the end of this data sheet.
6. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description		-15		-20		Unit	
			Min	Max	Min	Max		
t <sub>PD</sub>	Input, I/O, or Feedback to Combinatorial Output (Note 2)		3	15	3	20	ns	
t <sub>SA</sub>		Setup Time from Input, I/O, or Feedback to Product Term Clock	D-type	8		10	ns	
			T-type	9		11	ns	
t <sub>HA</sub>	Register Data Hold Time Using Product Term Clock		8		10		ns	
t <sub>COA</sub>	Product Term Clock to Output (Note 2)		4	18	4	22	ns	
t <sub>WLA</sub>	Product Term, Clock Width		LOW	9		12	ns	
t <sub>WHA</sub>			HIGH	9		12	ns	
f <sub>MAXA</sub>	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	1/(t <sub>SA</sub> + t <sub>COA</sub> )	D-type	38.5		31.2	MHz
			T-type	37		30.3	MHz	
		Internal Feedback (f <sub>CNTA</sub> )	D-type	47.6		37	MHz	
			T-type	45.4		35.7	MHz	
No Feedback (Note 4)	1/(t <sub>WLA</sub> + t <sub>WHA</sub> )	55.6		41.7	MHz			
t <sub>SS</sub>		Setup Time from Input, I/O, or Feedback to Global Clock	D-type	10		13	ns	
			T-type	11		14	ns	
t <sub>HS</sub>	Register Data Hold Time Using Global Clock		0		0		ns	
t <sub>COS</sub>	Global Clock to Output (Note 2)		2	10	2	12	ns	
t <sub>WLS</sub>	Global Clock Width		LOW	6		8	ns	
t <sub>WHS</sub>			HIGH	6		8	ns	
f <sub>MAXS</sub>	Maximum Frequency Using Global Clock (Note 3)	External Feedback	1/(t <sub>SS</sub> + t <sub>COS</sub> )	D-type	50		40	MHz
			T-type	47.6		38.5	MHz	
		Internal Feedback (f <sub>CNTS</sub> )	D-type	66.6		50	MHz	
			T-type	62.5		47.6	MHz	
No Feedback (Note 4)	1/(t <sub>WLS</sub> + t <sub>WHS</sub> )	83.3		62.5	MHz			
t <sub>SLA</sub>	Setup Time from Input, I/O, or Feedback to Product Term Clock		8		10		ns	
t <sub>HLA</sub>	Latch Data Hold Time Using Product Term Clock		8		10		ns	
t <sub>GOA</sub>	Product Term Gate to Output (Note 2)			19		22	ns	
t <sub>GWA</sub>	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		9		12		ns	
t <sub>SLS</sub>	Setup Time from Input, I/O, or Feedback to Global Gate		10		13		ns	
t <sub>HLS</sub>	Latch Data Hold Time Using Global Gate		0		0		ns	
t <sub>GOS</sub>	Gate to Output (Note 2)			11		12	ns	
t <sub>GWS</sub>	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)		6		8		ns	
t <sub>ICO</sub>	Input Register Clock to Combinatorial Output			20		25	ns	

**SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)  
(continued)**

Parameter Symbol	Parameter Description		-15		-20		Unit
			Min	Max	Min	Max	
t <sub>ICS</sub>	Input Register Clock to Output Register Setup		D-type	15		20	ns
			T-type	16		21	ns
t <sub>WICL</sub>	Input Register Clock Width		LOW	6		8	ns
t <sub>WICH</sub>			HIGH	6		8	ns
f <sub>MAXIR</sub>	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		62.5		MHz
t <sub>IGO</sub>	Input Latch Gate to Combinatorial Output			20		25	ns
t <sub>IGOL</sub>	Input Latch Gate to Output Through Transparent Output Latch			22		27	ns
t <sub>IGSA</sub>	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		14		19		ns
t <sub>IGSS</sub>	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		21		ns
t <sub>WIGL</sub>	Input Latch Gate Width LOW		6		8		ns
t <sub>AR</sub>	Asynchronous Reset to Registered or Latched Output			20		25	ns
t <sub>ARW</sub>	Asynchronous Reset Width (Note 3)		15		20		ns
t <sub>ARR</sub>	Asynchronous Reset Recovery Time (Note 3)		15		20		ns
t <sub>AP</sub>	Asynchronous Preset to Registered or Latched Output			20		25	ns
t <sub>APW</sub>	Asynchronous Preset Width (Note 3)		15		20		ns
t <sub>APR</sub>	Asynchronous Preset Recovery Time (Note 3)		15		20		ns
t <sub>EA</sub>	Input, I/O, or Feedback to Output Enable (Note 2)		2	15	2	20	ns
t <sub>ER</sub>	Input, I/O, or Feedback to Output Disable (Note 2)		2	15	2	20	ns
<b>Input Register with Standard-Hold-Time Option</b>							
t <sub>PDL</sub>	Input, I/O, or Feedback to Output Through Transparent Input Latch			17		22	ns
t <sub>SIR</sub>	Input Register Setup Time		2		2		ns
t <sub>HIR</sub>	Input Register Hold Time		4		5		ns
t <sub>SIL</sub>	Input Latch Setup Time		2		2		ns
t <sub>HIL</sub>	Input Latch Hold Time		4		5		ns
t <sub>SLLA</sub>	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate		10		12		ns
t <sub>SLLS</sub>	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate		12		16		ns
t <sub>PDLL</sub>	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19		24	ns

**SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)  
(continued)**

Parameter Symbol	Parameter Description	-15		-20		Unit
		Min	Max	Min	Max	
<b>Input Register with Zero-Hold-Time Option</b>						
t <sub>PDL</sub> <sup>1</sup>	Input, I/O, or Feedback to Output Through Transparent Input Latch		23		30	ns
t <sub>SIR</sub> <sup>1</sup>	Input Register Setup Time	6		8		ns
t <sub>HIR</sub> <sup>1</sup>	Input Register Hold Time	0		0		ns
t <sub>SIL</sub> <sup>1</sup>	Input Latch Setup Time	6		8		ns
t <sub>HIL</sub> <sup>1</sup>	Input Latch Hold Time	0		0		ns
t <sub>SLLA</sub> <sup>1</sup>	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	16		20		ns
t <sub>SLLS</sub> <sup>1</sup>	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	18		24		ns
t <sub>PDLL</sub> <sup>1</sup>	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		25		32	ns

**Notes:**

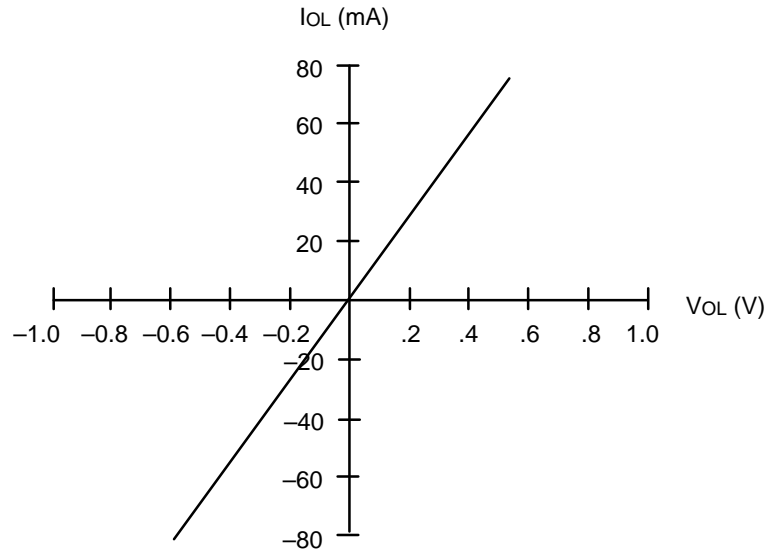
1. See Switching Test Circuit at the end of this Data Book for test conditions.
2. Parameters measured with 32 outputs switching.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
4. This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.



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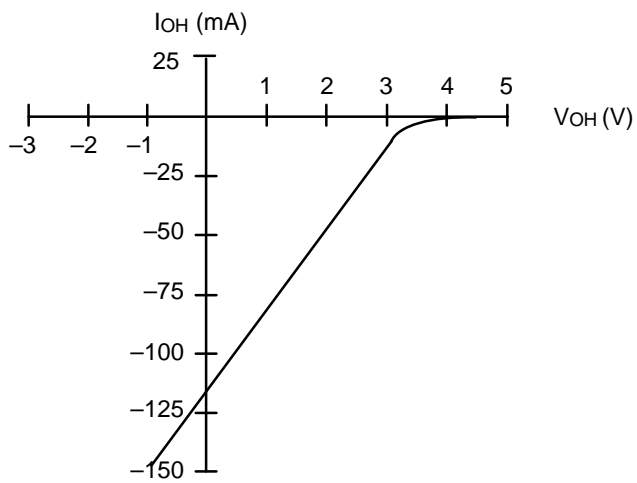
## TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

$V_{CC} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$



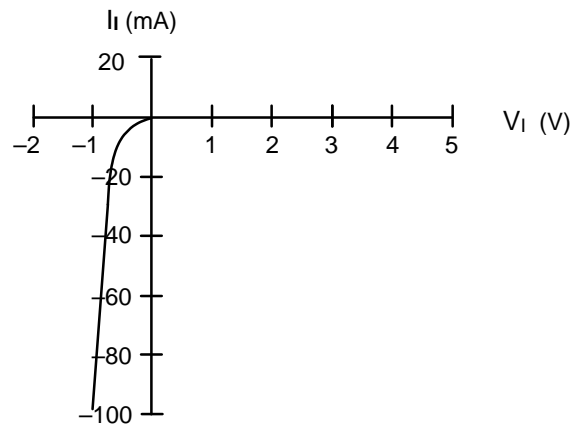
**Output, LOW**

17468E-4



**Output, HIGH**

17468E-5



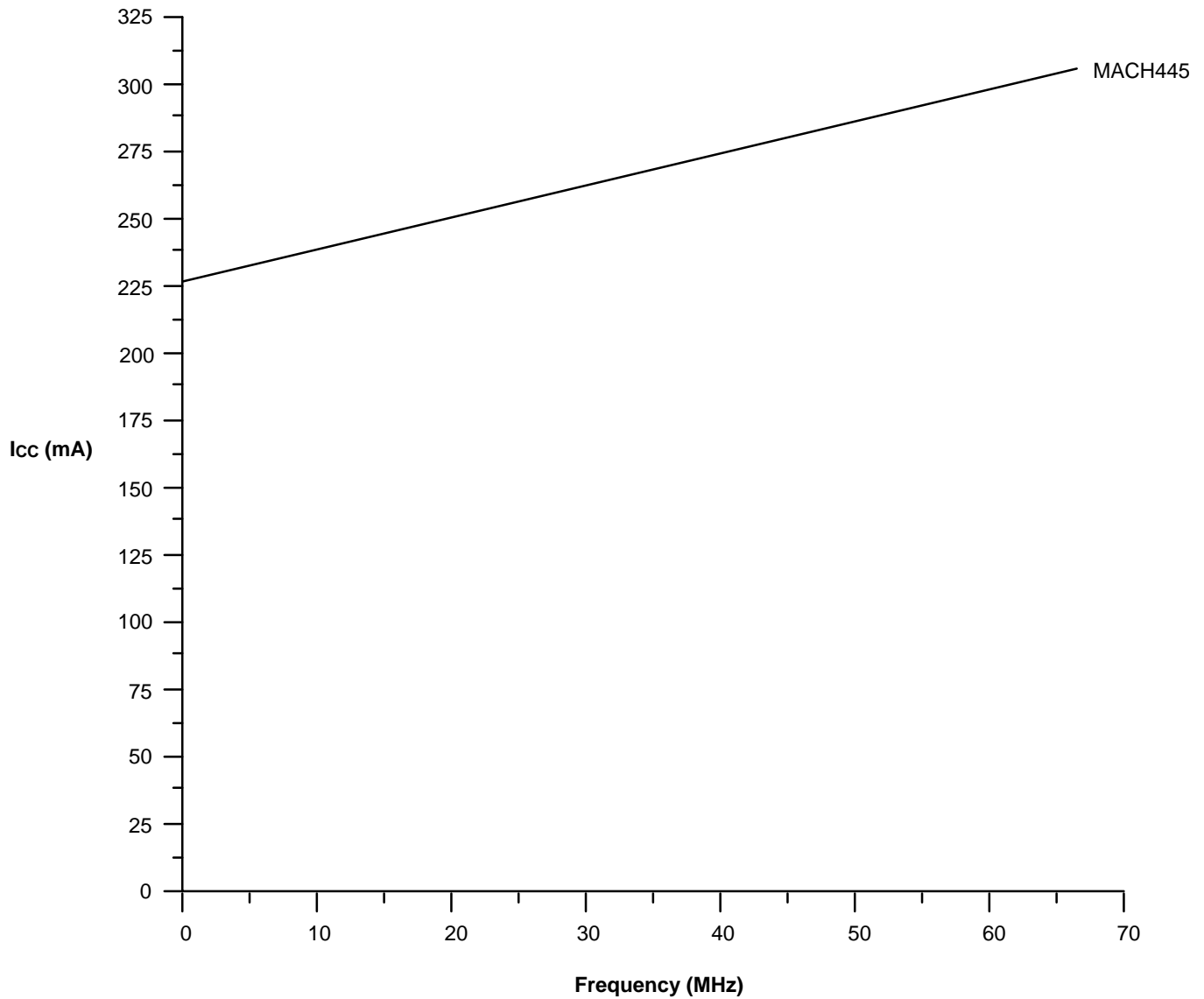
**Input**

17468E-6

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## TYPICAL $I_{CC}$ CHARACTERISTICS

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$



17468E-7

*The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

*Maximum frequency shown uses internal feedback and a D-type register.*

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## TYPICAL THERMAL CHARACTERISTICS

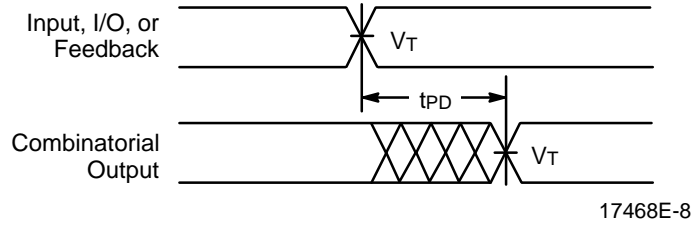
Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description	Typ	Unit	
		PQFP		
$\theta_{jc}$	Thermal impedance, junction to case	5	°C/W	
$\theta_{ja}$	Thermal impedance, junction to ambient	38	°C/W	
$\theta_{jma}$	Thermal impedance, junction to ambient with air flow	200 lpm air	32	°C/W
		400 lpm air	28	°C/W
		600 lpm air	26	°C/W
		800 lpm air	24	°C/W

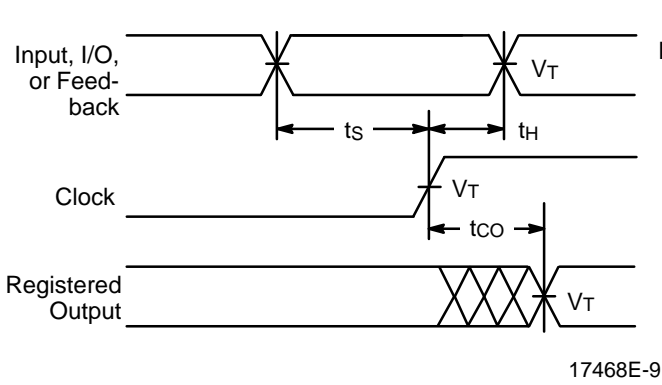
### **Plastic $\theta_{jc}$ Considerations**

*The data listed for plastic  $\theta_{jc}$  are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the  $\theta_{jc}$  measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore,  $\theta_{jc}$  tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.*

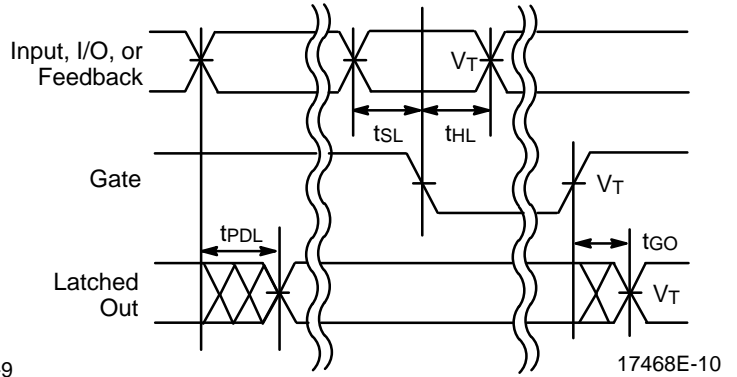
# SWITCHING WAVEFORMS



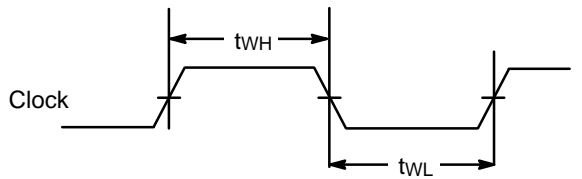
**Combinatorial Output**



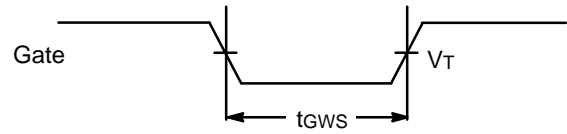
**Registered Output**



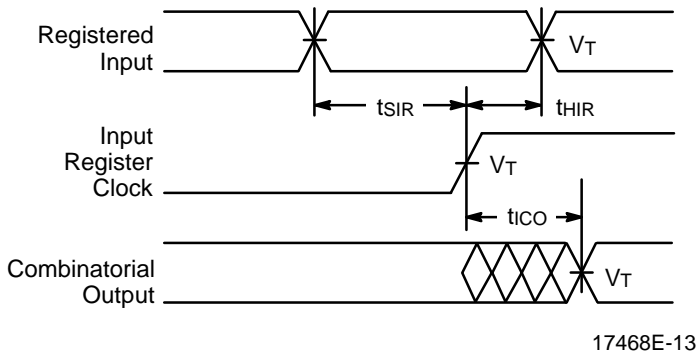
**Latched Output (MACH 2, 3, and 4)**



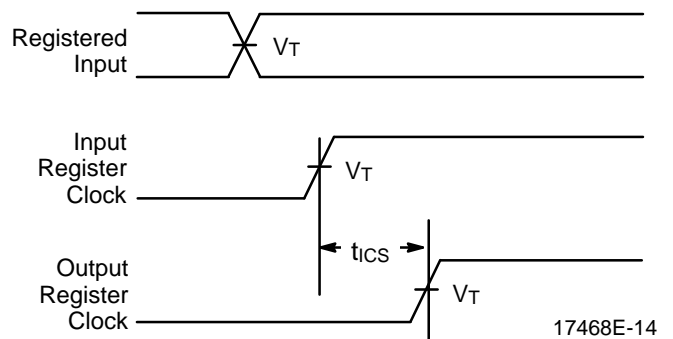
**Clock Width**



**Gate Width (MACH 2, 3, and 4)**



**Registered Input (MACH 2 and 4)**

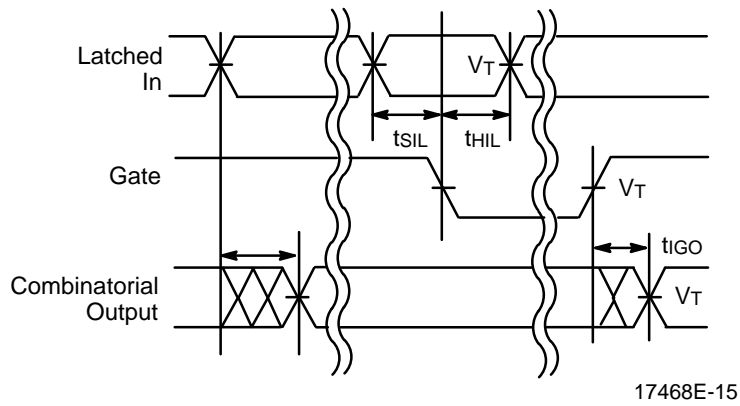


**Input Register to Output Register Setup (MACH 2 and 4)**

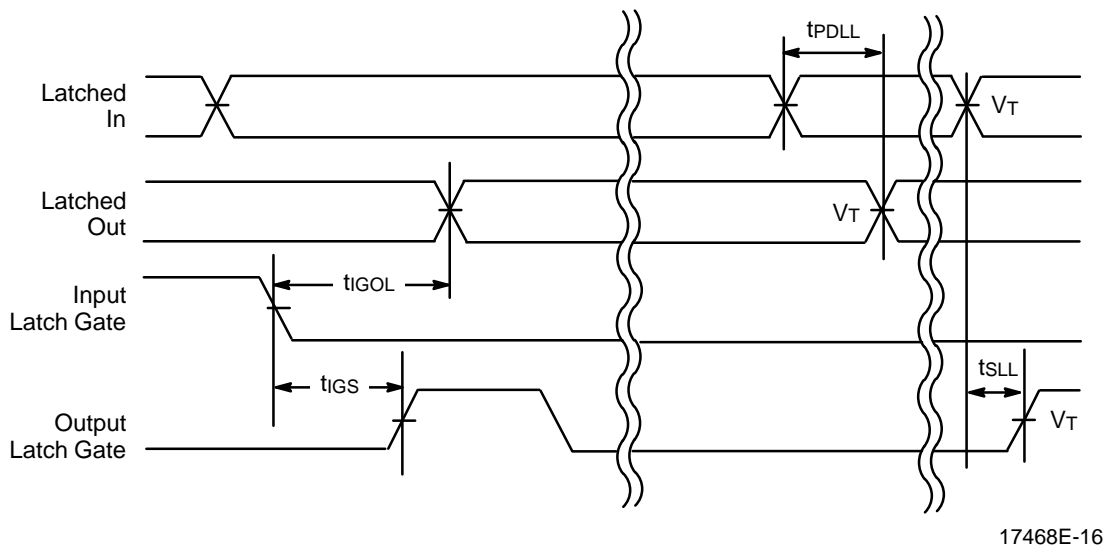
**Notes:**

1.  $V_T = 1.5\text{ V}$ .
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2 ns–4 ns typical.

## SWITCHING WAVEFORMS



Latched Input (MACH 2 and 4)

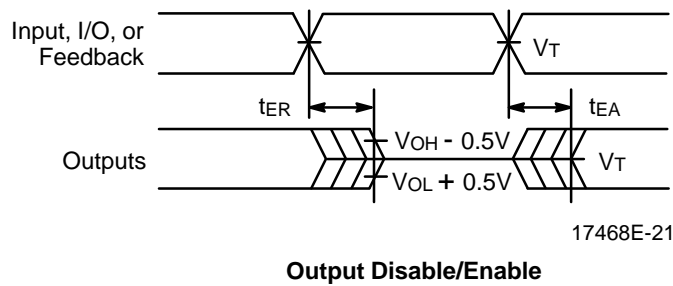
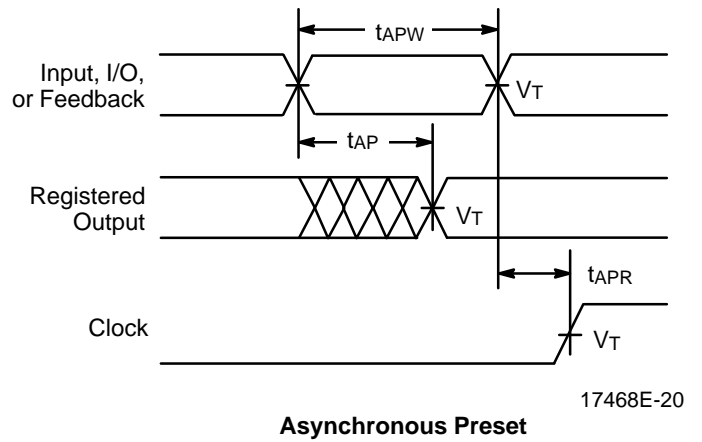
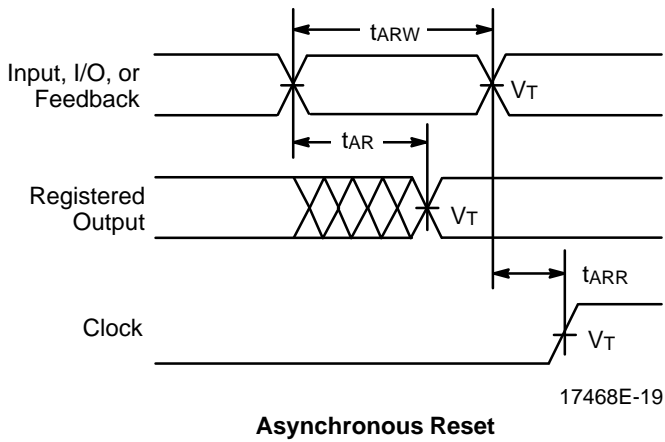
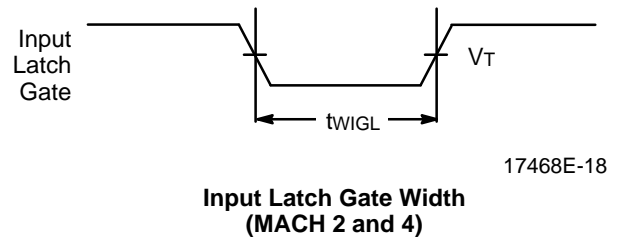
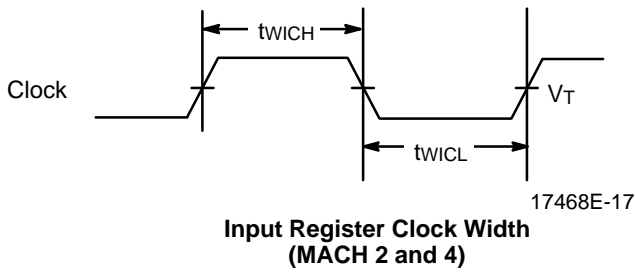


Latched Input and Output  
(MACH 2, 3, and 4)

### Notes:

1.  $V_T = 1.5 \text{ V}$ .
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2 ns–4 ns typical.




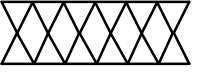
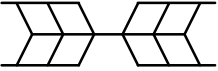
# SWITCHING WAVEFORMS



**Notes:**

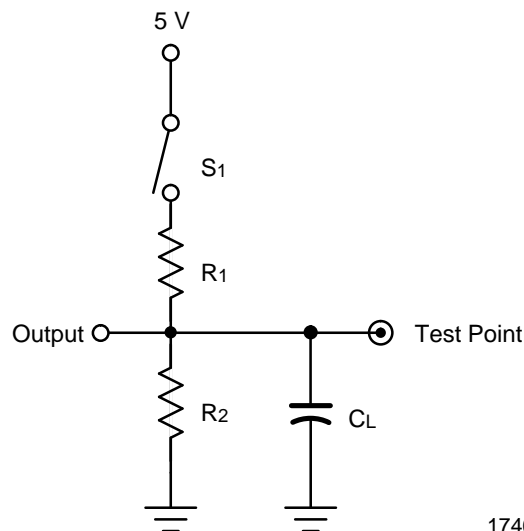
1.  $V_T = 1.5\text{ V}$ .
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2 ns–4 ns typical.

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

## SWITCHING TEST CIRCUIT



17468E-22

Specification	S <sub>1</sub>	C <sub>L</sub>	Commercial		Measured Output Value
			R <sub>1</sub>	R <sub>2</sub>	
t <sub>PD</sub> , t <sub>CO</sub>	Closed	35 pF	300 Ω	390 Ω	1.5 V
t <sub>EA</sub>	Z → H: Open Z → L: Closed				1.5 V
t <sub>ER</sub>	H → Z: Open L → Z: Closed	5 pF			H → Z: V <sub>OH</sub> - 0.5 V L → Z: V <sub>OL</sub> + 0.5 V

\*Switching several outputs simultaneously should be avoided for accurate measurement.

## f<sub>MAX</sub> PARAMETERS

The parameter f<sub>MAX</sub> is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f<sub>MAX</sub> is specified for three types of synchronous designs.

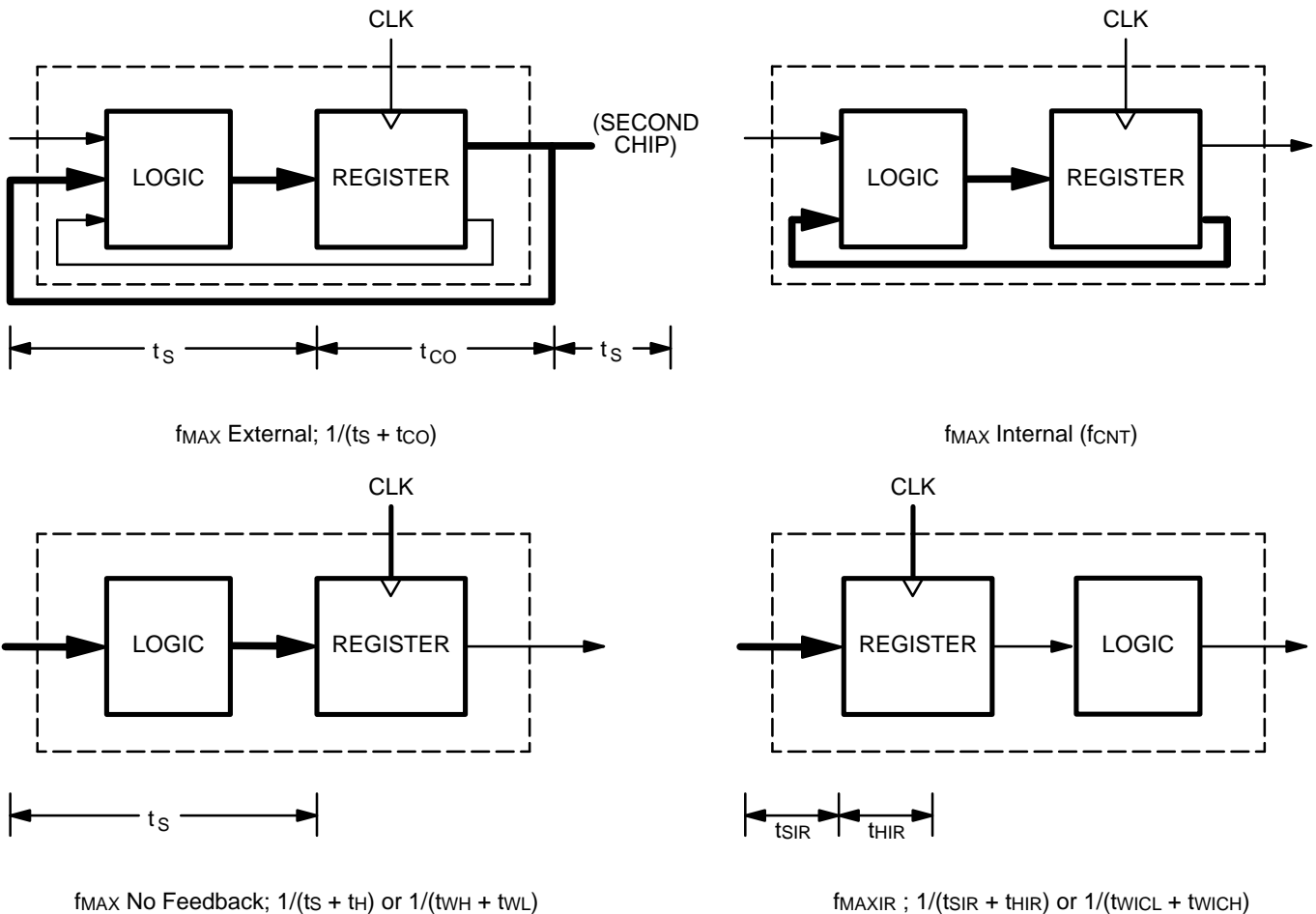
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals (t<sub>s</sub> + t<sub>CO</sub>). The reciprocal, f<sub>MAX</sub>, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f<sub>MAX</sub> is designated "f<sub>MAX</sub> external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f<sub>MAX</sub> is designated "f<sub>MAX</sub> internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "f<sub>CNT</sub>".

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time (t<sub>s</sub> + t<sub>H</sub>). However, a lower limit for the period of each f<sub>MAX</sub> type is the minimum clock period (t<sub>WH</sub> + t<sub>WL</sub>). Usually, this minimum clock period determines the period for the third f<sub>MAX</sub>, designated "f<sub>MAX</sub> no feedback."

For devices with input registers, one additional f<sub>MAX</sub> parameter is specified: f<sub>MAXIR</sub>. Because this involves no feedback, it is calculated the same way as f<sub>MAX</sub> no feedback. The minimum period will be limited either by the sum of the setup and hold times (t<sub>SIR</sub> + t<sub>HIR</sub>) or the sum of the clock widths (t<sub>WICL</sub> + t<sub>WICH</sub>). The clock widths are normally the limiting parameters, so that f<sub>MAXIR</sub> is specified as 1/(t<sub>WICL</sub> + t<sub>WICH</sub>). Note that if both input and output registers are used in the same path, the overall frequency will be limited by t<sub>ICS</sub>.

All frequencies except f<sub>MAX</sub> internal are calculated from other measured AC parameters. f<sub>MAX</sub> internal is measured directly.





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## ENDURANCE CHARACTERISTICS

The MACH families are manufactured using our advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in

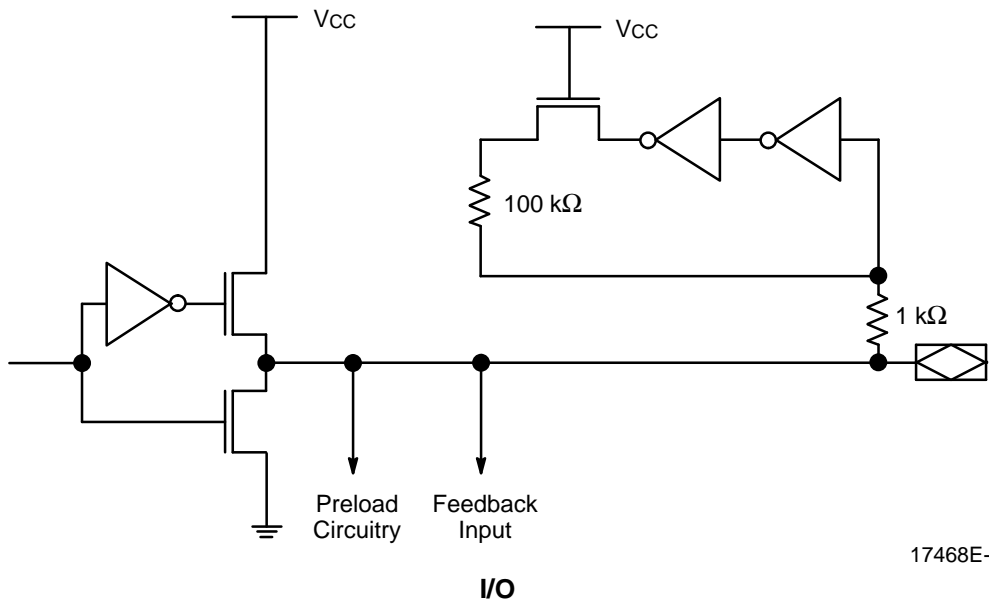
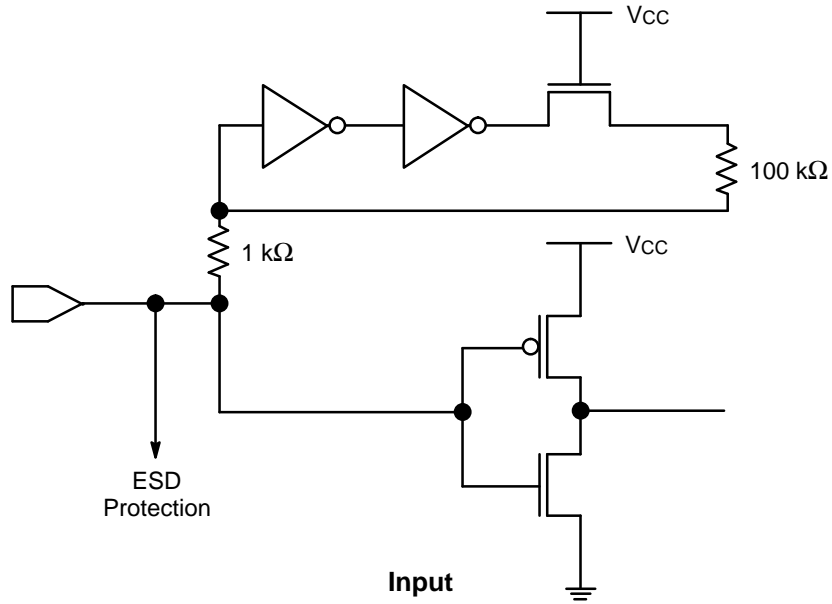
bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

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### Endurance Characteristics

Parameter Symbol	Parameter Description	Min	Units	Test Conditions
t <sub>DR</sub>	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

# INPUT/OUTPUT EQUIVALENT SCHEMATICS



17468E-24

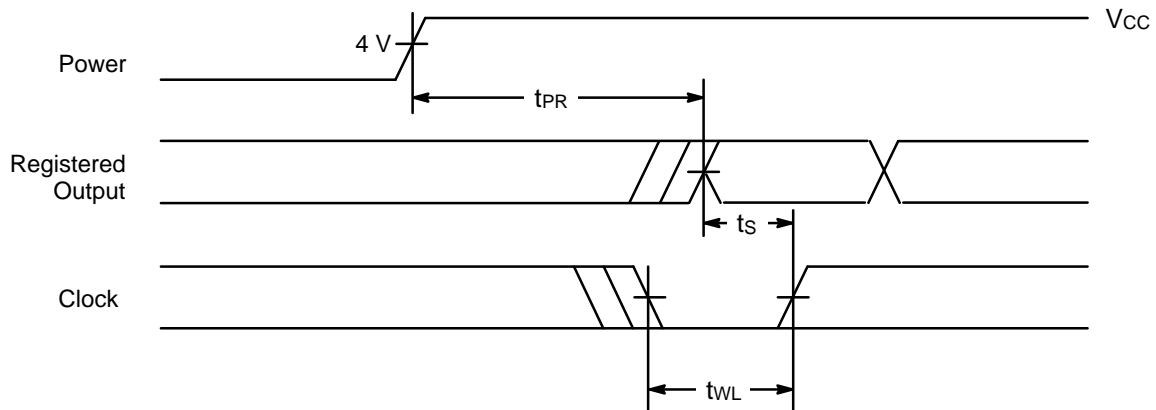
## POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the

wide range of ways  $V_{CC}$  can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The  $V_{CC}$  rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
$t_{PR}$	Power-Up Reset Time	10	$\mu s$
$t_s$	Input or Feedback Setup Time	See Switching Characteristics	
$t_{WL}$	Clock Width LOW	See Switching Characteristics	



17468E-25

Power-Up Reset Waveform

## USING PRELOAD AND OBSERVABILITY

In order to be testable, a circuit must be both controllable and observable. To achieve this, the MACH devices incorporate register preload and observability.

In preload mode, each flip-flop in the MACH device can be loaded from the I/O pins, in order to perform functional testing of complex state machines. Register preload makes it possible to run a series of tests from a known starting state, or to load illegal states and test for proper recovery. This ability to control the MACH device's internal state can shorten test sequences, since it is easier to reach the state of interest.

The observability function makes it possible to see the internal state of the buried registers during test by overriding each register's output enable and activating the output buffer. The values stored in output and buried registers can then be observed on the I/O pins. Without this feature, a thorough functional test would be impossible for any designs with buried registers.

While the implementation of the testability features is fairly straightforward, care must be taken in certain instances to insure valid testing.

One case involves asynchronous reset and preset. If the MACH registers drive asynchronous reset or preset lines and are preloaded in such a way that reset or preset are asserted, the reset or preset may remove the preloaded data. This is illustrated in Figure 2. Care should be taken when planning functional tests, so that states that will cause unexpected resets and presets are not preloaded.

Another case to be aware of arises in testing combinatorial logic. When an output is configured as combinatorial, the observability feature forces the output into registered mode. When this happens, all product terms are forced to zero, which eliminates all combinatorial data. For a straight combinatorial output, the correct value will be restored after the preload or observe function, and there will be no problem. If the function implements a combinatorial latch, however, it relies on feedback to hold the correct value, as shown in Figure 3. As this value may change during the preload or observe operation, you cannot count on the data being correct after the operation. To insure valid testing in these cases, outputs that are combinatorial latches should not be tested immediately following a preload or observe sequence, but should first be restored to a known state.

All MACH 2 devices support both preload and observability.

Contact individual programming vendors in order to verify programmer support.

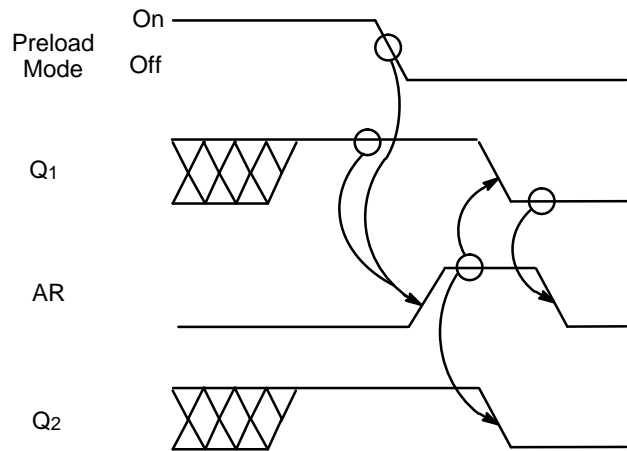
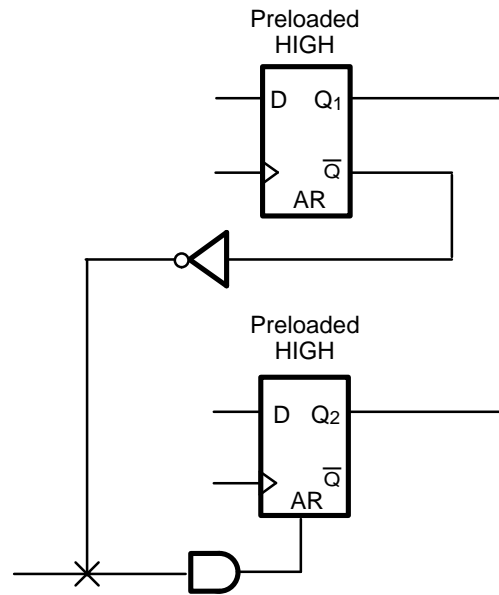


Figure 2. Preload/Reset Conflict

17468E-26

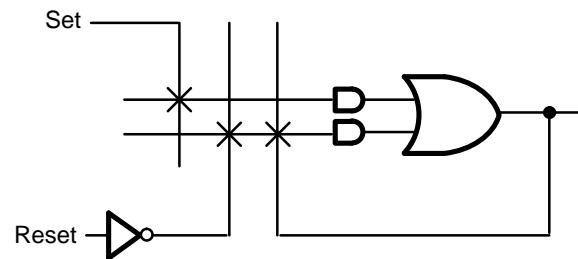


Figure 3. Combinatorial Latch

17468E-27